ANALOG DEVICES

EVAL-ADG5412FEBZ User Guide
UG-731

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Evaluation Board for the ADG5412F, Overvoltage Protected Quad SPST

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LED for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

- EVAL-ADG5412FEBZ evaluation board

DOCUMENTS NEEDED

- ADG5412F data sheet
- EVAL-ADG5412FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital voltage source: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a DMM

GENERAL DESCRIPTION

The EVAL-ADG5412FEBZ is the evaluation board for the ADG5412F, which features four independently controlled single-pole/single-throw (SPST) switches. The ADG5412F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5412FEBZ in a typical evaluation setup. The ADG5412F is soldered to the center of the evaluation board, and four wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals are used to power the device, with a fourth terminal used to provide a user defined digital voltage, if required. Alternatively, a low dropout (LDO) regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

Full specifications on the ADG5412F are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

TYPICAL EVALUATION SETUP

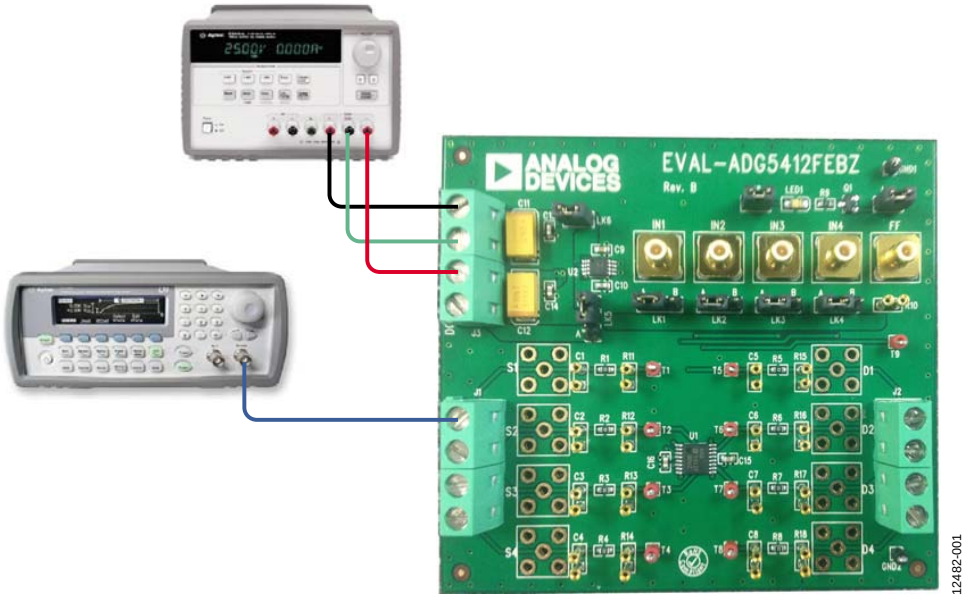

Figure 1. EVAL-ADG5412FEBZ (on Right), Power Supply, and Signal Generator

TABLE OF CONTENTS

REVISION HISTORY

8/15—Rev. 0 to Rev. A

Added Evaluation Board Schematics and Artwork Section and Figure 3 to Figure 9 6
Added Ordering Information Section, Bill of Materials Section, and Table 2 8

10/14—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5412FEBZ evaluation board is designed to be operated independently and does not require any additional evaluation boards or software to operate. An on-board LDO regulator is provided as the digital power supply for the LED and to manually control the ADG5412F.

Supply the evaluation board with a dual power source of up to ±22 V or a single supply of up to 44 V by connecting VSS and GND together. If VDD is greater than 28 V, remove the header on Link LK6 to protect the on-board LDO regulator, and change the header on LK5 to Position A to use an alternative digital voltage supply connected to DC_V1.

A simple functionality test can be set up as follows:

1. Connect a power supply to J3. Connect VSS and GND together if a single supply is required.
2. Insert the header for LK6 to use the on-board LDO regulator, and place the header for LK5 to Position B.
3. LK1 through LK4 control the digital signals for each switch on the ADG5412F.
   a. In Position A, the switch is open and presents as an open circuit.
   b. In Position B, the switch is closed and presents with a resistance of approximately 10 Ω.
4. The LED lights up to indicate that the switch is operating normally.

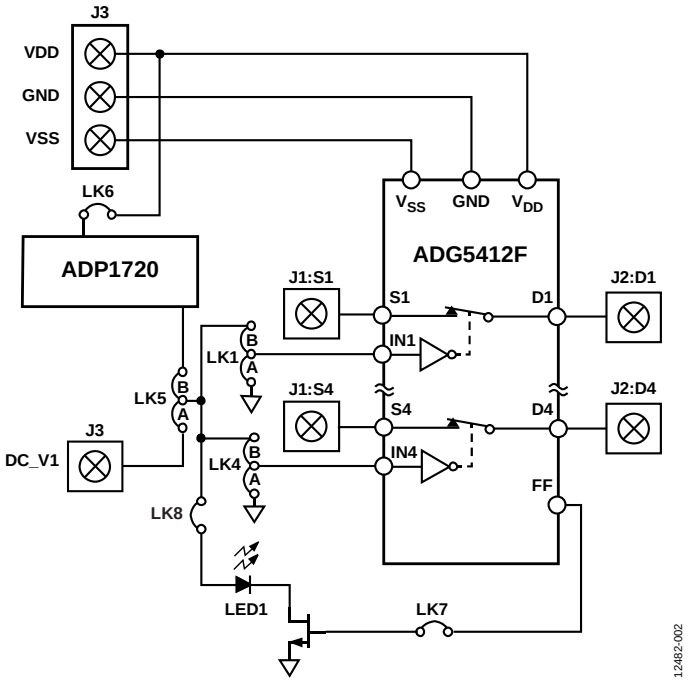

Figure 2. EVAL-ADG5412FEBZ Block Diagram

EVALUATION BOARD HARDWARE

The operation of the ADG5412F is evaluated using the EVAL-ADG5412FEBZ. Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

Using this evaluation board, the ADG5412F is used to pass signals from either the source or drain connectors. The source pins have fault detection circuitry that react to an overvoltage event. During an overvoltage event, the switch is turned off, and the FF pin is pulled low. See the ADG5412F data sheet for more details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the ADG5412F. VDD, GND, and VSS link to the appropriate pins on the ADG5412F. For dual supply voltages, the evaluation board can be powered from ±5 V to ±22 V. For single supply voltages, the GND and VSS terminals must be connected together, and the evaluation board can be powered from 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. A secondary voltage source can be connected to DC_V1 and used as the digital control voltages. To use DC_V1, place the header of LK5 into Position A. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove LK6 and supply an alternative digital voltage via DC_V1, if required.

INPUT SIGNALS

Two 4-pin screw connectors are provided to connect to both the source and drain pins of the ADG5412F. Additional SMB connector pads are available if extra connections are required. The ADG5412F is overvoltage protected on the source side, and each source terminal (S1 to S4) can be presented with a voltage of up to +55 V or −55 V. See the ADG5412F data sheet for more details.

Each trace on the source and drain side includes two sets of gold pin connectors, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the gold pin connectors can be used to create a simple resistor-capacitor (RC) filter.

The ADG5412F uses a parallel interface to control the operation of the switches. The switch operation can be manually controlled using the headers on LK1 to LK4, or an external controller can be interfaced directly to the control pins by using the SMB connectors (IN1 to IN4) and removing the link headers on LK1 to LK4.

OUTPUT SIGNALS

The only output from the ADG5412F is the FF pin. This pin indicates the operating state of the device. On the evaluation board, the FF pin controls the operation of the LED. When the device is operating normally, the FF pin remains high, and the LED turns on. If an overvoltage is presented to any of the source pins, the FF pin is pulled low, and the LED turns off. An SMB connector is provided to interface the evaluation board with an external controller, and two gold pin connectors are provided to connect a pull-up resistor between the FF signal and the digital supply.

JUMPER SETTINGS

LINK HEADERS

The link headers are used to control the ADG5412F manually, to configure the digital control voltage, and to isolate the LED from the rest of the system. Table 1 shows a summary of the link headers and how they are used on the evaluation board.

LK1 to LK4 are used to control the switches of the ADG5412F. Position A opens each switch, and Position B closes the switch.

LK6 connects the on-board LDO regulator to the VDD supply. Remove this header to protect the LDO regulator from voltages higher than 28 V. Change the header on LK5 to Position A to use an alternative digital voltage connected to DC_V1.

LK8 connects the LED to the digital power supply, and LK7 connects the FF pin of the ADG5412F to the LED control.

SMB CONNECTORS

The parallel interface of the ADG5412F is controlled manually using the link headers of LK1 to LK4, or it can be accessed using the SMB connectors, IN1 to IN4. To use the SMB connectors, remove the link headers of LK1 to LK4. The FF SMB connector is used to access the FF digital output from the ADG5412F.

Table 1. Link Header Descriptions

Link Header	Position	Description
LK1	A	S1/D1 switch open
	B	S1/D1 switch closed
LK2	A	S2/D2 switch open
	B	S2/D2 switch closed
LK3	A	S3/D3 switch open
	B	S3/D3 switch closed
LK4	A	S4/D4 switch open
	B	S4/D4 switch closed
LK5	A	On-board LDO regulator digital voltage
	B	DC_V1 digital voltage
LK6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
LK7	Inserted	FF pin connected to LED
	Removed	FF pin disconnected from LED
LK8	Inserted	LED connected to digital supply
	Removed	LED isolated

EVALUATION BOARD SCHEMATICS AND ARTWORK

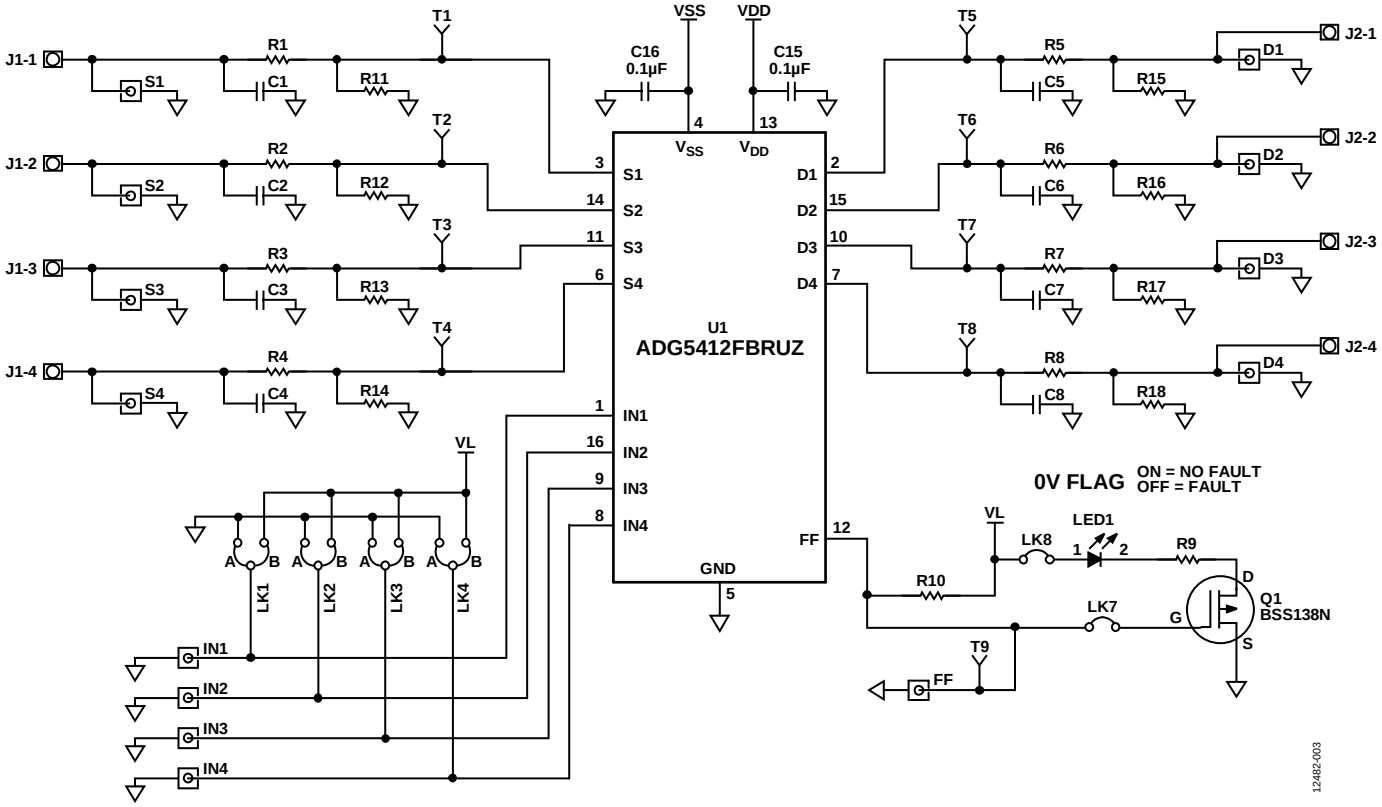

Figure 3. ADG5412F Evaluation Board Schematic—Page 1

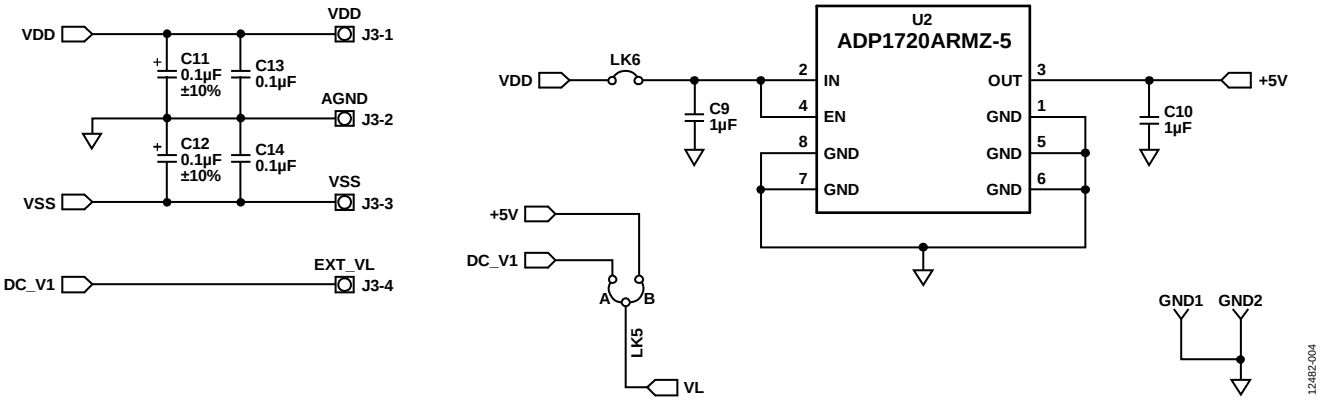

Figure 4. ADG5412F Evaluation Board Schematic—Page 1

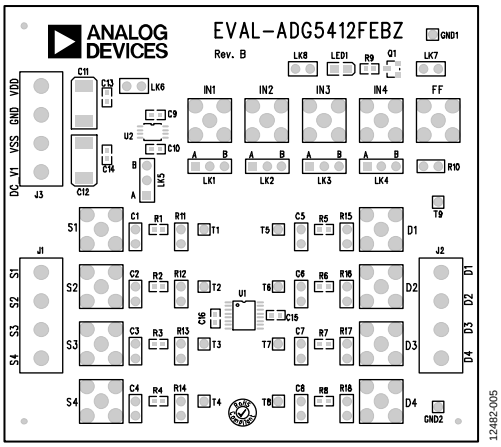

Figure 5. EVAL-ADG5412FEBZ Silkscreen

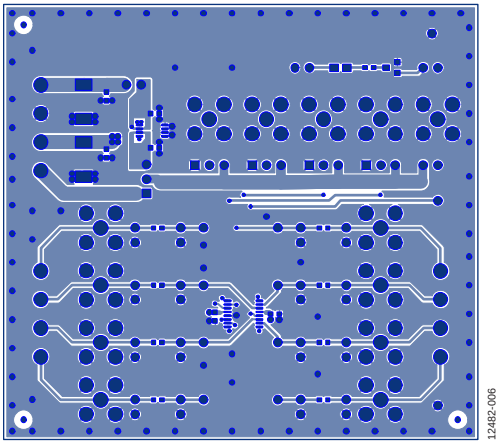

Figure 6. EVAL-ADG5412FEBZ Top Layer

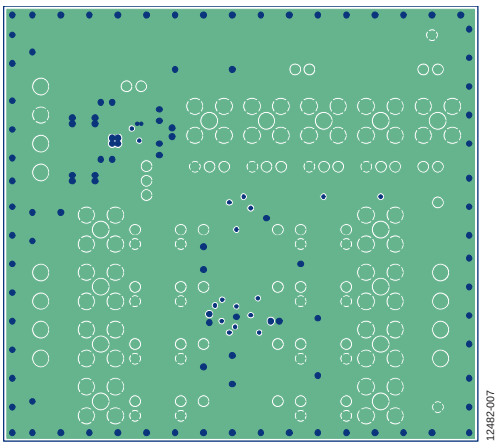

Figure 7. EVAL-ADG5412FEBZ Layer 2

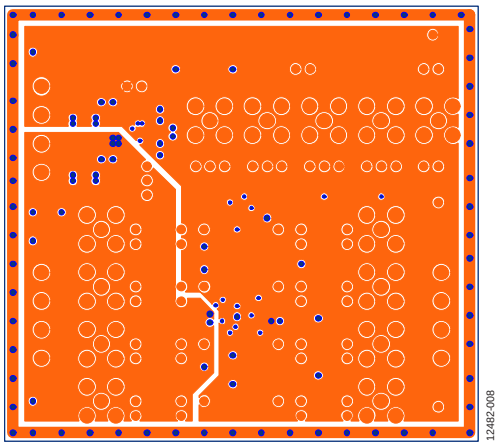

Figure 8. EVAL-ADG5412FEBZ Layer 3

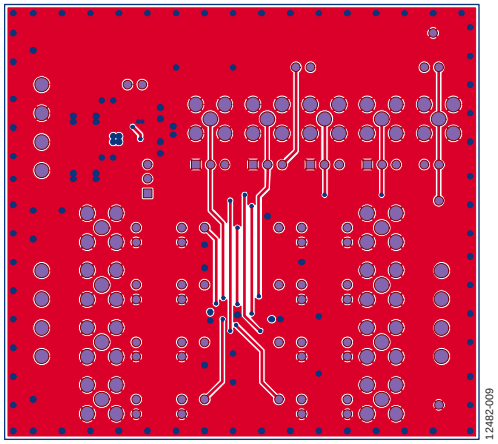

Figure 9. EVAL-ADG5412FEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer Part No.	Stock Code
C1 to C8	Socket pin, PCB, PK100 (two pins only)	66-3472	FEC 329563
C9	Capacitor, MLCC, X5R, 1 µF, 50 V, 0603	GRM188R61H105KAALD	FEC 1845736
C10	Capacitor, MLCC, X5R, 1 µF, 6.3vV, 0603	GRM188R60J105KA01D	FEC 9527699
C11, C12	50 V tantalum capacitor, D size	TAJD106K050RNJ	FEC 143-2387
C13 to C16	50 V, X7R, multilayer ceramic capacitor, 0603 size	GRM188R71H104KA93D	FEC 882-0023
D1 to D4	50 Ω, SMB socket	SMB1251B1-3GT30G-50	Do not insert
FF	50 Ω, SMB socket	SMB1251B1-3GT30G-50	FEC 1111349
GND1, GND2	Black test point	20-2137	FEC 873-1128 (pack of 100; 1 pack per 50 boards)
IN1 to IN4	50 Ω, SMB socket	SMB1251B1-3GT30G-50	FEC 1111349
J1 to J3	4-pin terminal block (5 mm pitch)	CTB5000/4	FEC 151791
LED1	LED, SMD, green, 0805	KP-2012SGC	FEC 1318243
LK1 to LK5	3-pin, SIL header and shorting link	M20-9990345 & M7567-05	FEC 1022248 & 150410
LK6 to LK8	2-pin (0.1" pitch) header and shorting shunt	M20-9990246	FEC 1022247 & 150-411
Q1	Transistor, N-channel MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R8	Resistor, 0603 1% 0R	MC0063W06030R	FEC 9331662
R9	Resistor, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K	FEC 9330380
R10 to R18	Socket pin, PCB, PK100 (two pins only)	66-3472	FEC 329563
S1 to S4	50 Ω, SMB socket	SMB1251B1-3GT30G-50	Do not insert
T1 to T9	Red test point	20-313137	FEC 873-1144 (pack of 100)
U1	Quad, SPST switch	ADG5412FBRUZ	ADG5412FBRUZ
U2	50 mA, high voltage, micropower linear regulator, 5 V	ADP1720ARMZ-5-R7	ADP1720ARMZ-5-R7

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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