PIC18(L)F1XK22 Family
Silicon Errata and Data Sheet Clarification

The PIC18(L)F1XK22 family devices that you have received conform functionally to the current Device Data Sheet (DS40001365**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F1XK22 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**AA**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the a hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F1XK22 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A3	A7	A8	AA
PIC18F14K22	4F20h	03h	07h	08h	0Ah
PIC18F13K22	4F40h	03h	07h	08h	0Ah
PIC18LF14K22	4F60h	03h	07h	08h	0Ah
PIC18LF13K22	4F80h	03h	07h	08h	0Ah

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F1XK22/LF1XK22 Flash Memory Programming Specification"* (DS41357) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3	A7	A8	AA
ADC (Analog-to-Digital Converter)	ADC Conversion	1.1	Large INL error on AN3.	X	X	X	X
ADC (Analog-to-Digital Converter)	ADC Conversion	1.2	ADC conversion does not complete.	X	X		
ECCP	Full-Bridge mode	2.1	Incorrect dead band when changing direction.	X	X	X	X
ECCP	Full-Bridge mode	2.2	Dead band ignored when changing direction.	X	X	X	X
EUSART	Asynchronous Receive mode	3.1	Unreliable RCIDL bit.	X	X	X	X
EUSART	—	3.2	OERR flag not cleared as expected.	X	X		
EUSART	—	3.3	RX and TX are unavailable for output.	X	X	X	X
EUSART	—	3.4	Unexpected results.	X	X	X	X
MSSP (Master Synchronous Serial Port)	I^2C™ Master mode	4.1	Baud rate error when SSPADD = 0x03.	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	4.2	SDI pin incorrectly sampled.	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	4.3	SCK pin unexpected pulse.	X	X	X	X
MSSP (Master Synchronous Serial Port)	I^2C Master mode	4.4	SSPADD invalid values.	X	X	X	X
MSSP (Master Synchronous Serial Port)	I^2C Master mode	4.5	RCEN bit not cleared correctly.	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	4.6	First SPI high time short.	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	4.7	Incorrect ninth pulse generated on SCK.	X	X	X	X
In-Circuit Serial Programming™ (ICSP™)	Programming	5.1	Minimum V_{DD} for ICSP™.	X	X	X	X
Oscillator	Clock Switching	6.1	FCMEN Configuration bit.	X	X	X	X
Interrupt-on-Change	Interrupt-on-Change	7.1	Interrupt-on-change.	X	X	X	X
Resets	Power-on Reset (POR)	8.1	Reset under low-power conditions.	X			
Comparators	Offset Voltage	9.1	High offset voltage at low temperatures.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**AA**).

1. Module: ADC (Analog-to-Digital Converter)

1.1 Large INL Error on AN3

ADC conversion on AN3/OSC2 will have large INL error up to approximately 8 LSb.

Work around

None for the AN3 pin. For better accuracy, use another analog pin.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

1.2 ADC Conversion Does Not Complete

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (an FOSC frequency).

   When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

Work around

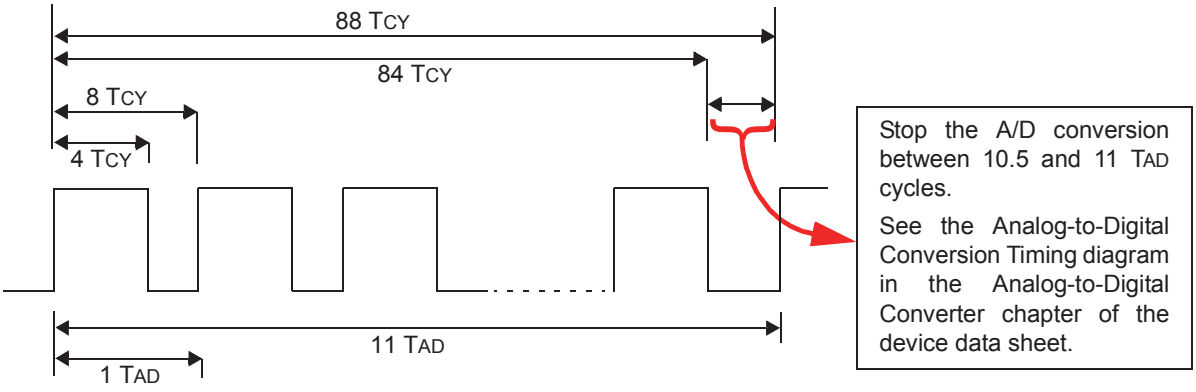
Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: Method 3 is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the Analog-to-Digital conversion manually, after all ten bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See ADC Clock Period (TAD) vs. Device Operating Frequencies Table, in the Analog-to-Digital Converter chapter of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of eight TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, GO; Start ADC conversion
               ; Provide 86 instruction
                       cycle delay here
BCF    ADCON0, GO; Terminate the conversion
                       manually
MOVF   ADRESH, W; Read conversion result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNT VS. TAD

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A3	A7	A8	AA				
X	X						

2. Module: ECCP

2.1 Incorrect Dead Band When Changing Direction

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

2.2 Dead Band Ignored When Changing Direction

In Full-Bridge mode, when PR2 = CCPR1L, DC1B<1:0> = 00, and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2 Prescale * DC1B<1:0>.

Work around

Avoid changing direction when the duty cycle is within three least significant steps of 100% duty cycle. Instead, clear the DC1B<1:0> bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

3. Module: EUSART

3.1 Unreliable RCIDL Bit

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when a low pulse greater than $1/16^{th}$ of a bit time is received on the RX input. The RCIDL bit will then improperly go high if a low pulse less than 1/16 bit time occurs on the RX input within one bit period, after the falling edge of the first pulse. This erratum affects only users monitoring the RCIDL bit as a part of their serial protocol.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

3.2 OERR Flag Not Cleared as Expected

The OERR flag of the RCSTA register is reset only by either clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit in lieu of clearing the SPEN bit.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X						

3.3 RX and TX are Unavailable for Output

When the SPEN bit of the RCSTA register is set and the CREN bit of the RCSTA register is clear, the RX pin is not available for general purpose output. Likewise, when the SPEN bit of the RCSTA register is set and the TXEN bit of the TXSTA register is clear, the TX pin is not available for general purpose output. However, both the RX and TX pins can be read regardless of the state of the RCSTA and TXSTA control registers.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

3.4 Unexpected Results

Unexpected results occur if the EUSART is disabled and then re-enabled with the EUSART receive interrupt and global interrupts enabled, then a single-cycle instruction is followed by a 2-cycle instruction.

Work around

Always execute at least two single-cycle instructions, immediately following setting the SPEN bit to '1'.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4. Module: MSSP (Master Synchronous Serial Port)

4.1 Baud Rate Error When SSPADD = 0x03

In I^2C™ Master mode, baud rates obtained by setting SSPADD to a value less than 0x03 will cause unexpected operation.

Work around

Ensure SSPADD is set to a value greater than or equal to 0x03.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.2 SDI Pin Incorrectly Sampled

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.3 SCK Pin Unexpected Pulse

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

Work around

Configure the SCK pin as an input until after the MSSP is setup.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.4 SSPADD Invalid Values

In I^2C Master mode, SSPADD values of 0x00, 0x01, 0x02 are invalid. The current I^2C Baud Rate Generator (BRG) is not set up to generate a clock signal for these values.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.5 RCEN Bit Not Cleared Correctly

In I^2C Master mode, the RCEN bit is not cleared by hardware if improper Stop is received on the bus.

Work around

Reset the module via clearing and setting the SSPEN bit of SSPCON1.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.6 First SPI High Time Short

In SPI Master mode, when the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

4.7 Incorrect Ninth Pulse Generated on SCK

In any SPI Master mode, SCK = TMR2/2, if SSPBUF is written to while shifting out data, a ninth SCK pulse is incorrectly generated. At that point, the module locks the user from writing to the SSPBUF register, but a write attempt will still cause eight or nine more SCK pulses to be generated.

Work around

The WCOL bit of the SSPCON register is correctly set to indicate that there was a write collision. Any time this bit is set, the module must be disabled and enabled (toggle SSPEN) to return to the correct operation. The bus will remain out of synchronization.

Affected Silicon Revisions.

A3	A7	A8	AA				
X	X	X	X				

5. Module: In-Circuit Serial Programming™ (ICSP™)

5.1 Minimum VDD for ICSP

The device cannot be programmed using ICSP when the device VDD is less than 2.0V.

Work around

Ensure that the device voltage is 2.0V or higher when programming the device.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

6. Module: Oscillator

6.1 Clock Switching

When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.

Work around

The IESO Configuration bit must also be set when the FCMEN Configuration bit is set.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

7. Module: Interrupt-on-Change

7.1 Interrupt-on-Change

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration, then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

8. Module: Resets

8.1 Reset Under Low-Power Conditions

Note: This issue pertains only to the F product versions, PIC18F14K22/13K22. The LF product versions, PIC18LF14K22/13K22, are not affected by this issue in any way.

When employing any one of the low-power oscillators (ECL mode, LP mode, LFINTOSC or Timer1 Oscillator) at temperatures of -20°C or colder, while at the same time the source voltage supplied to the VDD pin drops below 2.4 volts, the device may experience a Power-on Reset (POR). Also, when the source voltage supplied to the VDD pin is below 2.4 volts, at temperatures of -20°C or colder, and a SLEEP instruction is executed, the device may experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are four work-arounds available to avoid this Reset condition:

1. Enabling the Brown-out Reset (BOR) circuitry.
2. Enabling the Fixed Voltage Reference (FVR) module.
3. Maintaining a source voltage (VDD) to the device above 2.4 volts when operating at temperatures of -20°C or colder.
4. Use the LF product version (PIC18LF14K22/13K22) where the operational VDD requirement is between 1.8V and 3.6V.

Affected Silicon Revisions

A3	A7	A8	AA				
X							

9. Module: Comparators

9.1 High Offset Voltage at Low Temperatures

Comparators may have up to ±70 mV of Input Offset Voltage at temperatures below -10°C when comparators are configured to operate in High-Power mode.

Work around

None.

Affected Silicon Revisions

A3	A7	A8	AA				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001365**F**).

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ECCP

The introductory paragraphs and the definition of the ECCP1AS register in Section 13.4.4 "Enhanced PWM Auto-Shutdown Mode" have been changed as shown below in bold text.

13.4.4 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPAS<2:0> bits of the ECCPAS register. A shutdown event may be generated by:

- A logic '0' on the **INT1** pin
- A logic '1' on a comparator (Cx) output

REGISTER 13-2: ECCP1AS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ECCPASE:** ECCP Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; ECCP outputs are in shutdown state
0 = ECCP outputs are operating

bit 6-4 **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits
000 = Auto-Shutdown is disabled
001 = Comparator C1OUT output is high
010 = Comparator C2OUT output is high
011 = Either Comparator C1OUT or C2OUT is high
100 = VIL on **INT1** pin
101 = VIL on **INT1** pin or Comparator C1OUT output is high
110 = VIL on **INT1** pin or Comparator C2OUT output is high
111 = VIL on **INT1** pin or Comparator C1OUT or Comparator C2OUT is high

bit 3-2 **PSSACn:** Pins P1A and P1C Shutdown State Control bits
00 = Drive pins P1A and P1C to '0'
01 = Drive pins P1A and P1C to '1'
1x = Pins P1A and P1C tri-state

bit 1-0 **PSSBDn:** Pins P1B and P1D Shutdown State Control bits
00 = Drive pins P1B and P1D to '0'
01 = Drive pins P1B and P1D to '1'
1x = Pins P1B and P1D tri-state

2. Module: ECCP

Table 13-3 has been updated to include the INTCON3 register as shown below:

TABLE 13-3: REGISTERS ASSOCIATED WITH ECCP1 MODULE AND TIMER1 TO TIMER3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
CCPR1H	Capture/Compare/PWM Register 1, High Byte								255
CCPR1L	Capture/Compare/PWM Register 1, Low Byte								255
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	255
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	255
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RABIE	TMR0IF	INT0IF	RABIF	253
INTCON3	**INT2IP**	**INT1IP**	**—**	**INT2IE**	**INT1IE**	**—**	**INT2IF**	**INT1IF**	**253**
IPR1	—	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	256
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCLIP	—	TMR3IP	—	256
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	256
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCLIE	—	TMR3IE	—	256
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	256
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCLIF	—	TMR3IF	—	256
PR2	Timer2 Period Register								254
PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	255
RCON	IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	254
TMR1H	Timer1 Register, High Byte								254
TMR1L	Timer1 Register, Low Byte								254
TMR2	Timer2 Register								254
TMR3H	Timer3 Register, High Byte								255
TMR3L	Timer3 Register, Low Byte								255
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	256
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	254
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	254
T3CON	RD16	—	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYNC}$	TMR3CS	TMR3ON	255

Legend: — = unimplemented, read as '0'. Shaded cells are not used during ECCP operation.

3. Module: Product Identification System

The Product Identification System should be as follows:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](2)	X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Pattern

Device:	PIC18F13K22, PIC18LF13K22 PIC18F14K22, PIC18LF14K22
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1), (2)
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:	ML = QFN P = PDIP SO = SOIC SS = SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F14K22-E/P 301 = Extended temp., PDIP package, QTP pattern #301.

b) PIC18LF14K22-E/SO = Extended temp., SOIC package.

c) PIC18LF14K22-E/ML = Extended temp., QFN package.

d) PIC18F13K22T-I/SS = Industrial temp., SSOP package, Tape and Reel.

e) PIC18F14K22T-E/SO = Extended temp., SOIC package, Tape and Reel.

Note 1: Tape and Reel option is available for ML, MV, PT, SO and SS packages.

2: Tape and Reel identifier only appears in catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (3/2009)

Initial release of this document.

Rev. B Document (5/2009)

Revised Table 1; Added Table 2; Added Module 8: Internal Oscillator.

Added Data Sheet Clarifications Module 1: Electrical Specifications and Module 2: Device Overview.

Rev. C Document (4/2010)

Updated Table 1 and Table 2 adding revisions A7 and A8; Added Module 1.2; Added Module 3.4; Added Module 9: PORTB Interrupt-on-Change.

Data Sheet Clarifications:

Removed Modules 1 and 2.

Rev. D Document (7/2010)

Deleted Module 5, Module 6 and renumbered modules; Added Module 8 (Resets).

Rev. E Document (8/2011)

Added Module 9, Comparators; Other minor corrections.

Rev. F Document (11/2011)

Added Silicon Revision AA; Updated Table 2; Added titles to Modules 1.1, 1.2, 2.1, 2.2, 3.1 to 3.4, 4.1 to 4.7, 5.1 and 7.1; Other minor corrections.

Rev. G Document (7/2014)

Added MPLAB X IDE; Other minor corrections.

Data Sheet Clarifications: Added Modules 1 (ECCP) and 2 (ECCP).

Rev. H Document (1/2017)

Data Sheet Clarifications: Added Module 3 - Product Identification System. Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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