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LTC5587
6GHz RMS Power Detector
with 12-bit Digital Output

DESCRIPTION

Demonstration circuit 1638A is a Mean-Squared Power Detector with integrated 12-bit ADC featuring the LTC®5587 IC.

The LTC5587 is a wide dynamic range Mean Squared RF Power Detector, operational from 10MHz to 6GHz, with sample rate up to 500ksps. The input dynamic range at 2.14GHz, with ±1dB nonlinearity, is 40dB (from –34dBm to +6dBm, single-ended 50 input). The detector output, VOUT is also the input to the internal ADC, the digital output slope is typically 70LSB/dB, and the typical output variation over temperature is ±1dB at 2.14GHz.

LTC5587 has the internal 12-bit SPI compatible ADC. DC1638A demonstrates the performance in conjunction with DC590B Quick-Eval board. The DC590B board samples the ADC at approximately 200Hz. Faster sampling rate is possible, contact LTC applications for more information.

The 1638A Demo Circuit input is optimized for wide frequency range of 1.75GHz to 2.2GHz. However, input match can be shifted down to 10MHz or up to 6GHz with simple external matching.

Design files for this demo board are available. Call the LTC factory.

Typical Performance Summary (V_{CC} = V_{DD} = OV_{DD} = 3.3V, EN=3.3V, V_{REF} =1.8V, V_{OUT} =ADC OUTPUT(LSB) *1.8/4096, T_A = 25°C, unless otherwise noted. Test circuit shown in Figure 1.)

PARAMETER	CONDITION	TYPICAL VALUE
OV_{DD} Supply Voltage		1.0 to V_{DD}
V_{DD} Supply Voltage		2.7V to 3.6V
V_{CC} Supply Voltage	Should be equal to V_{DD}	2.7V to 3.6V
V_{REF} Reference Voltage		1.4 to V_{DD} +0.05V
Total Supply Current	No RF input signal, ADC operational at 500ksps	3mA
Shutdown Current	EN = 0.3V, CONV=3.3V, ADC Sleep-Mode	0.2µA
EN Voltage	Low, Chip Disabled HIGH, Chip Enabled	0.3V max 2V min
EN Input Current	V_{EN} = 0V V_{EN} = 3.3V	0µA 20µA
Output Detector Voltage, V_{OUT}	No Input Signal Present	0.18V
Rise Time(1000pF on V_{OUT})	0.2V to 1.6V, 10% to 90%, F_{RF} = 2140 MHz	1µs
Fall Time(1000pF on V_{OUT})	1.6V to 0.2V, 90% to 10%, F_{RF} = 2140 MHz	8µs
Input Frequency Range	With external matching components	10MHz to 6GHz
f = 880MHz		
RF Input Power Range	CW input: Externally Matched to 50Ω Source	-34 to 6 dBm
Linear Dynamic Range, CW	±1 dB linearity error	40 dB
Output Slope		73LSB/dB
Logarithmic Intercept		-42dBm

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Output Variation vs Temperature	P_{IN} = -34 to +6dBm	±1 dB
Deviation from CW Response	EDGE 3π/8 Shifted 8PSK, P_{IN} = -34 to +6dBm	±0.1 dB
f = 2140MHz		
RF Input Power Range	CW input: Externally Matched to 50Ω Source	-34 to 6 dBm
Linear Dynamic Range, CW	±1 dB linearity error	43 dB
Output Slope		73 LSB/dB
Logarithmic Intercept		-42dBm
Output Variation vs Temperature	P_{IN} = -34 to +6dBm	±1 dB
Deviation from CW Response	12 dB peak-to-average ratio (4 carrier WCDMA)	±0.5 dB
F=3500MHz		
Linear Dynamic Range, CW	±1 dB linearity error	36dB
Slope		73LSB/dB
Logarithmic Intercept		-40dBm
Output Variation vs Temperature	P_{IN} = -30 to +6dBm	±1 dB
Deviation from CW Response	WiMAX OFDM Burst; P_{IN} = -34 to +4dBm	±0.5dB
ADC Resolution		
ADC Resolution	(no missing code)	12 bits
Differential Linearity Error	EN=0V, Voltage on V_{OUT}=0V to 1.8V, V_{REF}=1.8V	±0.25
Measurement Resolution	1LSB= V_{REF}/(4096*29mV/dB), V_{REF}=1.8V	15mdB

Table 1. Jumper Description for DC1638A

JUMPER	FUNCTION	RANGE/SETTING (DEFAULT)
JP1	VDD, ADC power supply voltage	3.3V
JP2	VREF, ADC reference input voltage	VREG=1.8V
JP3	OVDD, ADC output driver supply voltage	3.3V

DC590B QUICK START PROCEDURE

The DC590B is a USB controller board that allows PC to communicate through serial data interface. The Quick start guide for DC590B can be found here: http://cds.linear.com/docs/Reference%20Design/dc590B.pdf. Download and install the QuickEval software supplied for DC590B here: http://www.linear.com/designtools/software/quick_eval.jsp. Connect DC590B to the host PC with the USB A/B cable.

1. Connect the DC1638A to the DC590B USB serial controller board using the supplied 14-conductor ribbon cable.

2. Set **VCCIO on DC590B to 3.3V** on the USB controller board.
3. Set the JP4, the "EN", which will enable the EEPROM for DC590B to automatically recognize the DC1638A board with LTC5587 when connected.
4. Set JP5 to ON, for both ISO and SW, they provide the VCCIO voltage to DC1638.
5. JP1, and JP2 are not used. Leave open.

DC1638A QUICK START PROCEDURE

Demonstration circuit 1638A is easy to set up to evaluate the performance of the LTC5587. Refer to Figure 2 for measurement equipment setup and follow the procedure below:

1. Connect DC power negative (-) supply to GND test point.

2. Connect DC power positive(+) supply to VCC and EN.

3. Set JP1(VDD) to 3.3V. This will power the LTC5587 Digital supply using the on board 3.3V regulator. The on board 3.3V regulator receives power from the DC590B board.

4. Set JP2(VREF) to VREG. This will supply the VREF using the on board 1.8V regulator. The on board 1.8V regulator receives power from the VCC supply.

5. Set JP3(OVDD) to 3.3V. This will power up the ADC output digital driver using the on board 3.3V regulator, which gets the power from DC590B.

6. Connect the signal generator's output to J1(RFIN), using the SMA connector. A 3dB attenuator pad may be used to improve broadband match, which will shift the detected power range up by 3dB.

7. The LTC5587 software control panel automatically opens when the DC1638A demo board is connected to the DC590B board. Using the Quick Eval software, set the VREF voltage to 1.8V.

8. Click on Collect to start reading the ADC.

NOTES:

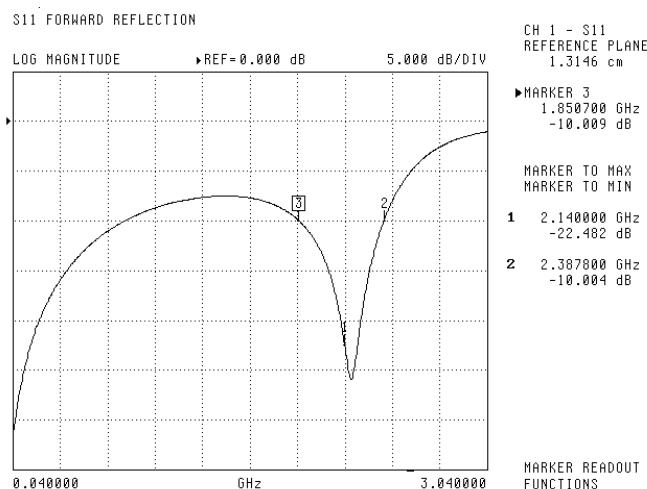1. The voltage on the EN test point must never exceed V_{CC} + 0.3V.

Figure 1. Standard Demo Board Return Loss

2. For digitally modulated signals, an oscilloscope can be used to observe the AC components of the output.

3. If no DC power supply is available. DC1638A can also be power up using the on board 3.3V regulator. Connect the 3.3V test point to VCC and EN.

4. Pin 6, C_{SQ} is the Optional Low Frequency Range Extension Capacitor. Use this pin for frequencies below 250MHz. Connect 0.01uF from Pin 8 to ground for 10MHz operation.

5. The software can display either ADC count, or the calculated voltage based on the ADC VREF input. Go to tools=>options to select.

6. The vertical axis can be toggled between Auto and Full by clicking on it at the upper left corner of the control panel.

7. Do not exceed +15dBm, the absolute maximum average RF input power.

8. Vout is the analog input voltage to the ADC. VREF defines the full-scale output range of ADC, 0V to VREF.

9. The Software allows datalog of output data, and saves the file as .adc format, which Microsoft Excel® can be used to open. Equivalent output voltage can be calculated from the ADC code based on the V_{REF} as follows.

$$Vout = \left(\frac{ADC\ Code * Vref}{4096} \right)$$

Where VREF=1.8V for the standard demo board.

10. Linearity Error at any input power level can be calculated from the Vout, given the best fit slope and Log intercept, as follows:

$$Linearity\ Error = \left(\frac{Vout}{slope} \right) + Log\ Intercept + Pin$$

Best fit slope is taken for Pin from -20dBm to 0dBm.

11. Averaging Function can be turned on by clicking on the upper left hand corner on the front control panel, Figure 3.
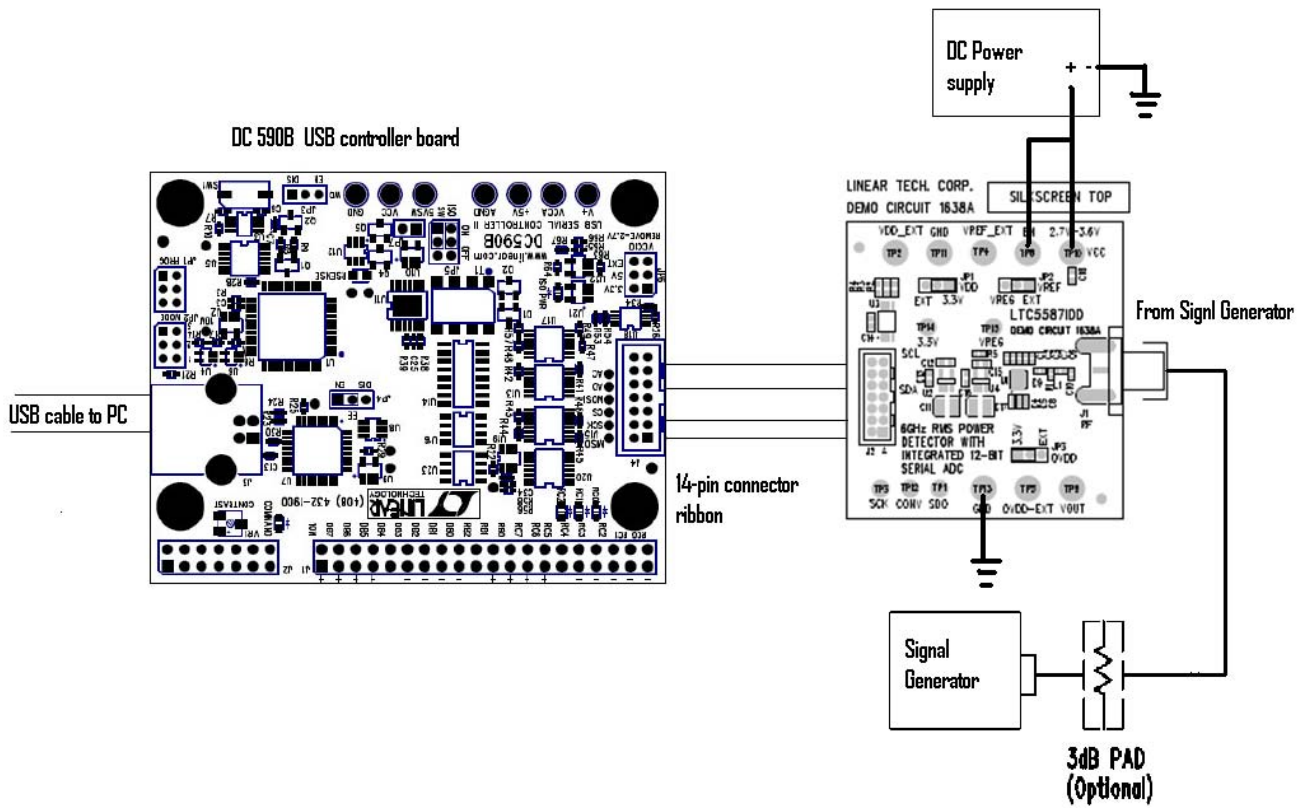
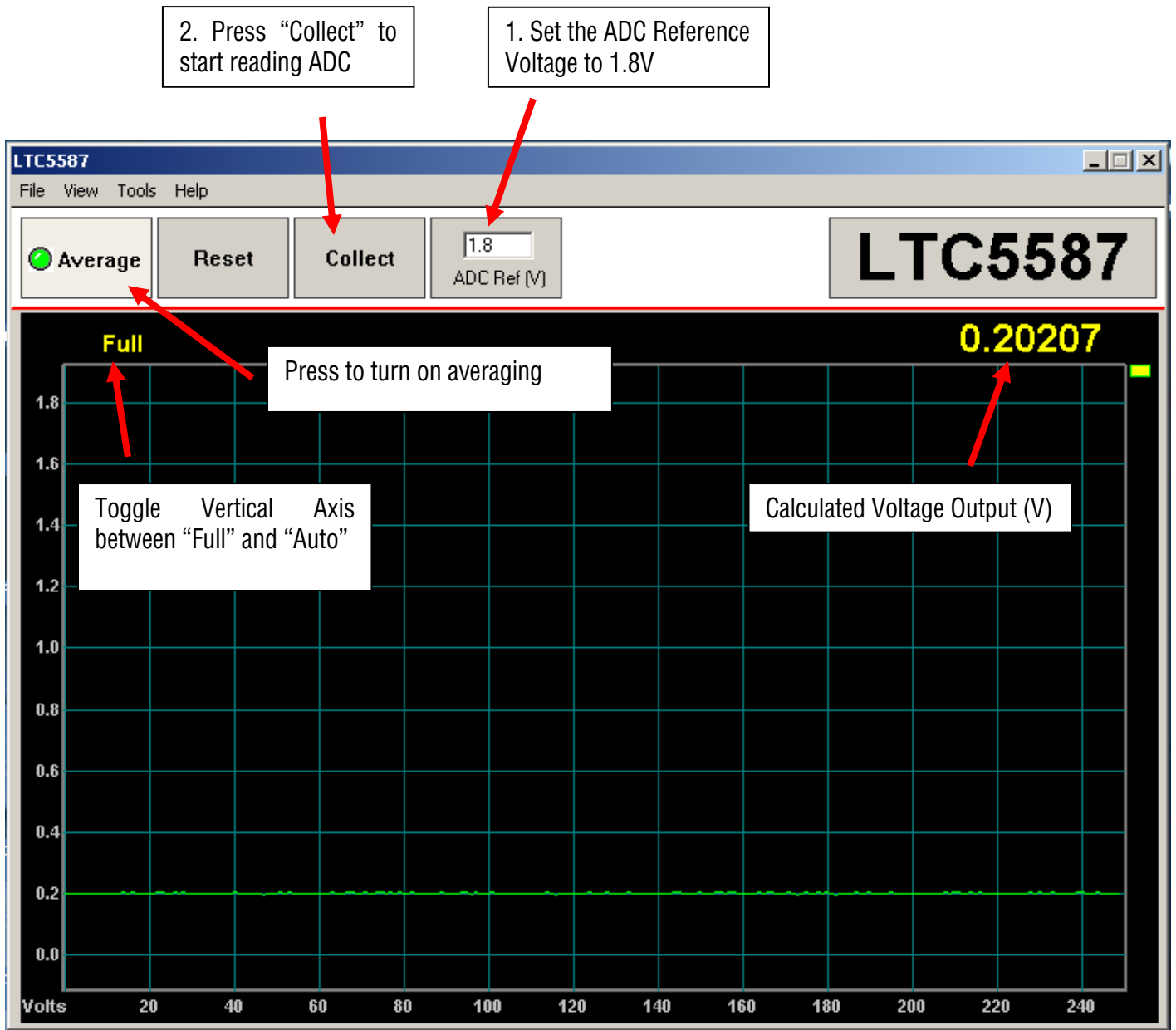**Figure 2. Proper test setup to connect DC1638A demo board to DC590A**

2. Press "Collect" to start reading ADC

1. Set the ADC Reference Voltage to 1.8V

Press to turn on averaging

Toggle Vertical Axis between "Full" and "Auto"

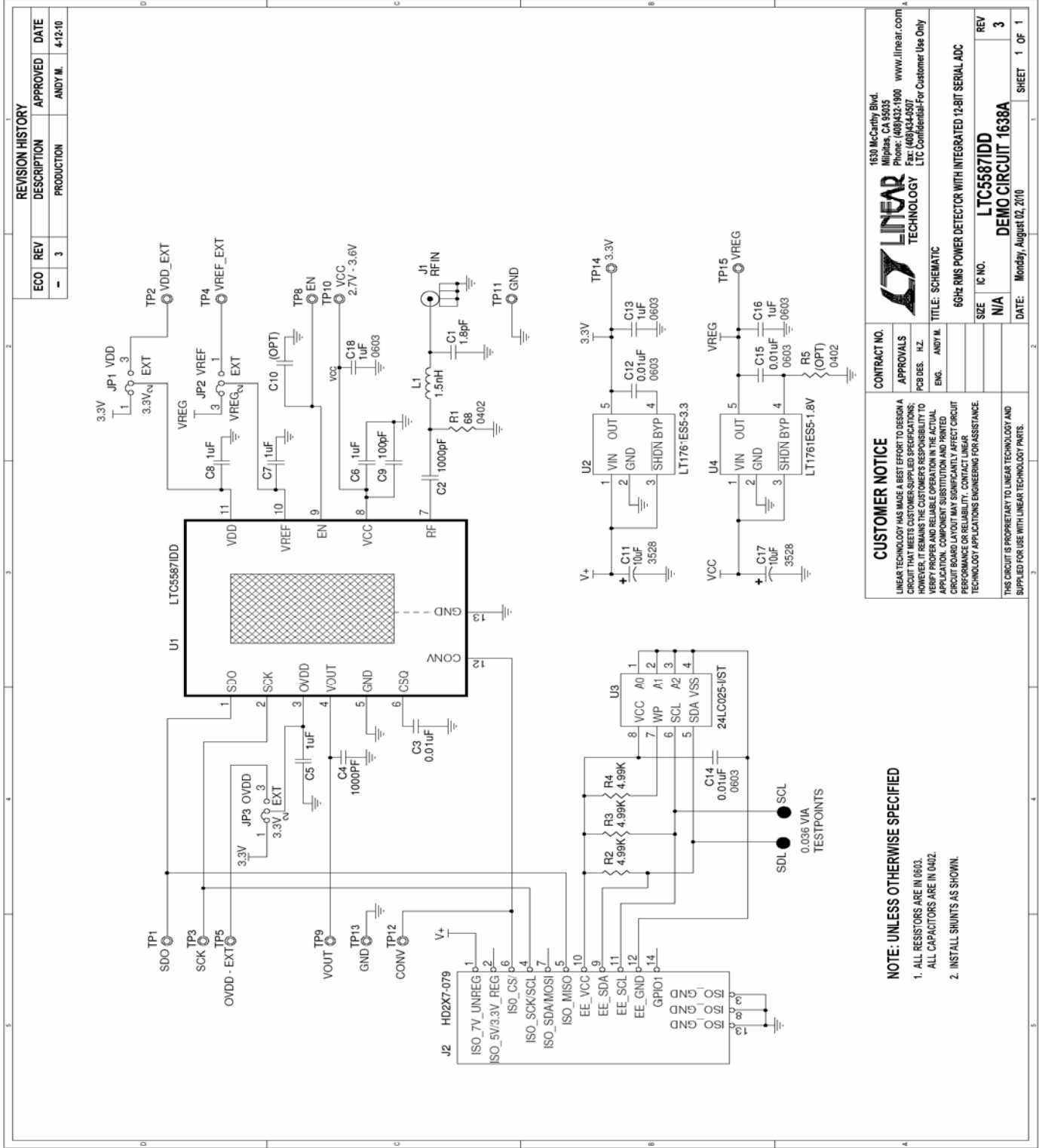Calculated Voltage Output (V)

Figure 3. Front Control Panel for LTC5587. With no RF input signal.

Table 2. RF Input Modifications for various Frequency Ranges.

FREQUENCY RANGE	RF$_{IN}$ MATCH	
	L1	C1
0.04 to 1.8GHz	3.3nH	1.8pF
1.75 to 2.2GHz	1.5nH	1.8pF
2.4 to 2.9GHz	0	1.5pF
2.8 to 3.8GHz	0	0.7pF
4.5 to 6.0GHz	0	0

Schematic

TP2 VDD_EXT
TP4 VREF_EXT
JP1 VDD
3.3V — 3.3V — EXT
VREG
JP2 VREF
3.3V — 3.3V — EXT
VREG
C10 (OPT)
TP8 EN
TP10 VCC 2.7V - 3.6V
VCC
C18 1uF 0603
J1 RFIN
TP11 GND
C1 1.8pF
L1 1.5nH
R1 68 0402
C2 1000pF

C8 1uF
C7 1uF
C6 1uF
C9 100pF

U1 LTC5587IDD

- 11 VDD
- 10 VREF
- 9 EN
- 8 VCC
- 7 RF
- 13 GND
- 12 CONV
- 1 SDO
- 2 SCK
- 3 OVDD
- 4 VOUT
- 5 GND
- 6 CSO

C5 1uF
C4 1000PF
C3 0.01uF

JP3 OVDD
3.3V — 3.3V — EXT

U2 LT176'ES5-3.3
- 1 VIN OUT 5
- 2 GND
- 3 SHDN BYP 4
TP14 3.3V
3.3V
C13 1uF 0603
C12 0.01uF 0603
V+ C11 10uF 3528

U4 LT1761ES5-1.8V
- 1 VIN OUT 5
- 2 GND
- 3 SHDN BYP 4
TP15 VREG
VREG
C16 1uF 0603
C15 0.01uF 0603
R5 (OPT) 0402
VCC C17 10uF 3528

U3 24LC025-I/ST
- 1 A0
- 2 A1
- 3 A2
- 4 SDA VSS
- 5 SDA VSS
- 6 SCL
- 7 WP
- 8 VCC
R4 4.99K
R3 4.99K
R2 4.99K
C14 0.01uF 0603

SCL
SDL
0.036 VIA TESTPOINTS

TP1 SDO
TP3 SCK
TP5 OVDD - EXT
TP9 VOUT
TP13 GND
TP12 CONV
V+

J2 HD2X7-079
- 1 ISO_7V_UNREG
- 2 ISO_5V/3.3V_REG
- 6 ISO_CS/
- 4 ISO_SCK/SCL
- 7 ISO_SDA/MOSI
- 5 ISO_MISO
- 10 EE_VCC
- 9 EE_SDA
- 11 EE_SCL
- 12 EE_GND
- 14 GPIO1
- ISO_GND
- ISO_GND
- ISO_GND

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN 0603.
   ALL CAPACITORS ARE IN 0402.

2. INSTALL SHUNTS AS SHOWN.