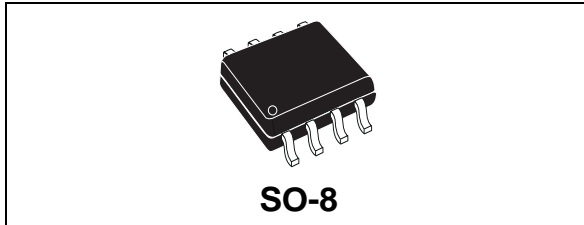


## OMNIFET III fully protected low-side driver

Datasheet - production data



### Description

The VNL5300S5-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery.

Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the device in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

### Features

Type	V <sub>clamp</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
VNL5300S5-E	41 V	300 mΩ	2 A

- Drain current: 2 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output

**Table 1. Devices summary**

Package	Order codes	
	Tube	Tape and reel
SO-8	VNL5300S5-E	VNL5300S5TR-E

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# 1 Block diagrams and pins configurations

Figure 1. Block diagram

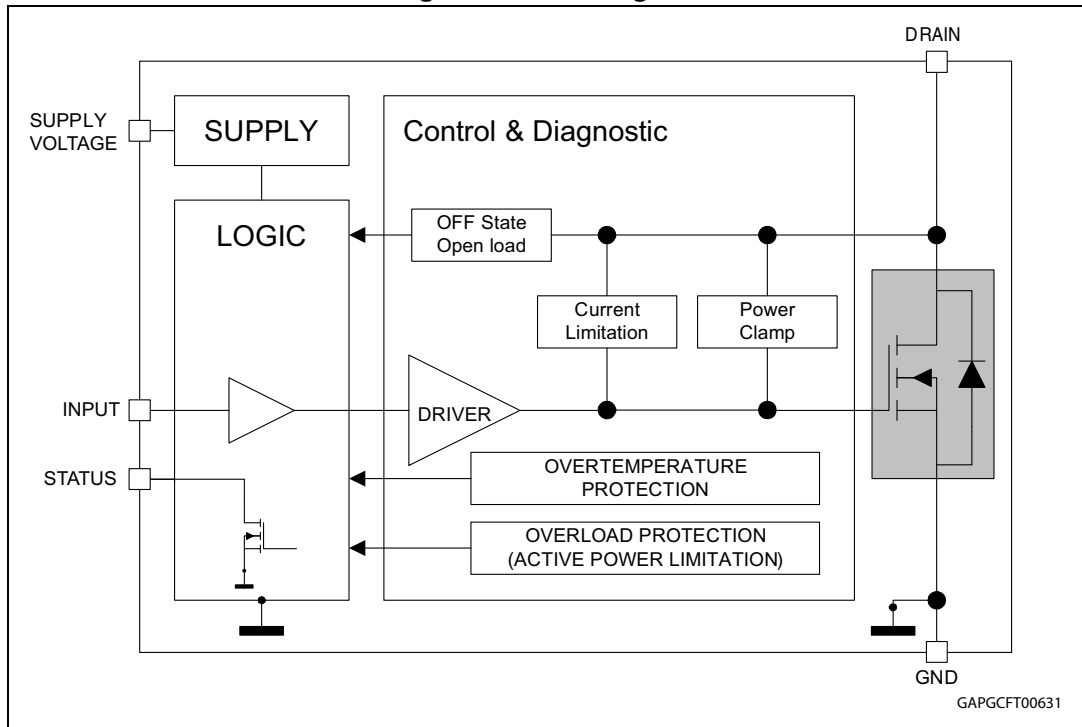


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. It Controls output switch state
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5 V)
STATUS	Open drain digital diagnostic pin

Figure 2. Current and voltage conventions

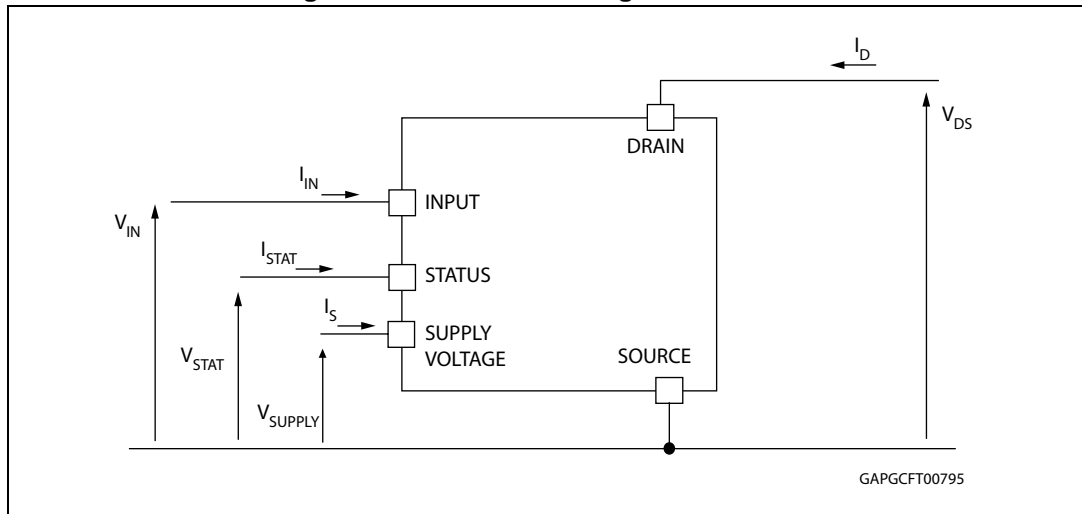


Figure 3. Configuration diagrams (top view)

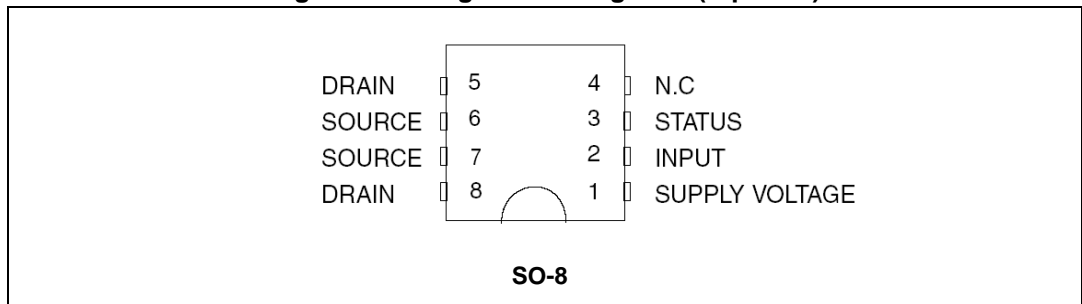


Table 3. Suggested connections for unused and N.C. pins

Connection / pin	STATUS	N.C.	INPUT
Floating	X <sup>(1)</sup>	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{IN} = 0\text{ V}$ )	Internally clamped	V
$I_D$	DC drain current	Internally limited	A
$-I_D$	Reverse DC drain current	6	A
$I_S$	DC supply current	-1 to 10	mA
$I_{IN}$	DC input current	-1 to 10	mA
$I_{STAT}$	DC status current	-1 to 10	mA
$V_{ESD1}$	Electrostatic discharge ( $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$ )		V
	– DRAIN	5000	
	– SUPPLY, INPUT, STATUS	4000	
$V_{ESD2}$	Electrostatic discharge on output pin only ( $R = 330\ \Omega$ , $C = 150\text{ pF}$ )	2000	V
$T_j$	Junction operating temperature	-40 to 150	°C
$T_{stg}$	Storage temperature	-55 to 150	°C
$E_{AS}$	Single pulse avalanche energy ( $L = 19\text{ mH}$ , $T_j = 150\text{ °C}$ , $R_L = 0$ , $I_{OUT} = I_{limL}$ )	26	mJ

### 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Maximum value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	115	°C/W

## 2.3 Electrical characteristics

Values specified in this section are for  $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$  to  $5.5 \text{ V}$ ,  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; unless otherwise stated.

**Table 6. PowerMOS section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{supply}}$	Operating supply voltage	-	3.5	5	5.5	V
$R_{\text{ON}}$	ON-state resistance	$I_D = 0.8 \text{ A}$ ; $T_j = 25^\circ\text{C}$ , $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$		300		m $\Omega$
		$I_D = 0.8 \text{ A}$ ; $T_j = 150^\circ\text{C}$ , $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$			600	
$V_{\text{CLAMP}}$	Drain-source clamp voltage	$V_{\text{IN}} = 0 \text{ V}$ ; $I_D = 0.8 \text{ A}$	41	46	52	V
$V_{\text{CLTH}}$	Drain-source clamp threshold voltage	$V_{\text{IN}} = 0 \text{ V}$ ; $I_D = 2 \text{ mA}$	36			V
$I_{\text{DSS}}$	OFF-state output current	$V_{\text{IN}} = 0 \text{ V}$ ; $V_{\text{DS}} = 13 \text{ V}$ ; $T_j = 25^\circ\text{C}$	0		3	$\mu\text{A}$
		$V_{\text{IN}} = 0 \text{ V}$ ; $V_{\text{DS}} = 13 \text{ V}$ ; $T_j = 125^\circ\text{C}$	0		5	

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}$	Forward on voltage	$I_D = 0.8 \text{ A}$ ; $V_{\text{IN}} = 0 \text{ V}$	—	0.8	—	V

**Table 8. Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{STAT}}$	Status low output voltage	$I_{\text{STAT}} = 1 \text{ mA}$			0.5	V
$I_{\text{LSTAT}}$	Status leakage current	Normal operation, $V_{\text{STAT}} = 5 \text{ V}$			10	$\mu\text{A}$
$C_{\text{STAT}}$	Status pin input capacitance	Normal operation, $V_{\text{STAT}} = 5 \text{ V}$			100	pF
$V_{\text{STCL}}$	Status clamp voltage	$I_{\text{STAT}} = 1 \text{ mA}$	5.5		7	V
		$I_{\text{STAT}} = -1 \text{ mA}$		-0.7		

**Table 9. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{IL}}$	Low-level input voltage				0.9	V
$I_{\text{IL}}$	Low-level input current	$V_{\text{IN}} = 0.9 \text{ V}$	1			$\mu\text{A}$
$V_{\text{IH}}$	High-level input voltage		2.1			V
$I_{\text{IH}}$	High-level input current	$V_{\text{IN}} = 2.1 \text{ V}$			10	$\mu\text{A}$
$V_{\text{I(hyst)}}$	Input hysteresis voltage		0.13			V



Table 9. Logic input (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1 \text{ mA}$	5.5		7	V
		$I_{IN} = -1 \text{ mA}$		-0.7		

Table 10. Openload detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OI}$	Openload OFF-state voltage detection threshold	$V_{IN} = 0 \text{ V}$	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in openload condition	$I_{OUT} = 0 \text{ A}$	45	425	1100	$\mu\text{s}$

Table 11. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Supply current	OFF-state; $T_j = 25^\circ\text{C}$ ; $V_{IN} = V_{DRAIN} = 0 \text{ V}$ ;		10	25	$\mu\text{A}$
		ON-state; $V_{IN} = 5 \text{ V}$ ; $V_{DS} = 0 \text{ V}$		25	65	
$V_{SCL}$	Supply clamp voltage	$I_{SCL} = 1 \text{ mA}$	5.5		7	V
		$I_{SCL} = -1 \text{ mA}$		-0.7		

Table 12. Switching characteristics<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	8	—	$\mu\text{s}$
$t_{d(OFF)}$	Turn-off delay time	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	12	—	$\mu\text{s}$
$t_r$	Rise time	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	11	—	$\mu\text{s}$
$t_f$	Fall time	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	7	—	$\mu\text{s}$
$W_{ON}$	Switching energy losses at turn-on	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	0.026	—	mJ
$W_{OFF}$	Switching energy losses at turn-off	$R_L = 16 \Omega$ ; $V_{CC} = 13 \text{ V}^{(2)}$	—	0.016	—	mJ
$Q_g$	Total gate charge	$V_{SUPPLY} = V_{IN} = 5 \text{ V}$	—	0.6	—	nC

1. See [Figure 5: Application schematic](#)

2. See [Figure 4: Switching characteristics](#)

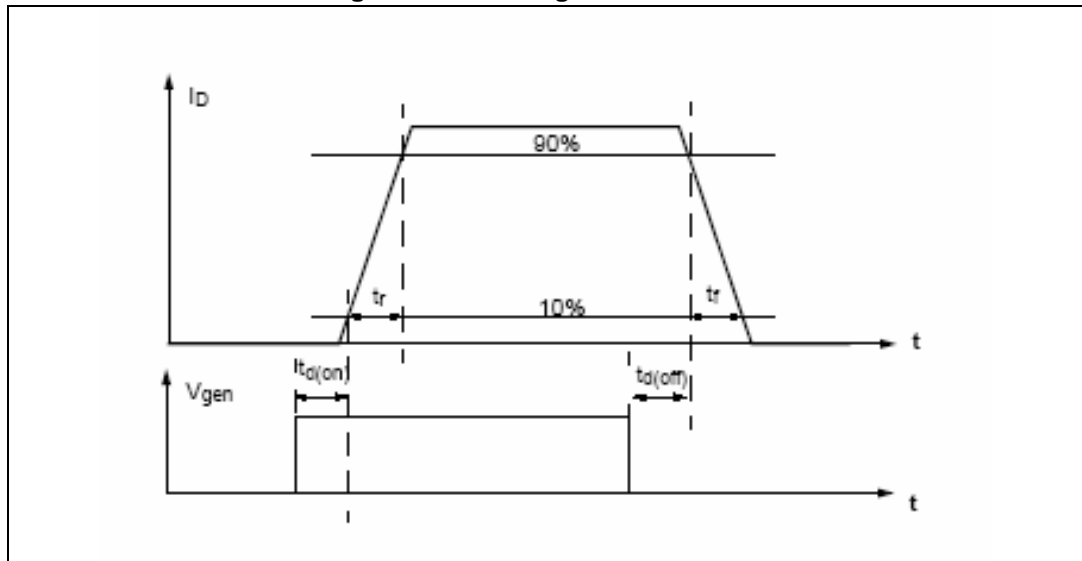
Table 13. Protection and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short-circuit current	$V_{DS} = 13\text{ V};$ $V_{supply} = V_{IN} = 5\text{ V}$	2	2.8	3.8	A
$I_{limL}$	Short-circuit current during thermal cycling	$V_{DS} = 13\text{ V}; T_R < T_j < T_{TSD};$ $V_{supply} = V_{IN} = 5\text{ V}$		1.4		A
$t_{dimL}$	Step response current limit	$V_{DS} = 13\text{ V}; V_{input} = 5\text{ V}$		7		$\mu\text{s}$
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
$T_{RS}$	Thermal reset of STATUS		135			$^{\circ}\text{C}$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		$^{\circ}\text{C}$

Table 14. Truth table

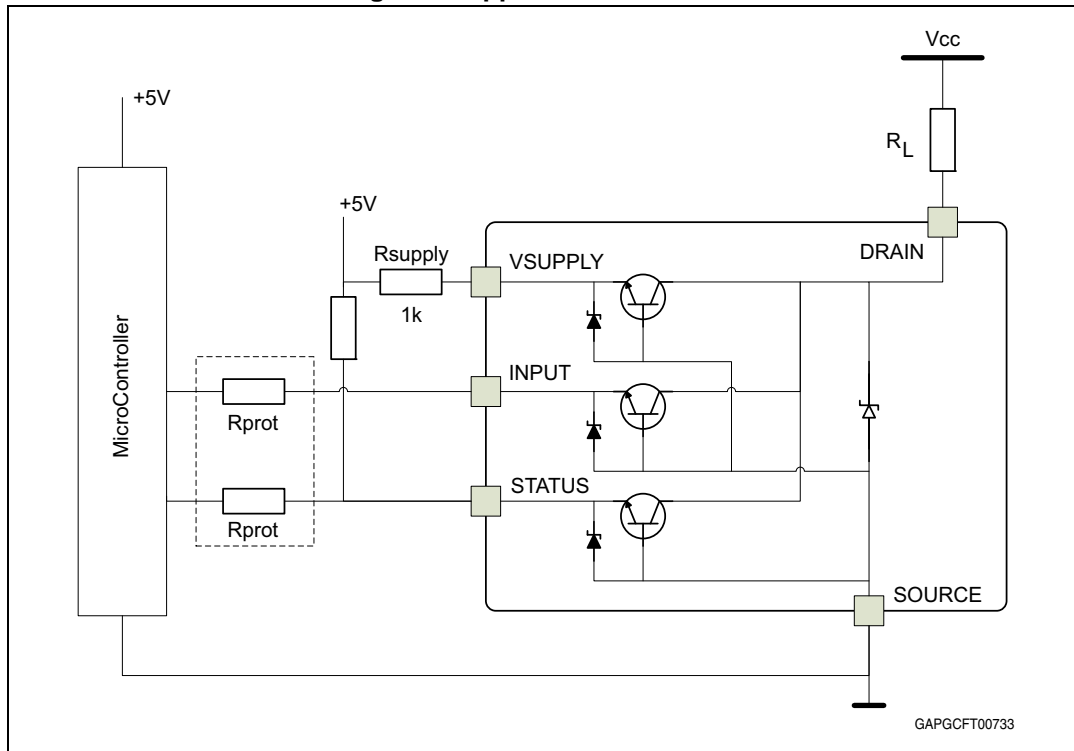
Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X
Output voltage $< V_{OL}$	L	L	L
	H	L	H

Figure 4. Switching characteristics



### 3 Application information

Figure 5. Application schematic



#### 3.1 MCU I/O protection

ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching up<sup>(a)</sup>. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

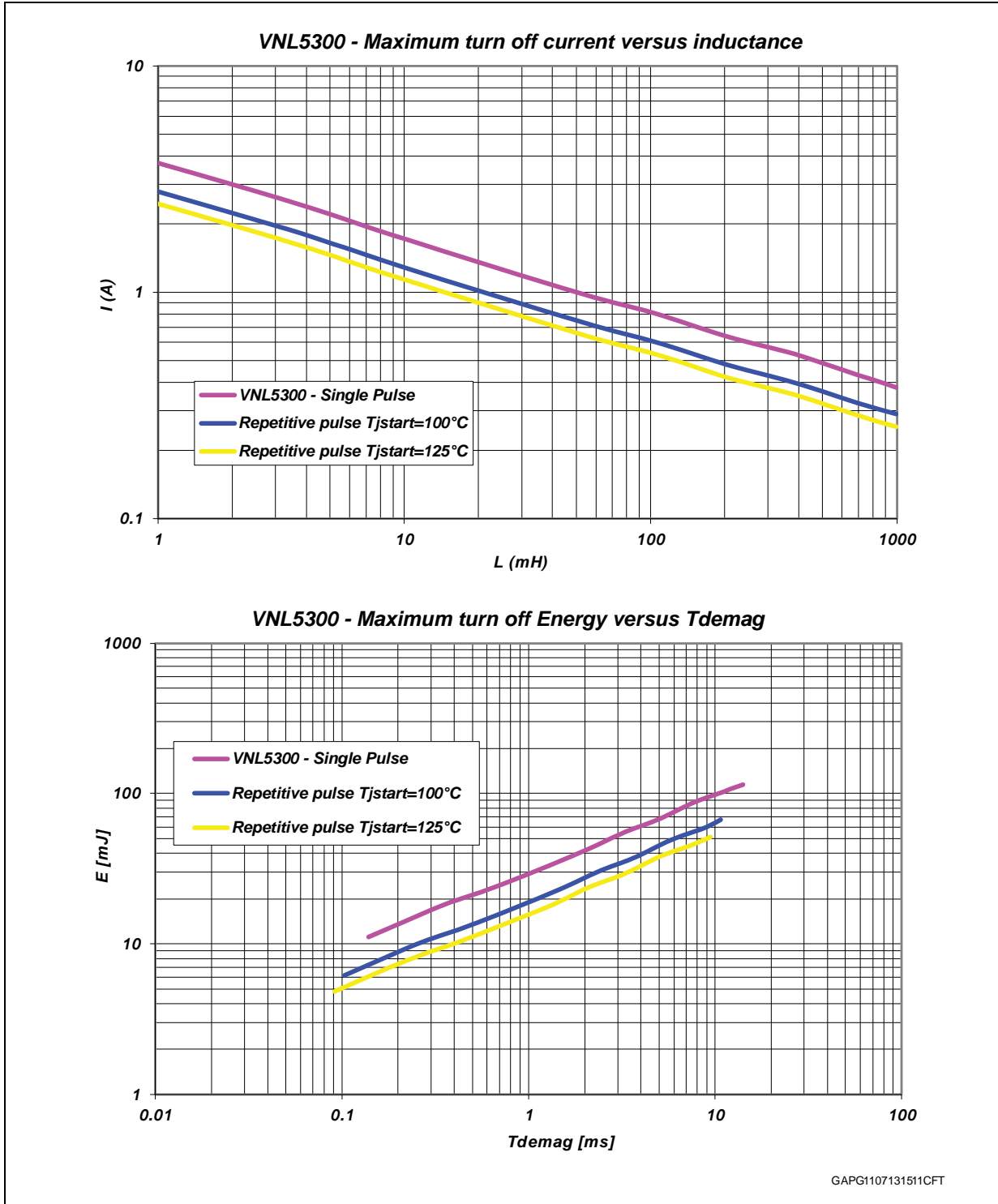
Let:

- $I_{latchup} \geq 20\ \text{mA}$
- $V_{OH\mu C} \geq 4.5\ \text{V}$
- $35\ \Omega \leq R_{prot} \leq 100\ \text{K}\Omega$

Then, the recommended value is  $R_{prot} = 1\ \text{K}\Omega$

a. In case of negative transient on the drain pin.

Figure 6. Maximum demagnetization energy

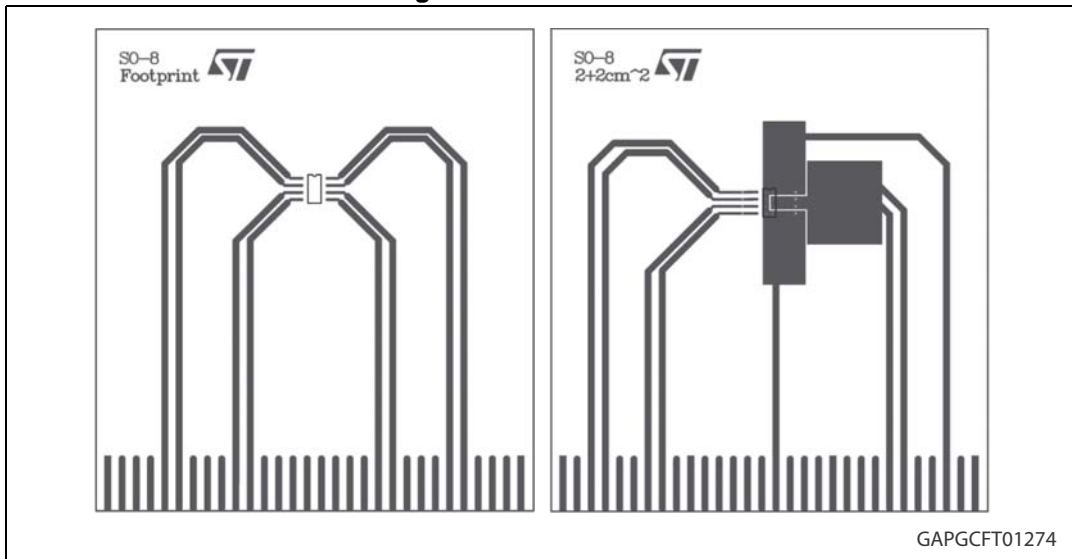


- Values are generated with  $R_{DS(on)} = 0\Omega$ .  
In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PC board thermal data

### 4.1 SO-8 thermal data

Figure 7. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 78 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal via separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 8. SO-8  $R_{thj-amb}$  vs PCB copper area in open box free air condition

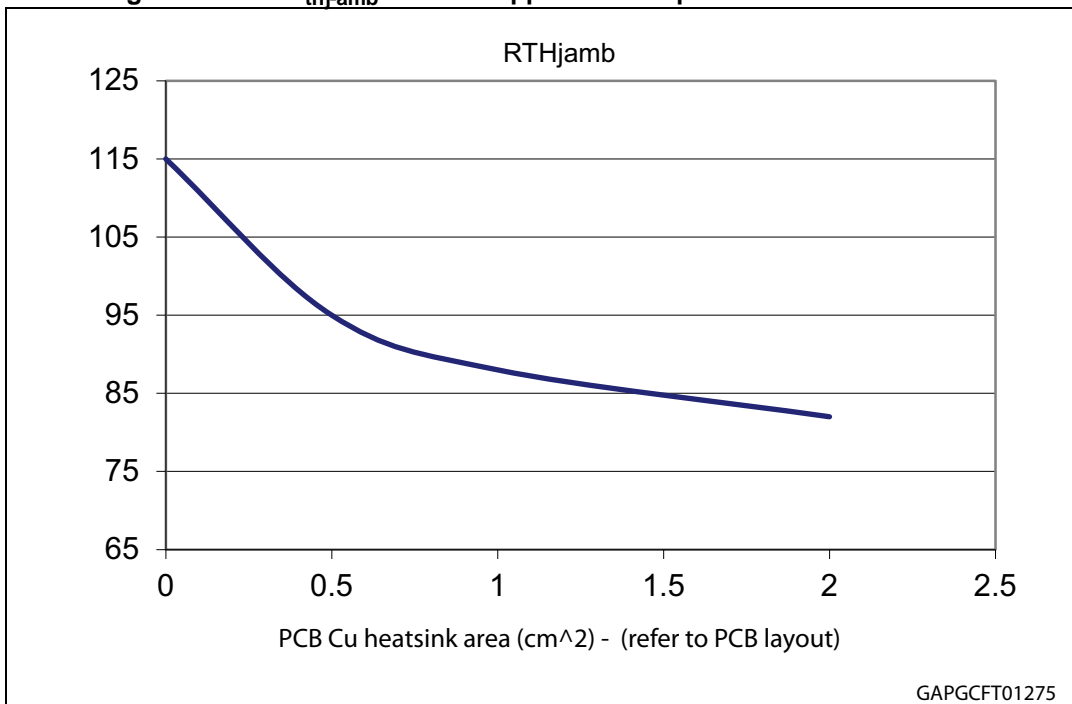
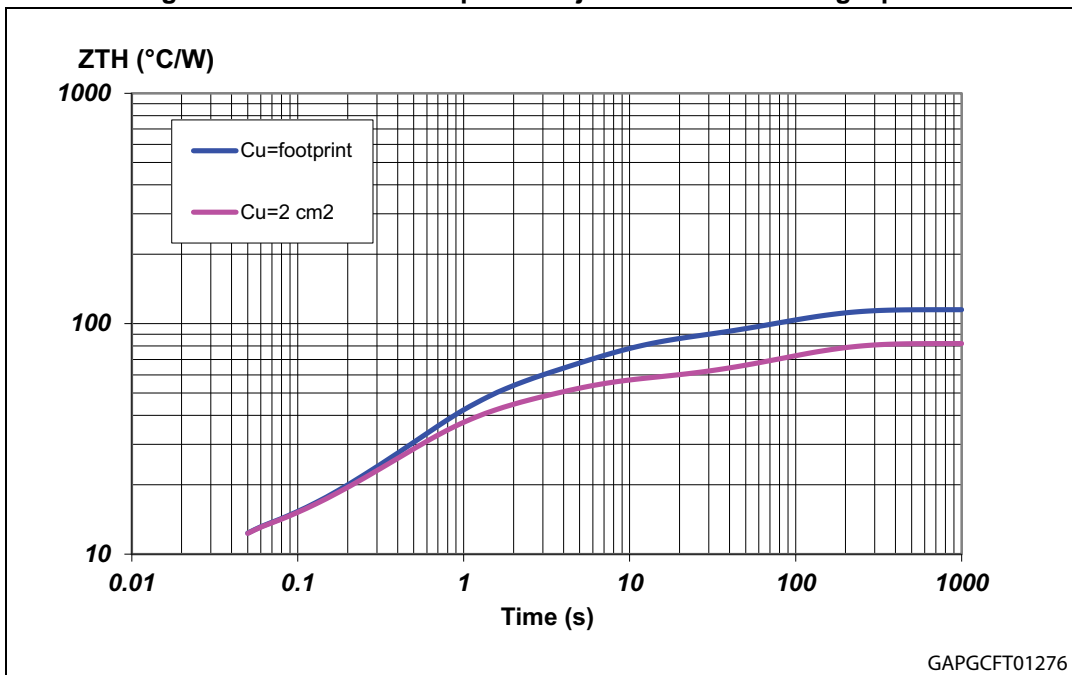


Figure 9. SO-8 thermal impedance junction ambient single pulse

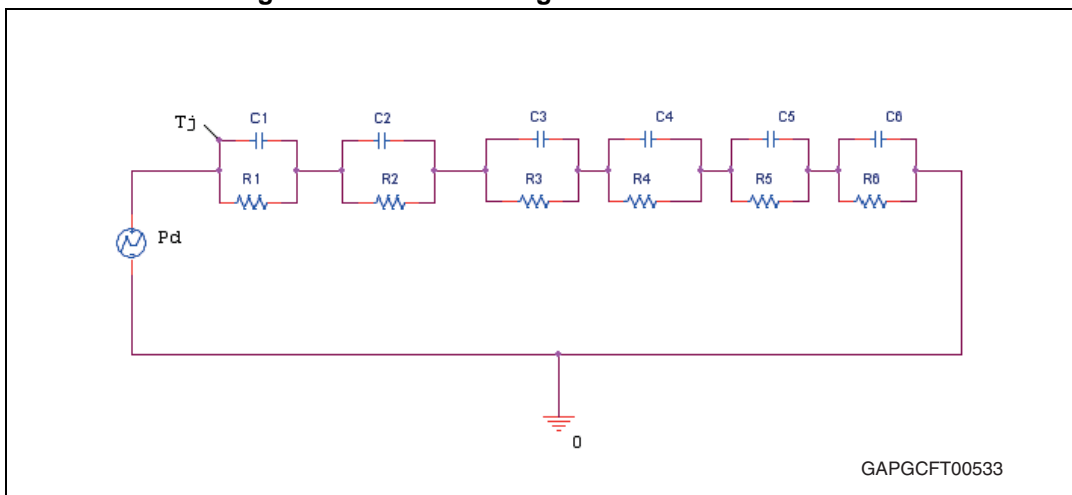


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 10. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. SO-8 thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	2.8	2.8
R2 (°C/W)	3.7	3.7
R3 (°C/W)	3.5	3.5
R4 (°C/W)	34	25
R5 (°C/W)	36	20
R6 (°C/W)	35	27
C1 (W.s/°C)	0.00002	0.00002
C2 (W.s/°C)	0.001	0.001
C3 (W.s/°C)	0.005	0.005
C4 (W.s/°C)	0.02	0.02
C5 (W.s/°C)	0.15	0.15
C6 (W.s/°C)	2.5	3.5



## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 SO-8 mechanical data

Figure 11. SO-8 package dimensions

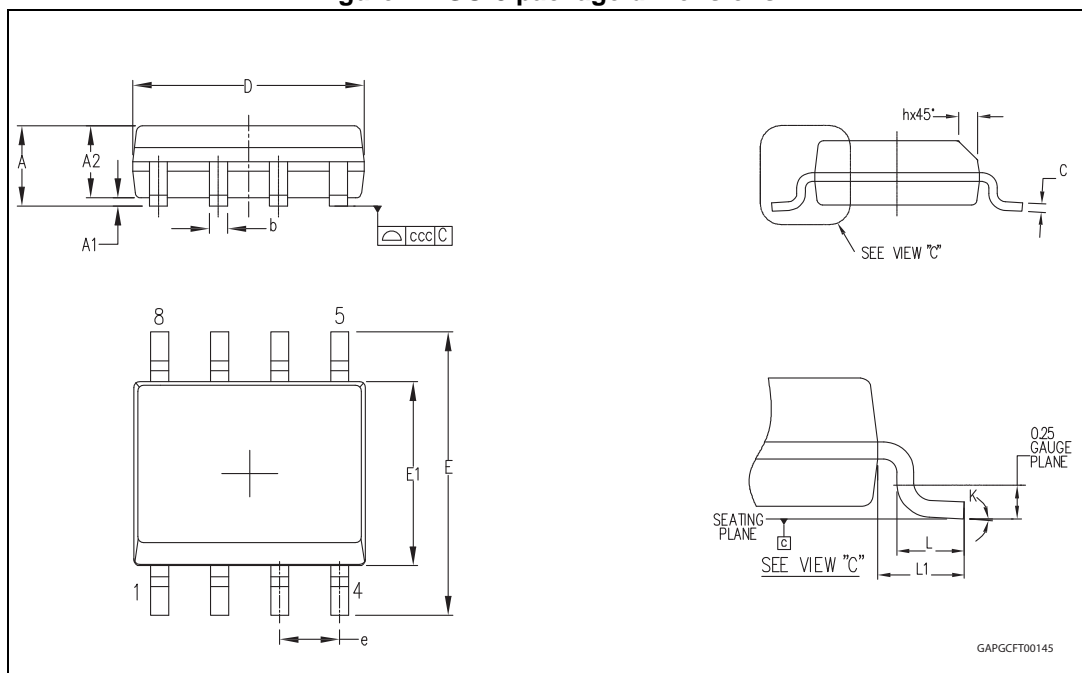


Table 16. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

### 5.3 SO-8 packing information

Figure 12. SO-8 tube shipment (no suffix)

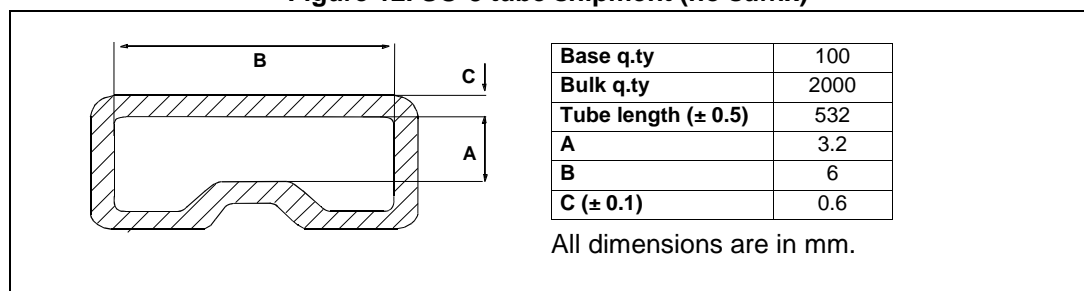
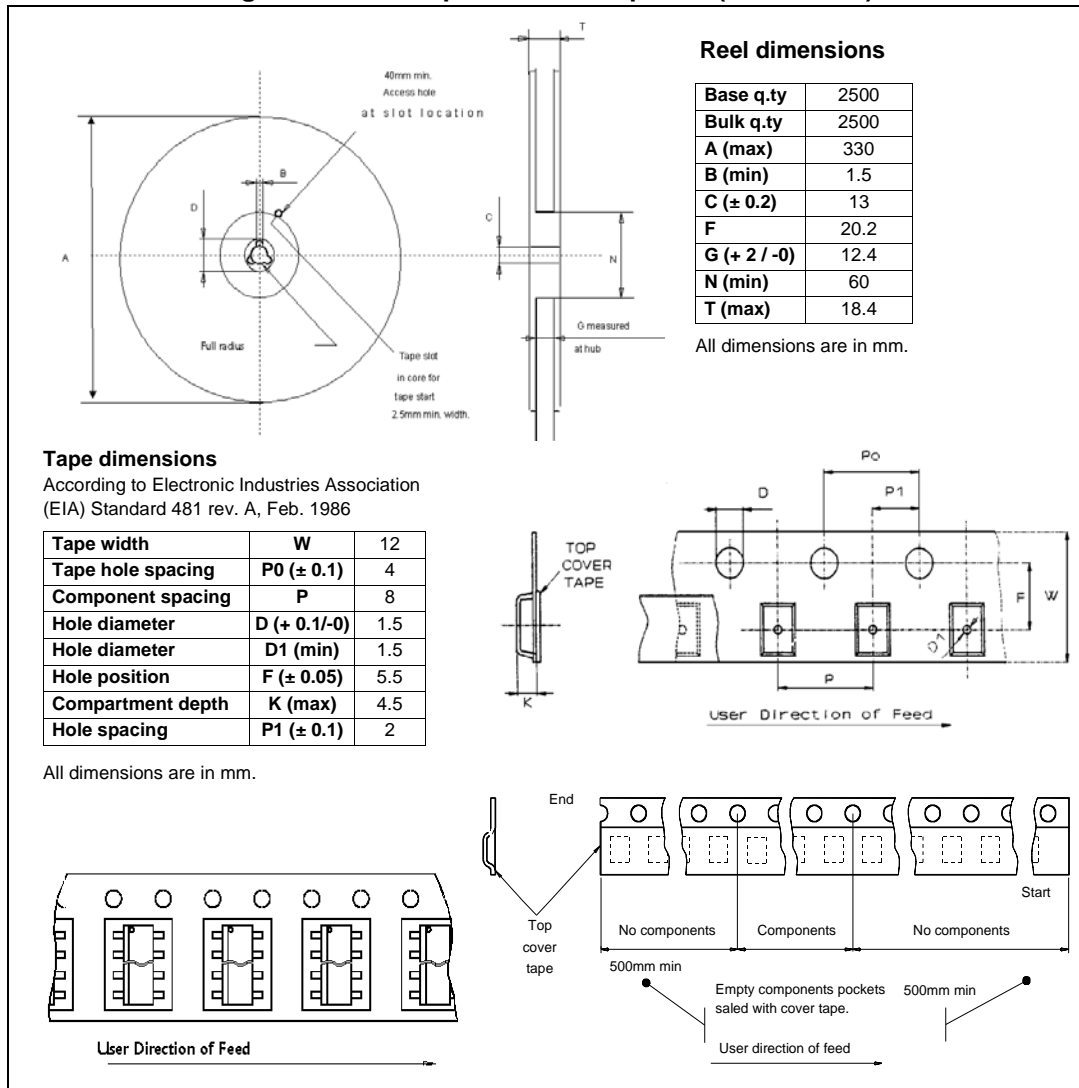


Figure 13. SO-8 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 17. Document revision history**

Date	Revision	Changes
02-Jul-2012	1	Initial release.
23-May-2013	2	<p><i>Table 5: Thermal data:</i></p> <ul style="list-style-type: none"> <li>- <math>R_{thj-amb}</math>: updated value</li> </ul> <p><i>Table 6: PowerMOS section:</i></p> <ul style="list-style-type: none"> <li>- <math>R_{ON}</math>: updated value</li> </ul> <p><i>Table 11: Supply section:</i></p> <ul style="list-style-type: none"> <li>- <math>I_S</math>: updated value</li> </ul> <p><i>Table 12: Switching characteristics:</i></p> <ul style="list-style-type: none"> <li>- <math>t_{d(ON)}</math>, <math>t_{d(OFF)}</math>, <math>t_r</math>, <math>W_{ON}</math>, <math>W_{OFF}</math>: updated values</li> </ul> <p><i>Table 13: Protection and diagnostics:</i></p> <ul style="list-style-type: none"> <li>- <math>t_{dlimL}</math>: updated value</li> </ul> <p>Updated <i>Figure 5: Application schematic</i></p> <p>Updated <i>Section 3.1: MCU I/O protection</i></p> <p>Updated <i>Chapter 4: Package and PC board thermal data</i></p>
18-Jul-2013	3	<p><i>Table 4: Absolute maximum ratings:</i></p> <ul style="list-style-type: none"> <li>- <math>-I_D</math>: updated value</li> <li>- <math>E_{AS}</math>: updated parameter value</li> </ul> <p><i>Table 12: Switching characteristics:</i></p> <ul style="list-style-type: none"> <li>- <math>t_{d(ON)}</math>, <math>t_r</math>, <math>W_{ON}</math>, <math>W_{OFF}</math>: updated typical values</li> </ul> <p>Added <i>Figure 6: Maximum demagnetization energy</i></p>
18-Sep-2013	4	Updated disclaimer.
13-Dec-2013	5	<p><i>Table 6: PowerMOS section:</i></p> <ul style="list-style-type: none"> <li>- <math>R_{ON}</math>: updated test conditions</li> </ul>

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