WPMDM1500602/ 171050601

MagI³C Power Module

VDRM - Variable Step Down Regulator Module

6-36V / 5A / 0.8-6V Output

DESCRIPTION

The VDRM series of the MagI³C Power Module family provide a fully integrated DC-DC power supply including the buck switching regulator and inductor in a package.

The WPMDH1200601 offers high efficiency and delivers up to 5A of output current. It operates from 6V input voltage up to 36V. It is designed for fast transient response.

It is available in an innovative industrial high power density TO263-7EP (10.16 x 13.77 x 4.57mm) package that enhances thermal performance and allows for hand or machine soldering.

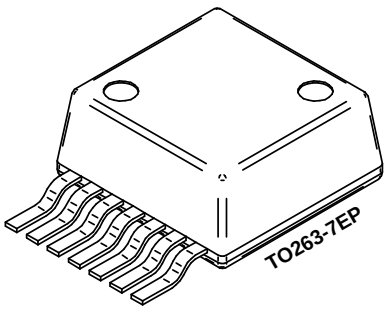
The VDRM regulators have an on-board protection circuitry to guard against thermal overstress and electrical damage featuring thermal shut-down, over-current, short-circuit, overvoltage and under-voltage protections.

FEATURES

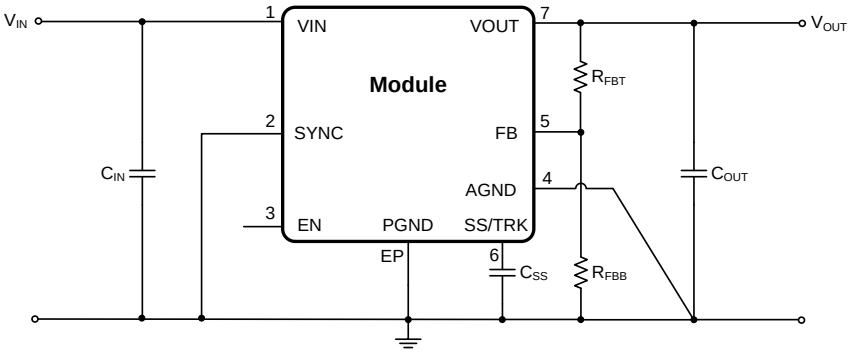
- Peak efficiency up to 92%
- Current capability up to 5A
- Wide input voltage range: 6V to 36V
- Output voltage range: 0.8V to 6V
- Maximum output power: 30W
- Integrated shielded inductor solution for quick time to market and ease of use
- Single exposed pad for best-in-class thermal performance
- Low output voltage ripple (< 10mV$_{PP}$)
- Under voltage lockout Protection (UVLO)
- Programmable soft-start and voltage tracking
- Frequency synchronization input
- Thermal shut down, inrush current and output short circuit protection
- Operating ambient temp. range up to 105°C
- Operating junction temp. range: -40 to 125°C
- RoHS & REACH compliant
- Mold compound UL 94 Class V0 (flammability testing) certified
- Complies with EN 55022 class B radiated and conducted emissions standard

TYPICAL APPLICATIONS

- Point-of-Load DC-DC applications from 12V and 24V industrial rails
- Industrial, Test & Measurement, Medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply



TYPICAL CIRCUIT DIAGRAM



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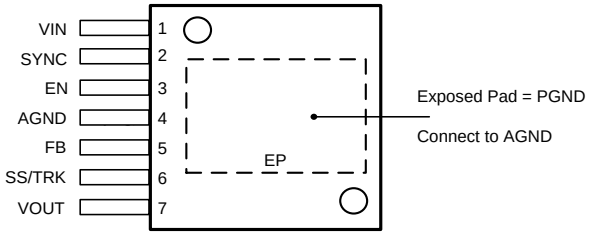
PACKAGE



PIN DESCRIPTION

PIN #	SYMBOL	TYPE	PIN DESCRIPTION
1	V_{IN}	Power	The supply input pin is a terminal for an unregulated input voltage source. It is required to place the input capacitor nearby the VIN pin and PGND.
2	SYNC	Input	The Sync Input pin allows to synchronize the PWM operating frequency to an external frequency source. Apply a CMOS logic level square wave with a frequency between 650 kHz and 950 kHz. When not using synchronization connect to ground. The module free running PWM frequency is 812kHz (typical).
3	EN	Input	The enable input pin is internally connected to the precision enable comparator and the rising threshold is at 1.18V. Maximum recommended input level is 6.5V.
4	AGND	Supply	The analog ground pin is the reference point for all stated voltages and must be connected to PGND.
5	FB	Input	The feedback pin is internally connected to the regulation circuitry, the over-voltage and short-circuit comparators. The regulation reference point is 0.796V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
6	SS/TRK	Input	The Soft-Start and Tracking pin is to extend the 1.6ms internal soft-start. Connect an external soft start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail.
7	V_{OUT}	Power	The output voltage pin is connected to the internal inductor. For the best stability and operation connect the output capacitor between this pin and PGND.
EP	PGND	Power	Exposed Pad – Main node for switch current of internal LS-MOSFET. Used as heat sink for power dissipation during operation. Must be electrically connected to pin 4.

ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	PACKAGE	PACKING UNIT
171050601	WPMDM1500602JT	TO263-7EP	Tape and Reel with 250 Units
178050601	WPMDM1500602JEV	Eval Board	evaluation board 1 Unit

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 79 42 945 - 0 www.we-online.com powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{IN}	Input Voltage to PGND	-0.3 to 40	V
EN, SYNC	Enable, Sync input to AGND	-0.3 to 5.5	V
SS/TRK, FB	Soft-start/Track, Feedback input to AGND	-0.3 to 2.5	V
AGND	AGND to PGND	-0.3 to 0.3	V
$V_{ESD-HBM}$	ESD, human body model (1)	-2000 to 2000	V
T_J	Junction temperature	150	°C
T_{ST}	Storage temperature	-65 to 150	°C
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 20sec (2) Maximum two cycles!	240 ±5°C	°C

OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

SYMBOL	PARAMETER	MIN (3)	TYP (4)	MAX (3)	UNIT
V_{IN}	Input voltage	6	-	36	V
V_{OUT}	Regulated output voltage	0.8		6	V
EN, SYNC	Enable, Sync input	0	-	5.0	V
T_A	Ambient temperature range	-40	-	note (5)	°C
T_J	Junction temperature range	-40	-	125	°C

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP	UNIT
θ_{JA}	Thermal resistance junction to ambient(6)	12	°C/W
θ_{JC}	Thermal resistance junction to case, no air flow	1.9	°C/W
T_{SD}	Thermal shut down, junction temperature, rising	165	°C
$T_{SD-HYST}$	Thermal shut down hysteresis, falling	15	°C

ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represent statistically the utmost probability at following conditions: V_{IN}=12V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
I_{OCP}	Over current protection		5.4	-	-	A
V_{EN}	EN threshold trip point	V_{EN} rising	1.10	1.279	1.458	V
I_{EN-HYS}	EN input current	V_{EN} > 1.279V	-	-21	-	µA
f_{SW}	Free-running oscillator frequency	Sync input connected to ground	711	812	914	kHz
f_{SYNC}	Synchronization range		650	-	950	kHz

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MIN and MAX limits are valid for the recommended junction temperature range of **-40°C to 125°C**. Typical values represent statistically the utmost probability at following conditions: V_{IN}=12V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
$V_{IL-SYNC}$	Synchronization logic zero amplitude	Relative to AGND	-	-	0.4	V
$V_{IH-SYNC}$	Synchronization logic zero amplitude	Relative to AGND	1.5	-	-	V
$SYNC_{d.c.}$	Synchronization duty cycle range		15	50	85	%
D_{max}	Maximum duty cycle		-	83	-	%
I_{SS}	Soft-start source current	V_{SS} = 0V	40	50	60	µA
tss	Internal soft-start time		-	1.6	-	ms
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V I_{OUT} = 5A	0.776	0.796	0.816	V
V_{FB-OVP}	Feedback over-voltage protection threshold		-	0.86	-	V
I_{FB}	Feedback input bias current		-	5	-	nA
I_Q	Non switching input current	V_{FB}= 0.86V	-	2.6	-	mA
I_{SD}	Shut down quiescent current	V_{EN}= 0V	-	70	-	µA
ΔV_{OUT}	Output voltage ripple	C_{OUT}=220µF 7mΩ ESR + 100µF X7R + 2x 0.047µF	-	9	-	mVpp
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{IN} = 12V to 36V I_{OUT}=1mA	-	±0.02	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 12V to 36V I_{OUT} = 1mA to 5A	-	1	-	mV/A
η	Efficiency	V_{IN}=12V, V_{OUT}=3.3V I_{OUT}=1A	-	86	-	%
η	Efficiency	V_{IN}=12V, V_{OUT}=3.3V I_{OUT}=5A	-	81.5	-	%
η	Efficiency	V_{IN}=24V, V_{OUT}=3.3V I_{OUT}=2A	-	80	-	%
η	Efficiency	V_{IN} = 24V, V_{OUT} = 3.3V I_{OUT} = 5A	-	76	-	%

NOTES

(1) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

(2) JEDEC J-STD020

(3) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(4) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(5) Depending on heat sink design, number of PCB layers, copper thickness and air flow.

(6) Measured on a 3.5” x 3.5” four layer board, with 104µm (3 ounce) copper on outer layers and 70µm (2 ounce) copper on inner layers, sixty 10 mil thermal vias, no air flow, and 1W power dissipation

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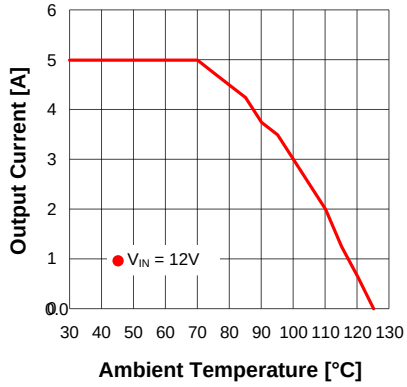
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 100µF X7R ceramic, T_{AMB} = 25°C

Thermal Derating: V_{OUT} = 3.3V @ θ_{JA} = 12°C/W



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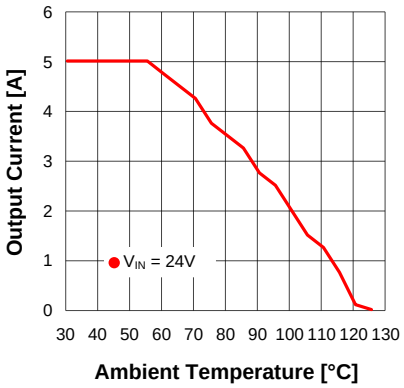
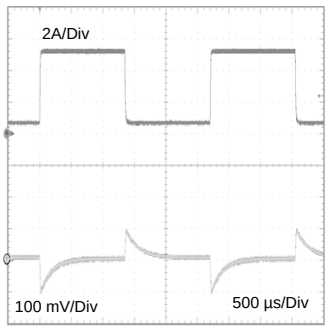
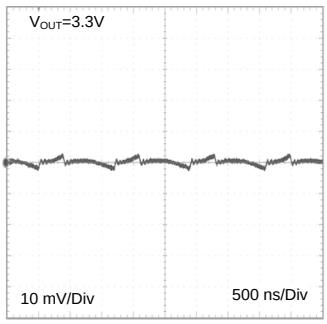


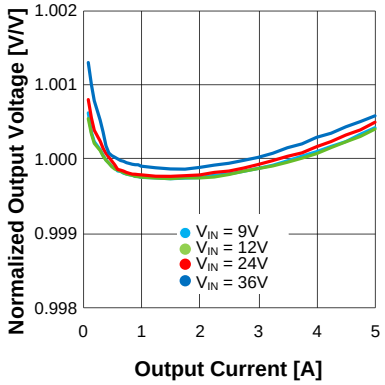
Transient response
V_{IN} = 12V, I_{OUT} = 0.5 to 5A Step



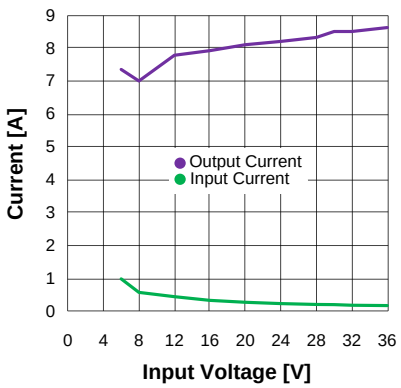
Output Ripple
V_{IN} = 12V, I_{OUT} = 5A, BW = 20MHz



Normalizied Line and Load V_{OUT} = 3.3V



Current Limit vs. Input Voltage



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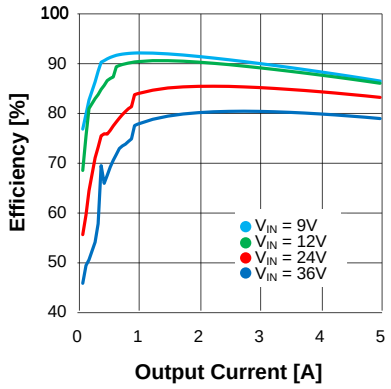
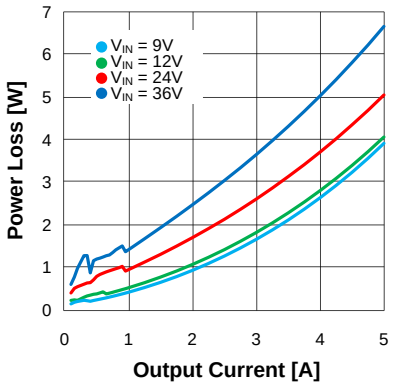
If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 100µF X7R ceramic, T_{AMB} = 25°C

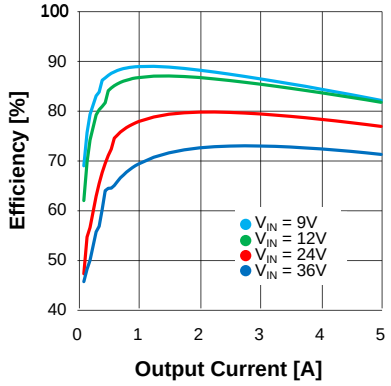
Efficiency: V_{OUT} = 5V @ T_{AMB} = 25°C



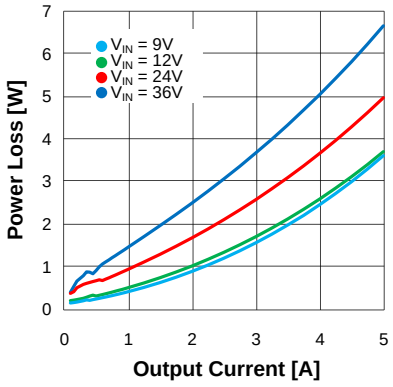
Power Loss: V_{OUT} = 5V @ T_{AMB} = 25°C



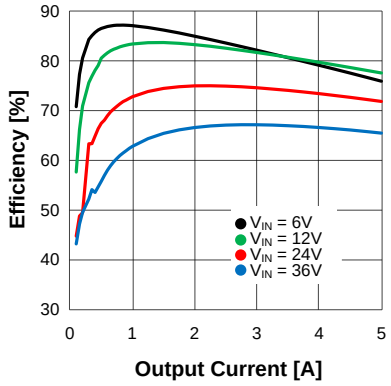
Efficiency: V_{OUT} = 3.3V @ T_{AMB} = 25°C



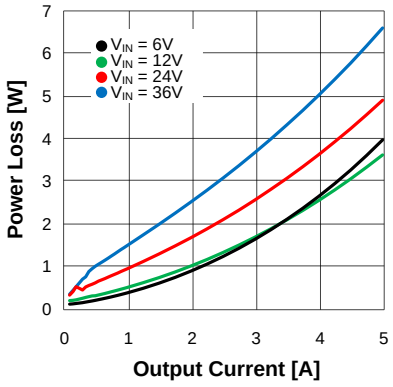
Power Loss: V_{OUT} = 3.3V @ T_{AMB} = 25°C



Efficiency: V_{OUT} = 2.5V @ T_{AMB} = 25°C



Power Loss: V_{OUT} = 2.5V @ T_{AMB} = 25°C



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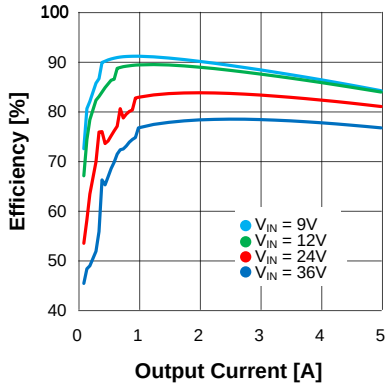
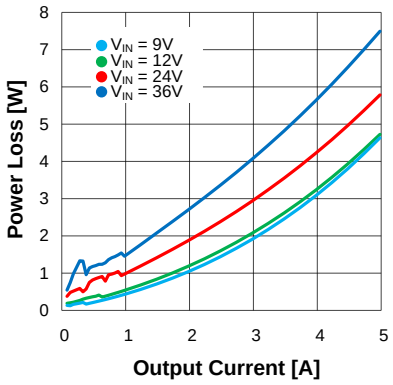
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 24V; C_{IN} = 10µF X7R ceramic; C_O = 100µF X7R ceramic, T_{AMB} = 25°C

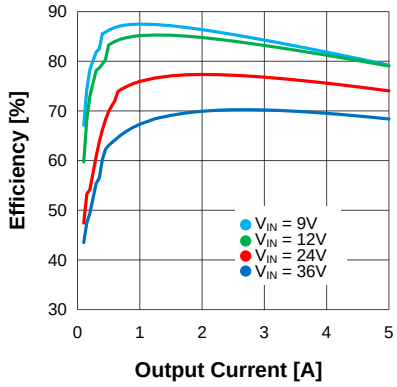
Efficiency: V_{OUT} = 5V @ T_{AMB} = 85°C



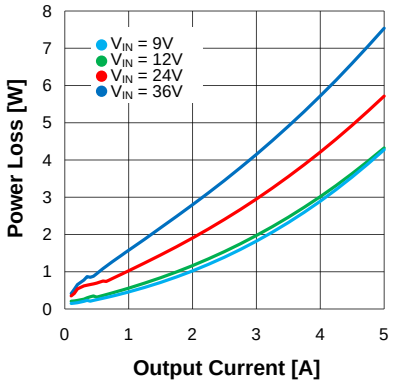
Power Loss: V_{OUT} = 5V @ T_{AMB} = 85°C



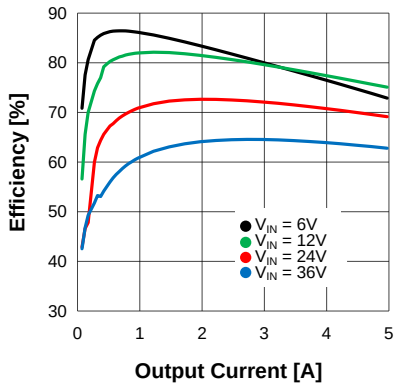
Efficiency: V_{OUT} = 3.3V @ T_{AMB} = 85°C



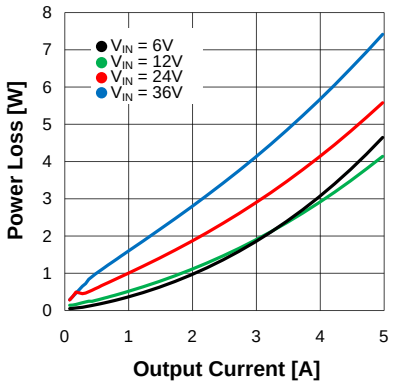
Power Loss: V_{OUT} = 3.3V @ T_{AMB} = 85°C



Efficiency: V_{OUT} = 2.5V @ T_{AMB} = 85°C



Power Loss: V_{OUT} = 2.5V @ T_{AMB} = 85°C



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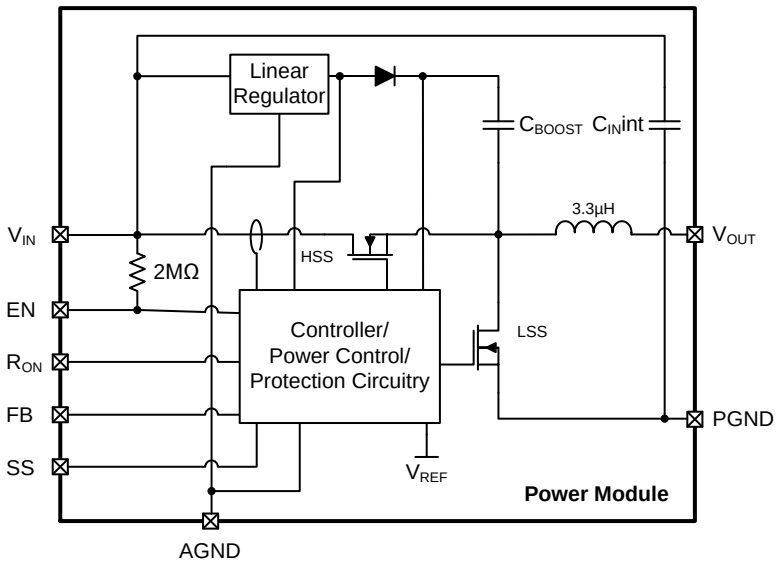
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module WPMDH1200601 is based on a synchronous step down regulator with integrated MOSFET and a power inductor. The control scheme is based on a Current Mode (CM) regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network R_{FBT} and R_{FBB} and fed into the FB pin. The error amplifier compares this signal with the internal 0.796V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse with generator. This signal drives the power mosfets.

The Current Mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output ripple values of 10ths of millivolts are achieved.

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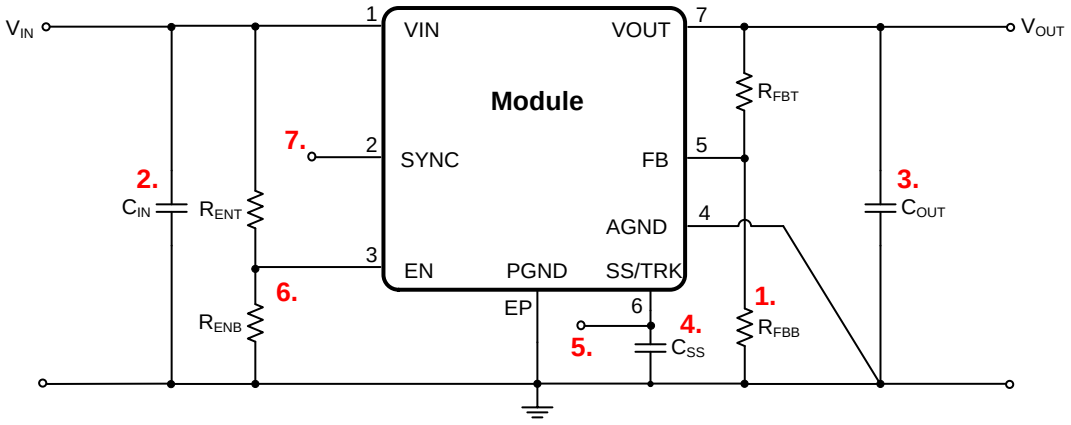
DESIGN FLOW

4 Steps (plus 3 Optional) to design the power application

The next 7 simple steps will show how to select the external components to design your power application:

1. **Program output voltage**
2. **Select input capacitor**
3. **Select output capacitor**
4. **Select soft-start capacitor**

5. **Optional: Voltage tracking**
6. **Optional: Program under voltage lockout divider**
7. **Optional: Synchronization to an external clock**



Step 1. Select Output Voltage (V_{OUT})
Output voltage is determined by a divider of two resistors connected between V_{OUT} and ground. The midpoint of the divider is connected to the FB input.
The ratio of the feedback resistors for a desired output voltage is:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{V_{OUT}}{0.796V}\right) - 1 \qquad (1)$$

These resistors should be chosen from values in the range of 1kΩ to 10kΩ.
For V_{OUT} = 0.8V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06kΩ to provide minimum output load. A table of values for R_{FBT} and R_{FBB}, is included in the applications circuit.

Step 2. Select Input Capacitor (C_{IN})
The MagI³C power module contains a small amount of internal ceramic input capacitors. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance should be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \approxeq \frac{1}{2} * I_{OUT} * \sqrt{(D / 1 - D)} \qquad (2)$$

where $D \approxeq \frac{V_{OUT}}{V_{IN}}$

DESIGN FLOW

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when V_{IN} = 2 * V_{OUT}).
Recommended minimum input capacitance is 22µF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature derating of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.
If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} * D * (1-D)}{f_{SW-CCM} * \Delta V_{IN}} \qquad (3)$$

If ΔV_{IN} is 1% of V_{IN} for a 12V input to 3.3V output application this equals 120 mV and f_{SW} = 812kHz.

$$C_{IN} \geq \frac{5A * \frac{3.3V}{12V} * (1-\frac{3.3V}{12V})}{812000 * 0.120V}$$

$$C_{IN} \geq 10.2\mu F$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The MagI³C power module typical applications schematic and evaluation board include a 150µF 50V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

Step 3. Select Output Capacitor (C_{OUT})
None of the required C_{OUT} output capacitance is contained within the module. A minimum value of 200 µF is required based on the values of internal compensation in the error amplifier. Low ESR tantalum, organic semiconductor or specialty polymer capacitor types are recommended for obtaining lowest ripple. The output capacitor C_{OUT} may consist of several capacitors in parallel placed in close proximity to the module. The output capacitor assembly must also meet the worst case minimum ripple current rating of 0.5 * $I_{LR\ P-P}$, as calculated in equation (4) below.

$$I_{LR\ P-P} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{3.3\mu H * f_{SW} * V_{IN}} \qquad (4)$$

Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. Loop response verification is also valuable to confirm closed loop behavior. For applications with dynamic load steps; the following equation provides a good first pass approximation of C_{OUT} for load transient requirements:

$$C_{OUT} \geq \frac{I_{STEP} * V_{OUT}}{(V_{OUT-TRAN} - ESR \cdot I_{STEP}) * f_{SW}} \qquad (5)$$

For example:
$I_{STEP} = 4.5A, V_{OUT} = 3.3V, V_{OUT-TRAN} = 100mV$

$$C_{OUT} \geq \frac{4.5A * 3.3V}{(0.1V - 0.007 * 4.5) * 800000}$$

$$C_{OUT} \geq 271\mu F$$

DESIGN FLOW

Note that the stability requirement for 200µF minimum output capacitance will take precedence.
One recommended output capacitor combination is a 220uF, 7 milliohm ESR specialty polymer cap in parallel with a 100µF 6.3V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small ceramic capacitors can be used for high frequency EMI suppression.

Step 4. Select Soft-Start Capacitor (C_{SS})
Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.
Upon turn-on, after all UVLO conditions have been passed, an internal 1.6ms circuit slowly ramps the SS/TRK input to implement internal soft start. If 2ms is an adequate turn–on time then the Css capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.
Soft start duration is given by the formula:

$$C_{SS} = t_{SS} * \frac{50\mu A}{0.796V} \quad (6)$$

with t_{ss} = select soft-start time in (ms)

Using a 0.22µF capacitor results in 3.5ms typical soft-start duration; and 0.47µF results in 7.5ms typical. 0.47µF is a recommended initial value. As the soft-start input exceeds 0.796V the output of the power stage will be in regulation and the 50µA current is deactivated. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The enable input being “pulled low”
- Thermal shutdown condition
- Internal V_{CC} UVLO (Approx 4.3V input to V_{IN})

Step 5. Optional: Voltage tracking
The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (i.e.<0.15V typ). The values for the tracking resistive divider should be selected such that the effect of the internal 50uA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy satisfy since the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.8V the input is no longer enabled and the 50 µA internal current source is switched off.

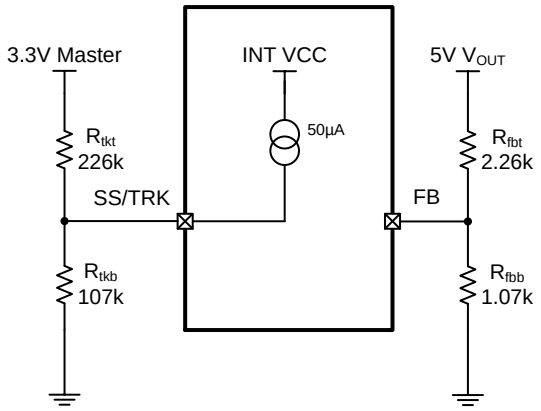


Figure 2. Tracking option input detail

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DESIGN FLOW

Step 6. Optional: Program under voltage lockout divider

Internal to the module is a 2MΩ pull-up resistor connected from V_{IN} to Enable. For applications not requiring precision under voltage lock out (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3V ($V_{IN\ rising}$).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail. Enable provides a precise 1.279V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 21µA (typ) of switched offset current allowing programmable hysteresis. See Figure 1.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable UVLO. The two resistors should be chosen based on the following ratio:

$$\frac{R_{ENT}}{R_{ENB}} = \left(\frac{V_{UVLO}}{1.279V}\right) - 1 \qquad (7)$$

The MagI³C power module typical application shows 12.7kΩ for R_{ENB} and 42.2kΩ for R_{ENT} resulting in a rising UVLO of 5.46V. Note that this divider presents 8.33V to the input when the divider is raised to 36V which would exceed the recommended 5.5V limit for Enable. A midpoint 5.1V zener clamp is applied to allow the application to cover the full 6V to 36V range of operation. The zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded. Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It is possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design. Rising threshold can be calculated as follows:

$$V_{EN}(rising) = 1.279\left(1 + \frac{(R_{ENT} \| 2M\Omega)}{R_{ENB}}\right) \qquad (8)$$

Whereas the falling threshold level can be calculated using:

$$V_{EN}(falling) = V_{EN}(rising) - 21\mu A * (R_{ENT} \| 2M\Omega \| R_{ENTB} + R_{ENH}) \qquad (9)$$

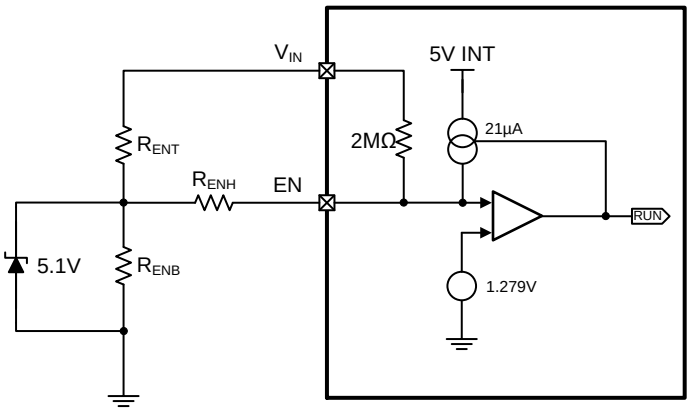


Figure 1. Enable input detail

DESIGN FLOW

Step 7. Optional: Synchronization to an external clock

The PWM switching frequency can be synchronized to an external frequency source. If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor of 1.5kΩ ohm or less. The allowed synchronization frequency range is 650kHz to 950 kHz. The typical input threshold is 1.4V transition level. Ideally the input clock should overdrive the threshold by a factor of 2, so direct drive from 3.3V logic via a 1.5kΩ source resistance is recommended. Note that applying a sustained “logic 1” corresponds to zero hertz PWM frequency and will cause the module to stop switching.

Determine power losses and thermal requirements of the board

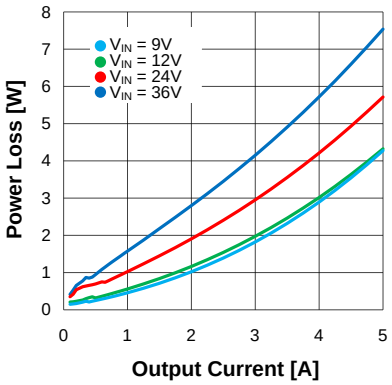
For example:
$V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 5A, T_{AMB(MAX)} = 85°C,$
the device must see a maximum junction-to-ambient thermal resistance of:

$$\theta_{CA} < \frac{(T_{J-MAX} - T_{AMB(MAX)})}{P_{IC-Loss}} - \theta_{JC} \qquad (10)$$

Given the typical thermal resistance from junction to case to be 1.9°C/W. Use the 85°C power dissipation curves in the typical performance characteristics section to estimate the $P_{IC-LOSS}$ for the application being designed. In this application it is 5.5W.

$$\theta_{CA} = \frac{(125°C - 85°C)}{5.5W} - 1.9°\frac{C}{W} = 5.37°C/W$$

Power Loss: V_{OUT} = 3.3V @ T_{AMB} = 85°C



To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to the following package thermal resistance graph. This graph is taken from the typical performance characteristics section and shows how the θ_{JA} varies with the PCB area.

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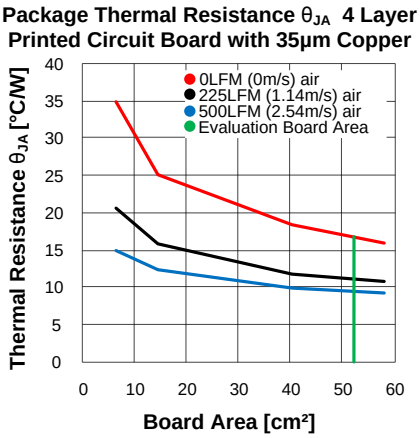
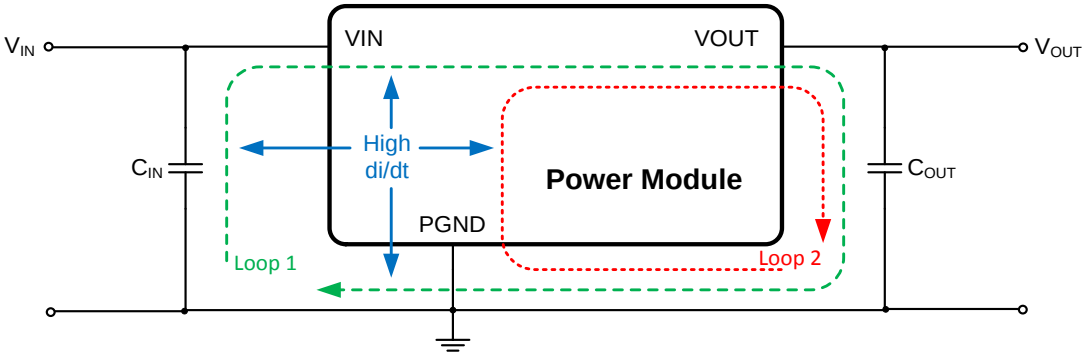


For $\theta_{CA} < 5.37°C/W$ and only natural convection (i.e. no air flow), the PCB area can be smaller than 18cm^2. This corresponds to a square board with 3cm x 3cm copper area, 4 layers, and 35µm copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

PCB Layout Instructions:

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following five simple design rules.

1: Minimize area of switched current loops.



Target is to identify the paths in the system which have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop1 is the current path during the ON-time of the High-Side Mosfet. Loop2 is the current path during the OFF-time of the High-Side Mosfet.

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MagI³C Power Module

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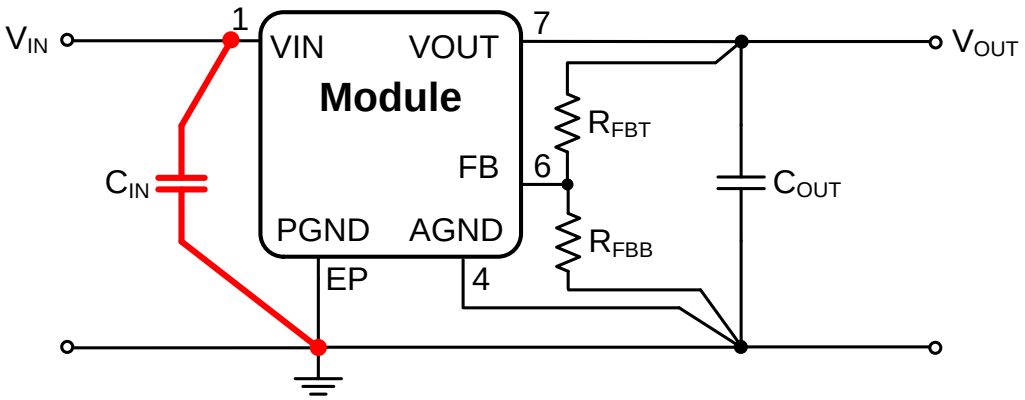
DESIGN FLOW



Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on Vin. Therefore place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND exposed pad EP. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad.

2: Have a single point ground.
The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.

Provide the single point ground connection from AGND pin 4 to the GND terminal of the output capacitor. This is the point of lowest noise.

3: Minimize trace length to the FB pin.
The feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the MagI³C power module to minimize noise pickup.

4: Make input and output bus connections as wide as possible.
This reduces any voltage drops on the input or output of the converter and maximizes efficiency.

5: Provide adequate device heat-sinking.
Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be used to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 254µm thermal vias spaced 1.5mm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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PROTECTIVE FEATURES

Output Over-voltage protection (OVP)

The voltage at FB is compared to a 0.92V internal reference. If FB rises above 0.92V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

Over current protection (OCP)

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below I_{CL}. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL}, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that DC current limit varies with duty cycle, switching frequency, and temperature.

Over temperature protection (OTP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165°C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145°C (typ Hyst = 20°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.
Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

Zero coil current detection (ZCCT)

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

Output under-voltage protection (UVP)

The MagI³C power module will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The pre-bias level of the output voltage must be less than the input UVLO set point. This will prevent the output pre-bias from enabling the regulator through the high side MOSFET body diode.

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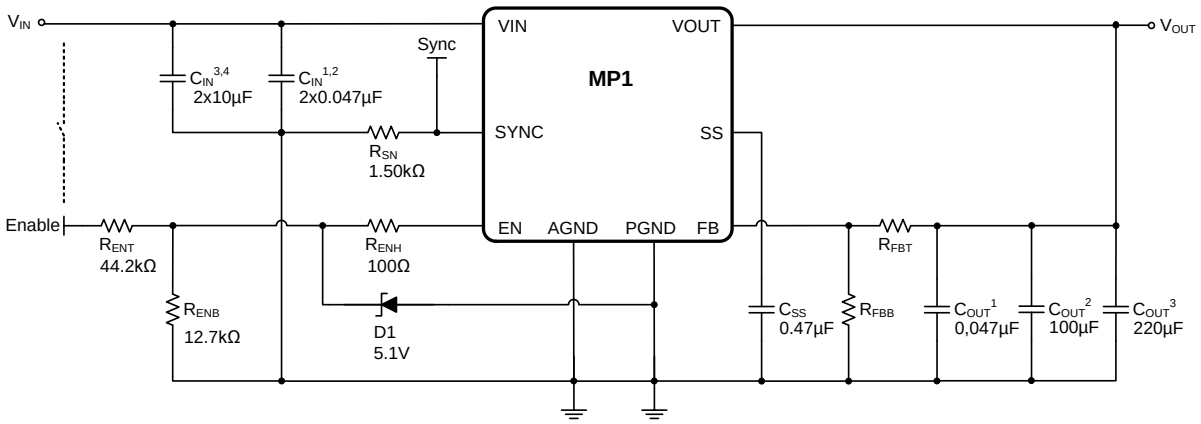
APPLICATIONS

The MagI³C power module for high output voltage is an easy-to-use DC-DC solution capable of driving up to a 5A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. It is available in an innovative package that enhances thermal performance and allows hand or machine soldering. Following application circuits show possible operating configurations.

Application Circuit



Bill of Materials for Design Example 1:

Recommended component values specified at T_A = 25°C

Ref Designator	Description	Case Size	Part
MP1	MagI³C Power Module	TO263-7EP	WE MagI³C Power Module
$C_{IN}^{1,2}$, C_{OUT}^{1}	0,047µF, 50V, X7R, ±10%	1206	Capacitor
$C_{IN}^{3,4}$	10µF, 50V, X5R, ±20%	1210	Capacitor
C_{OUT}^{2}	100µF, 6,3V, X5R, ±20%	1210	Capacitor
C_{OUT}^{3}	220µF, 6,3V, Polymer-Cap, ±20%	7343	Capacitor
C_{SS}	0.47µF, 16V, X7R, ±10%	0805	Capacitor
R_{ENB}	11.8kΩ, ±1%	0805	Resistor
R_{ENT}	68.1kΩ, ±1%	0805	Resistor
R_{FBT}	3.32kΩ, ±1%	0805	Resistor
R_{FBB}	1.07kΩ, ±1%	0805	Resistor
R_{ON}	61.9kΩ, ±1%	0805	Resistor

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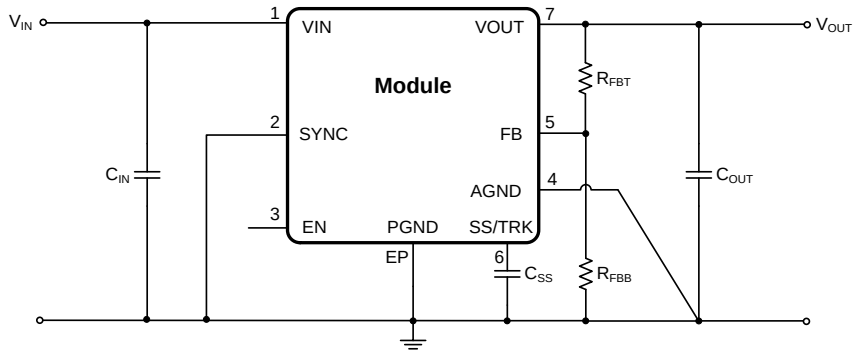
Application Circuit



Bill of Materials for Design Example 2:

Recommended component values: T_A = 25°C, I_{OUT} = 2A

V_{out}	5V	3.3V	2.5V	1.8V	1.5V	1.2V
R_{FBT}	5.62kΩ	3.32kΩ	2.26kΩ	1.87kΩ	1.00kΩ	1.07kΩ
R_{FBB}	1.07kΩ	1.07kΩ	1.07kΩ	1.5kΩ	1.13kΩ	2.05kΩ
C_{IN}	22µF					
C_{OUT}	220µF					
C_{SS}	0.47µF					
V_{IN}	9-36V	7-36V	6-36V	6-36V	6-36V	6-36V

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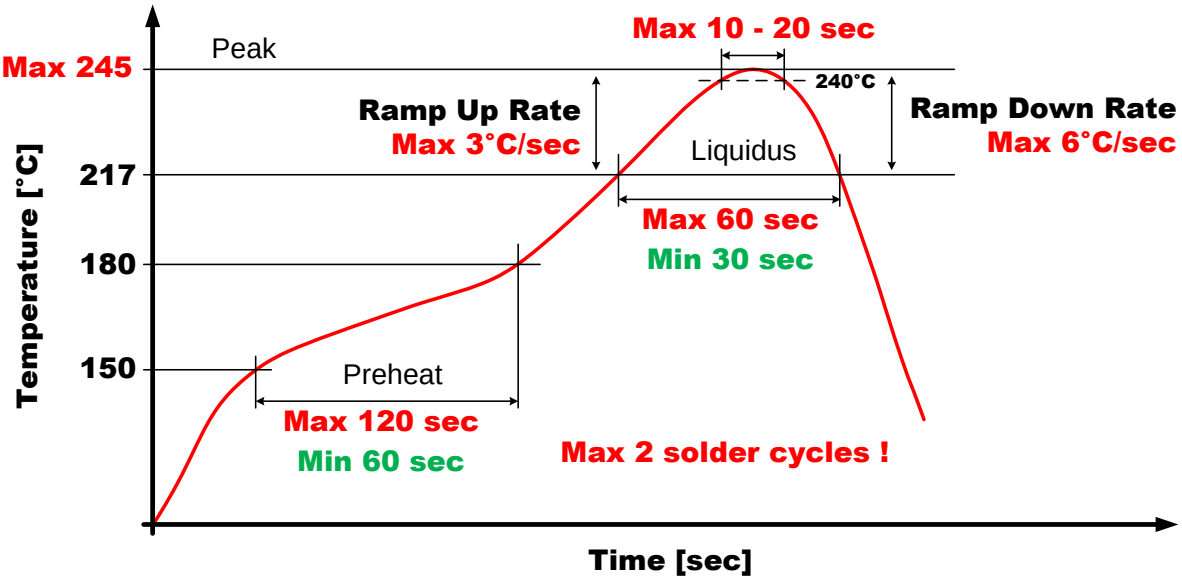
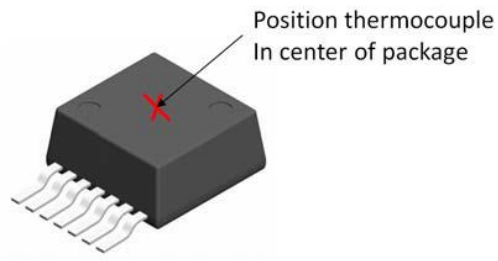
HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card .
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 240°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 240°C ±5°C must not exceed 20 seconds.
5. Reflow time above liquidus (217°C) must not exceed 60 seconds.
6. Maximum ramp up is rate 3°C per second
7. Maximum ramp down rate is 6°C per second
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is two**.
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk





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MagI³C Power Module

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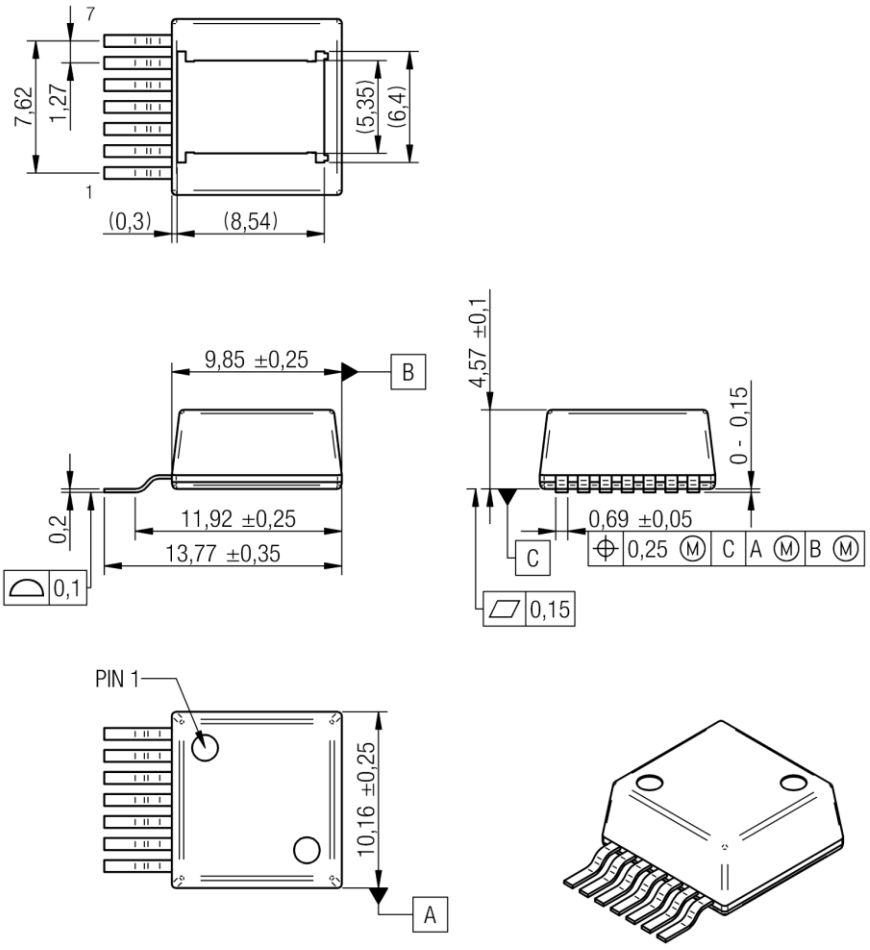
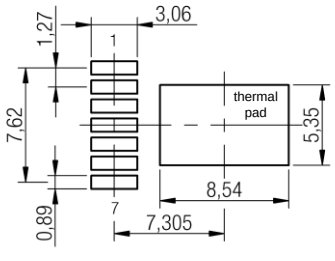
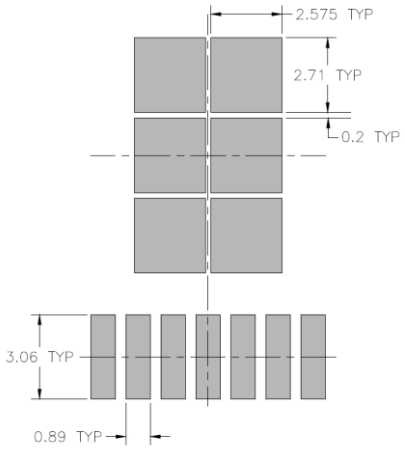
PHYSICAL DIMENSIONS (mm)

Package Type: TO263-7





recommended soldering pad



recommended stencil design
solder paste recommendation 150µm

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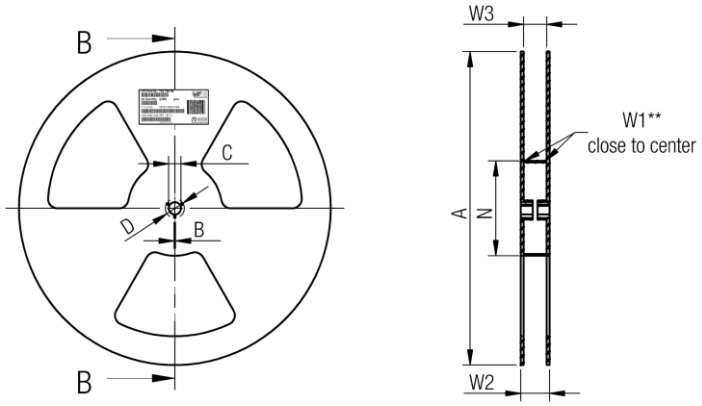
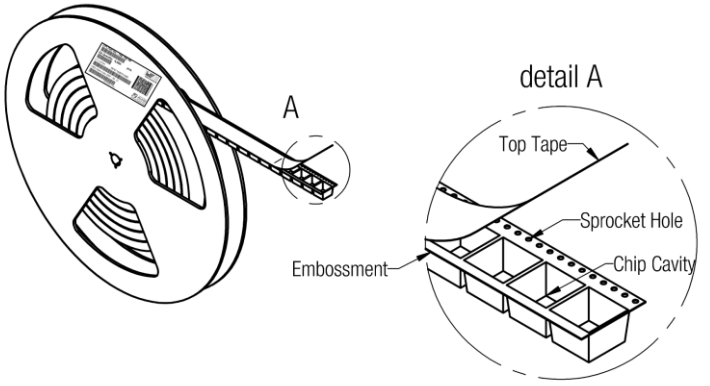
PACKAGING

Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40



20P

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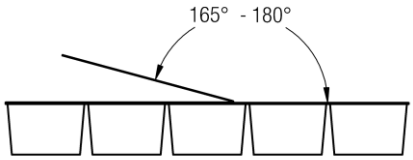
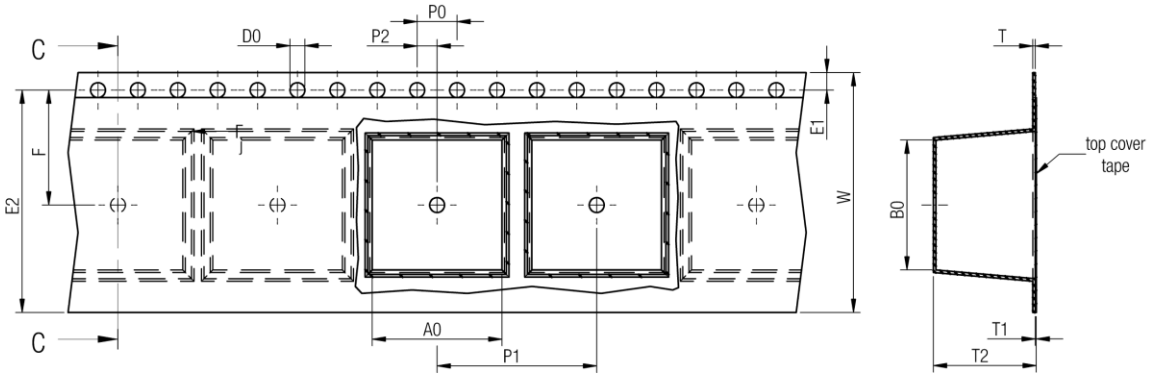
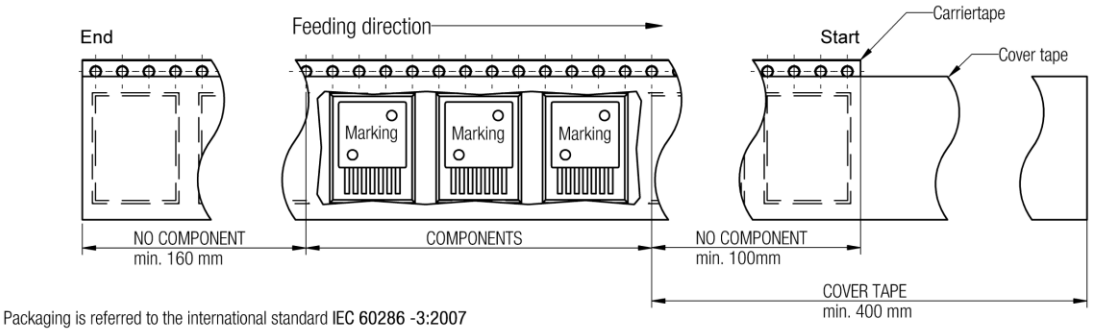
Tape (mm)



		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,3 -0,1	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	TO263-7EP	10,60	14,22	24,00	16,00	0,50	0,10	5,00	1,50	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

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DOCUMENT HISTORY

Revision	Date	Description	Page
1.0	10.03.2015	Release of final version	

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MagI³C Power Module
VDRM - Variable Step Down Regulator Module

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

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IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.