4-Output Quad DSPLL Any-Frequency Jitter Attenuating Clock Multiplier

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Overview
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Part:          Si5347CD
Design ID:     5347DBP1
Created By:    ClockBuilder Pro v2.0.2 [2015-06-22]
Timestamp:     2015-06-22 09:22:13 GMT-05:00

Device Grade
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Device      Output Clock
Grade       Frequency Range       Typical Jitter
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Si5347C     100 Hz to 710.4 MHz   < 150 fs
Si5347D*    100 Hz to 350 MHz     "

* Device Grade

Design
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Host Interface:
   I/O Power Supply: VDD (Core)
   SPI Mode: 4-Wire
   I2C Address Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)

XA/XB:
   48 MHz (XTAL - Crystal)

Inputs:
    IN0: Unused
    IN1: Unused
    IN2: Unused
    IN3: Unused

Outputs:
   OUT0: Unused
   OUT1: Unused
   OUT2: Unused
   OUT3: Unused

Frequency Plan
==============
No plan

Settings
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Location      Setting Name              Decimal Value  Hex Value
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0x000B[0:6]   I2C_ADDR                  108            0x6C
0x0016[0]     LOL_ON_HOLD_PLLA          1              0x1
0x0016[1]     LOL_ON_HOLD_PLLB          1              0x1
0x0016[2]     LOL_ON_HOLD_PLLC          1              0x1
0x0016[3]     LOL_ON_HOLD_PLLD          1              0x1
0x0017[0]     SYSINCAL_INTR_MSK         0              0x0
0x0017[1]     LOSXAXB_INTR_MSK          0              0x0
0x0017[5]     SMB_TMOUT_INTR_MSK        0              0x0
0x0018[0:3]   LOS_INTR_MSK              15             0xF
0x0018[4:7]   OOF_INTR_MSK              15             0xF
0x0019[0]     LOL_INTR_MSK_PLLA         1              0x1
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0x0019[1]	LOL_INTR_MSK_PLLB	1	0x1
0x0019[2]	LOL_INTR_MSK_PLLC	1	0x1
0x0019[3]	LOL_INTR_MSK_PLLD	1	0x1
0x0019[4]	HOLD_INTR_MSK_PLLA	1	0x1
0x0019[5]	HOLD_INTR_MSK_PLLB	1	0x1
0x0019[6]	HOLD_INTR_MSK_PLLC	1	0x1
0x0019[7]	HOLD_INTR_MSK_PLLD	1	0x1
0x001A[4]	CAL_INTR_MSK_PLLA	1	0x1
0x001A[5]	CAL_INTR_MSK_PLLB	1	0x1
0x001A[6]	CAL_INTR_MSK_PLLC	1	0x1
0x001A[7]	CAL_INTR_MSK_PLLD	1	0x1
0x002B[3]	SPI_3WIRE	0	0x0
0x002C[0:3]	LOS_EN	0	0x0
0x002C[4]	LOSXAXB_DIS	0	0x0
0x002D[0:1]	LOS0_VAL_TIME	0	0x0
0x002D[2:3]	LOS1_VAL_TIME	0	0x0
0x002D[4:5]	LOS2_VAL_TIME	0	0x0
0x002D[6:7]	LOS3_VAL_TIME	0	0x0
0x002E[0:15]	LOS0_TRG_THR	0	0x0000
0x0030[0:15]	LOS1_TRG_THR	0	0x0000
0x0032[0:15]	LOS2_TRG_THR	0	0x0000
0x0034[0:15]	LOS3_TRG_THR	0	0x0000
0x0036[0:15]	LOS0_CLR_THR	0	0x0000
0x0038[0:15]	LOS1_CLR_THR	0	0x0000
0x003A[0:15]	LOS2_CLR_THR	0	0x0000
0x003C[0:15]	LOS3_CLR_THR	0	0x0000
0x003F[0:3]	OOF_EN	0	0x0
0x003F[4:7]	FAST_OOF_EN	0	0x0
0x0040[0:2]	OOF_REF_SEL	4	0x4
0x0041[0:4]	OOF0_DIV_SEL	0	0x00
0x0042[0:4]	OOF1_DIV_SEL	0	0x00
0x0043[0:4]	OOF2_DIV_SEL	0	0x00
0x0044[0:4]	OOF3_DIV_SEL	0	0x00
0x0045[0:4]	OOFXO_DIV_SEL	12	0x0C
0x0046[0:7]	OOF0_SET_THR	0	0x00
0x0047[0:7]	OOF1_SET_THR	0	0x00
0x0048[0:7]	OOF2_SET_THR	0	0x00
0x0049[0:7]	OOF3_SET_THR	0	0x00
0x004A[0:7]	OOF0_CLR_THR	0	0x00
0x004B[0:7]	OOF1_CLR_THR	0	0x00
0x004C[0:7]	OOF2_CLR_THR	0	0x00
0x004D[0:7]	OOF3_CLR_THR	0	0x00
0x004E[0:2]	OOF0_DETWIN_SEL	0	0x0
0x004E[4:6]	OOF1_DETWIN_SEL	0	0x0
0x004F[0:2]	OOF2_DETWIN_SEL	0	0x0
0x004F[4:6]	OOF3_DETWIN_SEL	0	0x0
0x0051[0:3]	FAST_OOF0_SET_THR	0	0x0
0x0052[0:3]	FAST_OOF1_SET_THR	0	0x0
0x0053[0:3]	FAST_OOF2_SET_THR	0	0x0
0x0054[0:3]	FAST_OOF3_SET_THR	0	0x0
0x0055[0:3]	FAST_OOF0_CLR_THR	0	0x0
0x0056[0:3]	FAST_OOF1_CLR_THR	0	0x0
0x0057[0:3]	FAST_OOF2_CLR_THR	0	0x0
0x0058[0:3]	FAST_OOF3_CLR_THR	0	0x0
0x0059[0:1]	FAST_OOF0_DETWIN_SEL	0	0x0
0x0059[2:3]	FAST_OOF1_DETWIN_SEL	0	0x0
0x0059[4:5]	FAST_OOF2_DETWIN_SEL	0	0x0
0x0059[6:7]	FAST_OOF3_DETWIN_SEL	0	0x0
0x005A[0:25]	OOF0_RATIO_REF	0	0x0000000
0x005E[0:25]	OOF1_RATIO_REF	0	0x0000000
0x0062[0:25]	OOF2_RATIO_REF	0	0x0000000
0x0066[0:25]	OOF3_RATIO_REF	0	0x0000000
0x0092[0]	LOL_FST_EN_PLLA	0	0x0
0x0092[1]	LOL_FST_EN_PLLB	0	0x0

0x0092[2]	LOL_FST_EN_PLLC	0	0x0
0x0092[3]	LOL_FST_EN_PLLD	0	0x0
0x0093[0:3]	LOL_FST_DETWIN_SEL_PLLA	0	0x0
0x0093[4:7]	LOL_FST_DETWIN_SEL_PLLB	0	0x0
0x0094[0:3]	LOL_FST_DETWIN_SEL_PLLC	0	0x0
0x0094[4:7]	LOL_FST_DETWIN_SEL_PLLD	0	0x0
0x0095[0:1]	LOL_FST_VALWIN_SEL_PLLA	0	0x0
0x0095[2:3]	LOL_FST_VALWIN_SEL_PLLB	0	0x0
0x0095[4:5]	LOL_FST_VALWIN_SEL_PLLC	0	0x0
0x0095[6:7]	LOL_FST_VALWIN_SEL_PLLD	0	0x0
0x0096[0:3]	LOL_FST_SET_THR_SEL_PLLA	0	0x0
0x0096[4:7]	LOL_FST_SET_THR_SEL_PLLB	0	0x0
0x0097[0:3]	LOL_FST_SET_THR_SEL_PLLC	0	0x0
0x0097[4:7]	LOL_FST_SET_THR_SEL_PLLD	0	0x0
0x0098[0:3]	LOL_FST_CLR_THR_SEL_PLLA	0	0x0
0x0098[4:7]	LOL_FST_CLR_THR_SEL_PLLB	0	0x0
0x0099[0:3]	LOL_FST_CLR_THR_SEL_PLLC	0	0x0
0x0099[4:7]	LOL_FST_CLR_THR_SEL_PLLD	0	0x0
0x009A[0]	LOL_SLOW_EN_PLLA	0	0x0
0x009A[1]	LOL_SLOW_EN_PLLB	0	0x0
0x009A[2]	LOL_SLOW_EN_PLLC	0	0x0
0x009A[3]	LOL_SLOW_EN_PLLD	0	0x0
0x009B[0:3]	LOL_SLW_DETWIN_SEL_PLLA	0	0x0
0x009B[4:7]	LOL_SLW_DETWIN_SEL_PLLB	0	0x0
0x009C[0:3]	LOL_SLW_DETWIN_SEL_PLLC	0	0x0
0x009C[4:7]	LOL_SLW_DETWIN_SEL_PLLD	0	0x0
0x009D[0:1]	LOL_SLW_VALWIN_SEL_PLLA	0	0x0
0x009D[2:3]	LOL_SLW_VALWIN_SEL_PLLB	0	0x0
0x009D[4:5]	LOL_SLW_VALWIN_SEL_PLLC	0	0x0
0x009D[6:7]	LOL_SLW_VALWIN_SEL_PLLD	0	0x0
0x009E[0:3]	LOL_SLW_SET_THR_PLLA	0	0x0
0x009E[4:7]	LOL_SLW_SET_THR_PLLB	0	0x0
0x009F[0:3]	LOL_SLW_SET_THR_PLLC	0	0x0
0x009F[4:7]	LOL_SLW_SET_THR_PLLD	0	0x0
0x00A0[0:3]	LOL_SLW_CLR_THR_PLLA	0	0x0
0x00A0[4:7]	LOL_SLW_CLR_THR_PLLB	0	0x0
0x00A1[0:3]	LOL_SLW_CLR_THR_PLLC	0	0x0
0x00A1[4:7]	LOL_SLW_CLR_THR_PLLD	0	0x0
0x00A2[0]	LOL_TIMER_EN_PLLA	0	0x0
0x00A2[1]	LOL_TIMER_EN_PLLB	0	0x0
0x00A2[2]	LOL_TIMER_EN_PLLC	0	0x0
0x00A2[3]	LOL_TIMER_EN_PLLD	0	0x0
0x00A3[0:34]	LOL_CLR_DELAY_PLLA	0	0x000000000
0x00A8[0:34]	LOL_CLR_DELAY_PLLB	0	0x000000000
0x00AD[0:34]	LOL_CLR_DELAY_PLLC	0	0x000000000
0x00B2[0:34]	LOL_CLR_DELAY_PLLD	0	0x000000000
0x0102[0]	OUTALL_DISABLE_LOW	1	0x1
0x0108[0]	OUT0_PDN	1	0x1
0x0108[1]	OUT0_OE	0	0x0
0x0108[2]	OUT0_RDIV_FORCE2	0	0x0
0x0109[0:2]	OUT0_FORMAT	1	0x1
0x0109[3]	OUT0_SYNC_EN	1	0x1
0x0109[4:5]	OUT0_DIS_STATE	0	0x0
0x0109[6:7]	OUT0_CMOS_DRV	0	0x0
0x010A[0:3]	OUT0_CM	11	0xB
0x010A[4:6]	OUT0_AMPL	3	0x3
0x010B[0:2]	OUT0_MUX_SEL	0	0x0
0x010B[6:7]	OUT0_INV	0	0x0
0x010C[0:2]	OUT0_DIS_SRC	0	0x0
0x011C[0]	OUT1_PDN	1	0x1
0x011C[1]	OUT1_OE	0	0x0
0x011C[2]	OUT1_RDIV_FORCE2	0	0x0
0x011D[0:2]	OUT1_FORMAT	1	0x1
0x011D[3]	OUT1_SYNC_EN	1	0x1

0x011D[4:5]	OUT1_DIS_STATE	0	0x0
0x011D[6:7]	OUT1_CMOS_DRV	0	0x0
0x011E[0:3]	OUT1_CM	11	0xB
0x011E[4:6]	OUT1_AMPL	3	0x3
0x011F[0:2]	OUT1_MUX_SEL	0	0x0
0x011F[6:7]	OUT1_INV	0	0x0
0x0120[0:2]	OUT1_DIS_SRC	0	0x0
0x0126[0]	OUT2_PDN	1	0x1
0x0126[1]	OUT2_OE	0	0x0
0x0126[2]	OUT2_RDIV_FORCE2	0	0x0
0x0127[0:2]	OUT2_FORMAT	1	0x1
0x0127[3]	OUT2_SYNC_EN	1	0x1
0x0127[4:5]	OUT2_DIS_STATE	0	0x0
0x0127[6:7]	OUT2_CMOS_DRV	0	0x0
0x0128[0:3]	OUT2_CM	11	0xB
0x0128[4:6]	OUT2_AMPL	3	0x3
0x0129[0:2]	OUT2_MUX_SEL	0	0x0
0x0129[6:7]	OUT2_INV	0	0x0
0x012A[0:2]	OUT2_DIS_SRC	0	0x0
0x012B[0]	OUT3_PDN	1	0x1
0x012B[1]	OUT3_OE	0	0x0
0x012B[2]	OUT3_RDIV_FORCE2	0	0x0
0x012C[0:2]	OUT3_FORMAT	1	0x1
0x012C[3]	OUT3_SYNC_EN	1	0x1
0x012C[4:5]	OUT3_DIS_STATE	0	0x0
0x012C[6:7]	OUT3_CMOS_DRV	0	0x0
0x012D[0:3]	OUT3_CM	11	0xB
0x012D[4:6]	OUT3_AMPL	3	0x3
0x012E[0:2]	OUT3_MUX_SEL	0	0x0
0x012E[6:7]	OUT3_INV	0	0x0
0x012F[0:2]	OUT3_DIS_SRC	0	0x0
0x0141[0]	OUT_DIS_MSK_PLLA	0	0x0
0x0141[1]	OUT_DIS_MSK_PLLB	0	0x0
0x0141[2]	OUT_DIS_MSK_PLLC	0	0x0
0x0141[3]	OUT_DIS_MSK_PLLD	0	0x0
0x0141[5]	OUT_DIS_LOL_MSK	0	0x0
0x0141[6]	OUT_DIS_LOSXAXB_MSK	1	0x1
0x0141[7]	OUT_DIS_MSK_LOS_PFD	0	0x0
0x0142[0]	OUT_DIS_MSK_LOL_PLLA	1	0x1
0x0142[1]	OUT_DIS_MSK_LOL_PLLB	1	0x1
0x0142[2]	OUT_DIS_MSK_LOL_PLLC	1	0x1
0x0142[3]	OUT_DIS_MSK_LOL_PLLD	1	0x1
0x0142[4]	OUT_DIS_MSK_HOLD_PLLA	1	0x1
0x0142[5]	OUT_DIS_MSK_HOLD_PLLB	1	0x1
0x0142[6]	OUT_DIS_MSK_HOLD_PLLC	1	0x1
0x0142[7]	OUT_DIS_MSK_HOLD_PLLD	1	0x1
0x0202[0:31]	XAXB_FREQ_OFFSET	0	0x00000000
0x0206[0:1]	PXAXB	0	0x0
0x0208[0:47]	P0_NUM	0	0x000000000000
0x020E[0:31]	P0_DEN	0	0x00000000
0x0212[0:47]	P1_NUM	0	0x000000000000
0x0218[0:31]	P1_DEN	0	0x00000000
0x021C[0:47]	P2_NUM	0	0x000000000000
0x0222[0:31]	P2_DEN	0	0x00000000
0x0226[0:47]	P3_NUM	0	0x000000000000
0x022C[0:31]	P3_DEN	0	0x00000000
0x0231[0:3]	P0_FRACN_MODE	1	0x1
0x0231[4]	P0_FRACN_EN	0	0x0
0x0232[0:3]	P1_FRACN_MODE	1	0x1
0x0232[4]	P1_FRACN_EN	0	0x0
0x0233[0:3]	P2_FRACN_MODE	1	0x1
0x0233[4]	P2_FRACN_EN	0	0x0
0x0234[0:3]	P3_FRACN_MODE	1	0x1
0x0234[4]	P3_FRACN_EN	0	0x0

0x0235[0:43]	MXAXB_NUM	0	0x00000000000
0x023B[0:31]	MXAXB_DEN	0	0x00000000
0x0240[0]	MXAXB_FSTEP_MSK	0	0x0
0x0240[1]	MXAXB_FSTEP_DEN	0	0x0
0x0241[0:43]	MXAXB_FSTEPW	0	0x00000000000
0x024A[0:23]	R0_REG	0	0x000000
0x0256[0:23]	R1_REG	0	0x000000
0x025C[0:23]	R2_REG	0	0x000000
0x025F[0:23]	R3_REG	0	0x000000
0x026B[0:7]	DESIGN_ID0	53	0x35
0x026C[0:7]	DESIGN_ID1	51	0x33
0x026D[0:7]	DESIGN_ID2	52	0x34
0x026E[0:7]	DESIGN_ID3	55	0x37
0x026F[0:7]	DESIGN_ID4	68	0x44
0x0270[0:7]	DESIGN_ID5	66	0x42
0x0271[0:7]	DESIGN_ID6	80	0x50
0x0272[0:7]	DESIGN_ID7	49	0x31
0x0302[0:43]	N0_NUM	0	0x00000000000
0x0308[0:31]	N0_DEN	0	0x00000000
0x030D[0:43]	N1_NUM	0	0x00000000000
0x0313[0:31]	N1_DEN	0	0x00000000
0x0318[0:43]	N2_NUM	0	0x00000000000
0x031E[0:31]	N2_DEN	0	0x00000000
0x0323[0:43]	N3_NUM	0	0x00000000000
0x0329[0:31]	N3_DEN	0	0x00000000
0x0339[0:4]	N_FSTEP_MSK	0	0x00
0x033B[0:43]	N0_FSTEPW	0	0x00000000000
0x0341[0:43]	N1_FSTEPW	0	0x00000000000
0x0347[0:43]	N2_FSTEPW	0	0x00000000000
0x034D[0:43]	N3_FSTEPW	0	0x00000000000
0x0402[0]	PFD_PDNB_PLLA	1	0x1
0x0402[1]	PFD_RST_PLLA	0	0x0
0x0402[2]	M_RST_PLLA	0	0x0
0x0402[3]	PFD_CLKM_STOP_PLLA	0	0x0
0x0402[4]	ADD_DIV256_PLLA	0	0x0
0x0408[0:5]	BW0_PLLA	0	0x00
0x0409[0:5]	BW1_PLLA	0	0x00
0x040A[0:5]	BW2_PLLA	0	0x00
0x040B[0:5]	BW3_PLLA	0	0x00
0x040C[0:5]	BW4_PLLA	0	0x00
0x040D[0:5]	BW5_PLLA	0	0x00
0x040E[0:5]	FAST_BW0_PLLA	0	0x00
0x040F[0:5]	FAST_BW1_PLLA	0	0x00
0x0410[0:5]	FAST_BW2_PLLA	0	0x00
0x0411[0:5]	FAST_BW3_PLLA	0	0x00
0x0412[0:5]	FAST_BW4_PLLA	0	0x00
0x0413[0:5]	FAST_BW5_PLLA	0	0x00
0x0415[0:55]	M_NUM_PLLA	0	0x00000000000000
0x041C[0:31]	M_DEN_PLLA	0	0x00000000
0x0421[0:3]	M_FRAC_MODE_PLLA	1	0x1
0x0421[4]	M_FRAC_EN_PLLA	0	0x0
0x0422[0]	M_FSTEP_MSK_PLLA	1	0x1
0x0422[1]	M_FSTEPW_DEN_PLLA	0	0x0
0x0423[0:55]	M_FSTEPW_PLLA	0	0x00000000000000
0x042A[0:2]	IN_SEL_PLLA	0	0x0
0x042B[0]	FASTLOCK_AUTO_EN_PLLA	1	0x1
0x042B[1]	FASTLOCK_MAN_PLLA	0	0x0
0x042C[0]	HOLD_EN_PLLA	1	0x1
0x042C[3]	HOLD_RAMP_BYP_PLLA	1	0x1
0x042C[5:7]	HOLD_RAMP_RATE_PLLA	0	0x0
0x042D[1]	HOLD_RAMPBYP_NOHIST_PLLA	1	0x1
0x042E[0:4]	HOLD_HIST_LEN_PLLA	0	0x00
0x042F[0:4]	HOLD_HIST_DELAY_PLLA	0	0x00
0x0431[0:4]	HOLD_REF_COUNT_FRC_PLLA	0	0x00

0x0432[0:23]	HOLD_15M_CYC_COUNT_PLLA	1024	0x000400
0x0436[0:1]	CLK_SWITCH_MODE_PLLA	2	0x2
0x0436[2]	HSW_EN_PLLA	1	0x1
0x0436[3]	HSW_RAMP_BYP_PLLA	1	0x1
0x0437[0:3]	IN_LOS_MSK_PLLA	0	0x0
0x0437[4:7]	IN_OOF_MSK_PLLA	0	0x0
0x0438[0:2]	IN0_PRIORITY_PLLA	0	0x0
0x0438[4:6]	IN1_PRIORITY_PLLA	0	0x0
0x0439[0:2]	IN2_PRIORITY_PLLA	0	0x0
0x0439[4:6]	IN3_PRIORITY_PLLA	0	0x0
0x0502[4]	ADD_DIV256_PLLB	0	0x0
0x0508[0:5]	BW0_PLLB	0	0x00
0x0509[0:5]	BW1_PLLB	0	0x00
0x050A[0:5]	BW2_PLLB	0	0x00
0x050B[0:5]	BW3_PLLB	0	0x00
0x050C[0:5]	BW4_PLLB	0	0x00
0x050D[0:5]	BW5_PLLB	0	0x00
0x050E[0:5]	FAST_BW0_PLLB	0	0x00
0x050F[0:5]	FAST_BW1_PLLB	0	0x00
0x0510[0:5]	FAST_BW2_PLLB	0	0x00
0x0511[0:5]	FAST_BW3_PLLB	0	0x00
0x0512[0:5]	FAST_BW4_PLLB	0	0x00
0x0513[0:5]	FAST_BW5_PLLB	0	0x00
0x0515[0:55]	M_NUM_PLLB	0	0x00000000000000
0x051C[0:31]	M_DEN_PLLB	0	0x00000000
0x0521[0:3]	M_FRAC_MODE_PLLB	1	0x1
0x0521[4]	M_FRAC_EN_PLLB	0	0x0
0x0522[0]	M_FSTEP_MSK_PLLB	1	0x1
0x0522[1]	M_FSTEPW_DEN_PLLB	0	0x0
0x0523[0:55]	M_FSTEPW_PLLB	0	0x00000000000000
0x052A[0]	IN_SEL_REGCTRL_PLLB	1	0x1
0x052A[1:3]	IN_SEL_PLLB	0	0x0
0x052B[0]	FASTLOCK_AUTO_EN_PLLB	1	0x1
0x052B[1]	FASTLOCK_MAN_PLLB	0	0x0
0x052C[0]	HOLD_EN_PLLB	1	0x1
0x052C[3]	HOLD_RAMP_BYP_PLLB	1	0x1
0x052C[5:7]	HOLD_RAMP_RATE_PLLB	0	0x0
0x052D[1]	HOLD_RAMPBYP_NOHIST_PLLB	1	0x1
0x052E[0:4]	HOLD_HIST_LEN_PLLB	0	0x00
0x052F[0:4]	HOLD_HIST_DELAY_PLLB	0	0x00
0x0531[0:4]	HOLD_REF_COUNT_FRC_PLLB	0	0x00
0x0532[0:23]	HOLD_15M_CYC_COUNT_PLLB	1024	0x000400
0x0536[0:1]	CLK_SWITCH_MODE_PLLB	2	0x2
0x0536[2]	HSW_EN_PLLB	1	0x1
0x0536[3]	HSW_RAMP_BYP_PLLB	1	0x1
0x0537[0:3]	IN_LOS_MSK_PLLB	0	0x0
0x0537[4:7]	IN_OOF_MSK_PLLB	0	0x0
0x0538[0:2]	IN0_PRIORITY_PLLB	0	0x0
0x0538[4:6]	IN1_PRIORITY_PLLB	0	0x0
0x0539[0:2]	IN2_PRIORITY_PLLB	0	0x0
0x0539[4:6]	IN3_PRIORITY_PLLB	0	0x0
0x0602[4]	ADD_DIV256_PLLC	0	0x0
0x0608[0:5]	BW0_PLLC	0	0x00
0x0609[0:5]	BW1_PLLC	0	0x00
0x060A[0:5]	BW2_PLLC	0	0x00
0x060B[0:5]	BW3_PLLC	0	0x00
0x060C[0:5]	BW4_PLLC	0	0x00
0x060D[0:5]	BW5_PLLC	0	0x00
0x060E[0:5]	FAST_BW0_PLLC	0	0x00
0x060F[0:5]	FAST_BW1_PLLC	0	0x00
0x0610[0:5]	FAST_BW2_PLLC	0	0x00
0x0611[0:5]	FAST_BW3_PLLC	0	0x00
0x0612[0:5]	FAST_BW4_PLLC	0	0x00
0x0613[0:5]	FAST_BW5_PLLC	0	0x00

0x0615[0:55]	M_NUM_PLLC	0	0x00000000000000
0x061C[0:31]	M_DEN_PLLC	0	0x00000000
0x0621[0:3]	M_FRAC_MODE_PLLC	1	0x1
0x0621[4]	M_FRAC_EN_PLLC	0	0x0
0x0622[0]	M_FSTEP_MSK_PLLC	1	0x1
0x0622[1]	M_FSTEPW_DEN_PLLC	0	0x0
0x0623[0:55]	M_FSTEPW_PLLC	0	0x00000000000000
0x062A[0:2]	IN_SEL_PLLC	0	0x0
0x062B[0]	FASTLOCK_AUTO_EN_PLLC	1	0x1
0x062B[1]	FASTLOCK_MAN_PLLC	0	0x0
0x062C[0]	HOLD_EN_PLLC	1	0x1
0x062C[3]	HOLD_RAMP_BYP_PLLC	1	0x1
0x062C[5:7]	HOLD_RAMP_RATE_PLLC	0	0x0
0x062D[1]	HOLD_RAMPBYP_NOHIST_PLLC	1	0x1
0x062E[0:4]	HOLD_HIST_LEN_PLLC	0	0x00
0x062F[0:4]	HOLD_HIST_DELAY_PLLC	0	0x00
0x0631[0:4]	HOLD_REF_COUNT_FRC_PLLC	0	0x00
0x0632[0:23]	HOLD_15M_CYC_COUNT_PLLC	1024	0x000400
0x0636[0:1]	CLK_SWITCH_MODE_PLLC	2	0x2
0x0636[2]	HSW_EN_PLLC	1	0x1
0x0636[3]	HSW_RAMP_BYP_PLLC	1	0x1
0x0637[0:3]	IN_LOS_MSK_PLLC	0	0x0
0x0637[4:7]	IN_OOF_MSK_PLLC	0	0x0
0x0638[0:2]	IN0_PRIORITY_PLLC	0	0x0
0x0638[4:6]	IN1_PRIORITY_PLLC	0	0x0
0x0639[0:2]	IN2_PRIORITY_PLLC	0	0x0
0x0639[4:6]	IN3_PRIORITY_PLLC	0	0x0
0x0702[4]	ADD_DIV256_PLLD	0	0x0
0x0709[0:5]	BW0_PLLD	0	0x00
0x070A[0:5]	BW1_PLLD	0	0x00
0x070B[0:5]	BW2_PLLD	0	0x00
0x070C[0:5]	BW3_PLLD	0	0x00
0x070D[0:5]	BW4_PLLD	0	0x00
0x070E[0:5]	BW5_PLLD	0	0x00
0x070F[0:5]	FAST_BW0_PLLD	0	0x00
0x0710[0:5]	FAST_BW1_PLLD	0	0x00
0x0711[0:5]	FAST_BW2_PLLD	0	0x00
0x0712[0:5]	FAST_BW3_PLLD	0	0x00
0x0713[0:5]	FAST_BW4_PLLD	0	0x00
0x0714[0:5]	FAST_BW5_PLLD	0	0x00
0x0716[0:55]	M_NUM_PLLD	0	0x00000000000000
0x071D[0:31]	M_DEN_PLLD	0	0x00000000
0x0722[0:3]	M_FRAC_MODE_PLLD	1	0x1
0x0722[4]	M_FRAC_EN_PLLD	0	0x0
0x0723[0]	M_FSTEP_MSK_PLLD	1	0x1
0x0723[1]	M_FSTEPW_DEN_PLLD	0	0x0
0x0724[0:55]	M_FSTEPW_PLLD	0	0x00000000000000
0x072B[0:2]	IN_SEL_PLLD	0	0x0
0x072C[0]	FASTLOCK_AUTO_EN_PLLD	1	0x1
0x072C[1]	FASTLOCK_MAN_PLLD	0	0x0
0x072D[0]	HOLD_EN_PLLD	1	0x1
0x072D[3]	HOLD_RAMP_BYP_PLLD	1	0x1
0x072D[5:7]	HOLD_RAMP_RATE_PLLD	0	0x0
0x072E[1]	HOLD_RAMPBYP_NOHIST_PLLD	1	0x1
0x072F[0:4]	HOLD_HIST_LEN_PLLD	0	0x00
0x0730[0:4]	HOLD_HIST_DELAY_PLLD	0	0x00
0x0732[0:4]	HOLD_REF_COUNT_FRC_PLLD	0	0x00
0x0733[0:23]	HOLD_15M_CYC_COUNT_PLLD	1024	0x000400
0x0737[0:1]	CLK_SWITCH_MODE_PLLD	2	0x2
0x0737[2]	HSW_EN_PLLD	1	0x1
0x0737[3]	HSW_RAMP_BYP_PLLD	1	0x1
0x0738[0:3]	IN_LOS_MSK_PLLD	0	0x0
0x0738[4:7]	IN_OOF_MSK_PLLD	0	0x0
0x0739[0:2]	IN0_PRIORITY_PLLD	0	0x0

0x0739[4:6]	IN1_PRIORITY_PLLD	0	0x0
0x073A[0:2]	IN2_PRIORITY_PLLD	0	0x0
0x073A[4:6]	IN3_PRIORITY_PLLD	0	0x0
0x090E[0]	XAXB_EXTCLK_EN	0	0x0
0x0943[0]	IO_VDD_SEL	0	0x0
0x0949[0:3]	IN_EN	0	0x0
0x0949[4:7]	IN_PULSED_CMOS_EN	0	0x0
0x094A[0:3]	INX_TO_PFD_EN	15	0xF
0x0A03[0:4]	N_CLK_TO_OUTX_EN	15	0x0F
0x0A04[0:4]	N_PIBYP	0	0x00
0x0A05[0:4]	N_PDNB	15	0x0F
0x0B44[0:3]	PDIV_FRACN_CLK_DIS	0	0x0
0x0B44[4]	FRACN_CLK_DIS_PLLA	0	0x0
0x0B44[5]	FRACN_CLK_DIS_PLLB	0	0x0
0x0B44[6]	FRACN_CLK_DIS_PLLC	0	0x0
0x0B44[7]	FRACN_CLK_DIS_PLLD	0	0x0
0x0B45[0]	CLK_DIS_PLLA	0	0x0
0x0B45[1]	CLK_DIS_PLLB	0	0x0
0x0B45[2]	CLK_DIS_PLLC	0	0x0
0x0B45[3]	CLK_DIS_PLLD	0	0x0
0x0B46[0:3]	LOS_CLK_DIS	0	0x0
0x0B47[0:4]	OOF_CLK_DIS	0	0x00
0x0B48[0:4]	OOF_DIV_CLK_DIS	15	0x0F
0x0B4A[0:4]	N_CLK_DIS	0	0x00

This datasheet addendum is provided as supplemental information to the Si5347D datasheet, located at www.silabs.com/timing. You can search for and download any datasheet addendum for Si534x/8x part numbers. Go to http://www.silabs.com/custom-timing for more information.

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