Data Sheet | September 28, 2009 | FN6239.2

Precision 0.600V Low Voltage FGA™ References

The ISL21032 FGA™ voltage references are very high precision analog voltage references specifically designed to meet the rigorous performance requirements of high current, low voltage VRM and POL modules.

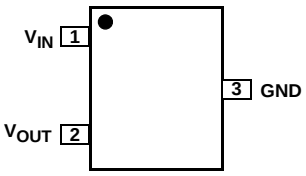
Fabricated in Intersil's proprietary Floating Gate Analog technology, these references feature guaranteed performance over the -40°C to +130°C operating temperature range.

Additional features include guaranteed absolute accuracy as low as ±0.5% over the operating temperature range of -40°C to +130°C. Long-term stability is 10ppm/$\sqrt{1{,}000\text{Hrs}}$.

The absolute accuracy and thermal performance of the ISL21032 family are an ideal fit for the next generation of high current, low voltage VRM and POL modules.

Pinout

ISL21032
(3 LD SOT-23
TOP VIEW)



Features

- Reference Voltage 0.6V
- Initial Accuracy Options @ +25°C ±1.0mV, ±2.5mV, and ±5.0mV
- Absolute Accuracy Options Over Operating Temp Range ±0.5% (±3.0mV), ±0.75% (±4.5mV), and ±1.0% (±6.0mV)
- Supply Voltage Range . . . . . 2.7V to 5.5V
- Low Quiescent Current . . . . . 12µA typ.
- Long Term Stability. . . . . 10ppm/$\sqrt{1{,}000\text{Hrs}}$.
- Thermal Hysteresis . . . . . 100ppm @ ΔT_A = +170°C
- Source and Sink Current 7mA
- ESD Protection. . . . . 5kV (Human Body Model)
- Standard 3 Ld SOT-23 Packaging
- Extended Temperature Range . . . . . -40°C to +130°C
- Pb-Free (RoHS Compliant)

Applications

- Low Voltage, High Current VRM and POL Modules
- Accurate Reference for Low Voltage DC/DC Converters

Ordering Information

PART NUMBER (Note)	PART MARKING	V_{OUT} OPTION (V)	GRADE	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL21032BPH306Z-TK*	DEU	0.6	±0.5%@ DT_A = 170°C	-40 to +130	3 Ld SOT-23 T&R	P3.064
ISL21032CPH306Z-TK*	DEV	0.6	±0.75%@ DT_A = 170°C	-40 to +130	3 Ld SOT-23 T&R	P3.064
ISL21032DPH306Z-TK*	APE	0.6	±1.0%@ DT_A = 170°C	-40 to +130	3 Ld SOT-23 T&R	P3.064

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Storage Temperature Range . . . . . .-65°C to +150°C
Max Voltage V_{IN} to GND . . . . . -0.5V to +6.5V
Max Voltage V_{OUT} to GND (Note 1)
ISL21032, V_{OUT} = 0.6V . . . . . -0.5V to +1.6V
Voltage on “DNC” Pins. . . No Connections Permitted to These Pins.
ESD Rating
Human Body Model 5kV
Machine Model. 500V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
3 Ld SOT-23 Package	371.4

Storage Temperature . . . . . .-65°C to +150°C
Pb-Free Reflow Profile (Note 3). . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

For guaranteed specifications and test conditions, see Electrical Specifications.

The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

NOTES:

1. Maximum duration = 10s.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
3. Post-reflow drift for the ISL21032 devices will range from 100µV to 1.0mV based on experimental results with devices tested in sockets and also on FR4 multi-layer PC boards. The design engineer must take this into account when considering the reference voltage after assembly.

Electrical Specifications (VOUT = 0.600V)

Operating Conditions: V_{IN} = 3.0V, I_{OUT} = 0mA, C_{OUT} = 0.001µF, T_A = -40 to +130°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage			0.600		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C	ISL21032B06	-1.0		+1.0	mV
		ISL21032C06	-2.5		+2.5	mV
		ISL21032D06	-5.0		+5.0	mV
V_{OA}	V_{OUT} Accuracy Over Op Temp Range (-40° < T_A < +130°C)	ISL21032B06	-3.0		+3.0	mV
		ISL21032C06	-4.5		+4.5	mV
		ISL21032D06	-6.0		+6.0	mV
V_{IN}	Input Voltage Range		2.7		5.5	V
I_{IN}	Supply Current			12	25	µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	+2.7V ≤ V_{IN} ≤ +5.5V		50	200	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{SOURCE} ≤ 7mA		20	70	µV/mA
		Sinking: -7mA ≤ I_{SINK} ≤ 0mA		20	70	µV/mA
$\Delta V_{OUT}/\Delta t$	Long Term Stability (Note 6)	T_A = +25°C		10		ppm/√1kHrs
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 4)	ΔT_A = +170°C		100		ppm
I_{SC}	Short Circuit Current (Note 5)	T_A = +25°C, V_{OUT} tied to GND		50	80	mA
V_N	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz		30		μV_{P-P}

NOTES:

4. Thermal Hysteresis is the change in V_{OUT} measured @ T_A = +25°C after temperature cycling over a specified range, ΔT_A. V_{OUT} is read initially at T_A = +25°C for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at +25°C. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For ΔT_A = 170°C, the device under is cycled from +25°C to +130°C to -40°C to +25°C.
5. Limits are established by full device characterization over temperature range and are not tested in production.
6. FGA™ voltage reference long term drift is a logarithmic characteristic. Changes that occur after the first few hundred hours of operation are significantly smaller with time, asymptotically approaching zero beyond 2000 hours. Because of this decreasing characteristic, long-term drift is specified in ppm/√1kHr.

Typical Performance Curves, ISL21032 Low Voltage Output Reference

V_{IN} = 3.0V, I_{OUT} = 0mA, T_A = +25°C Unless Otherwise Specified

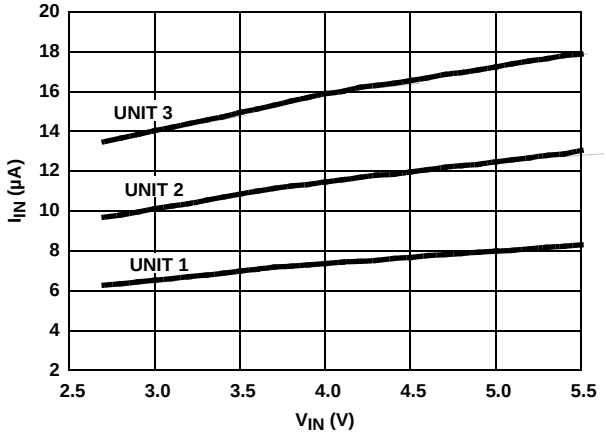


FIGURE 1. I_{IN} vs V_{IN} (3 REPRESENTATIVE UNITS)

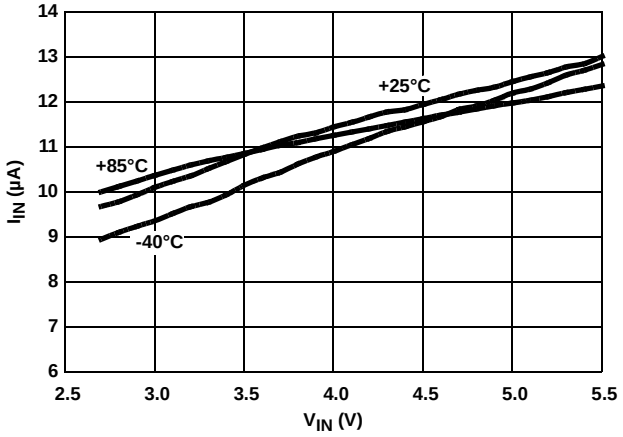


FIGURE 2. I_{IN} vs V_{IN} - 3 TEMPS

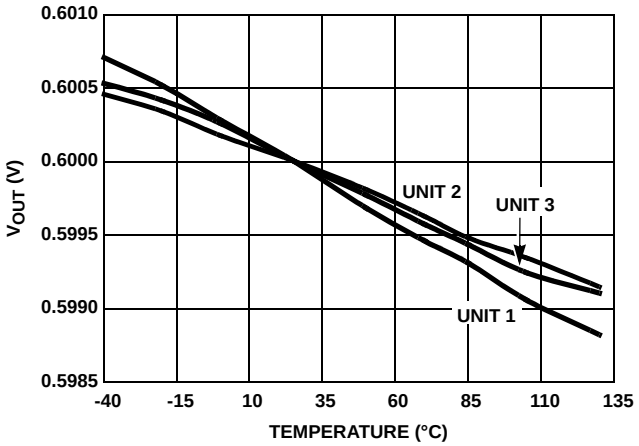


FIGURE 3. V_{OUT} vs TEMP

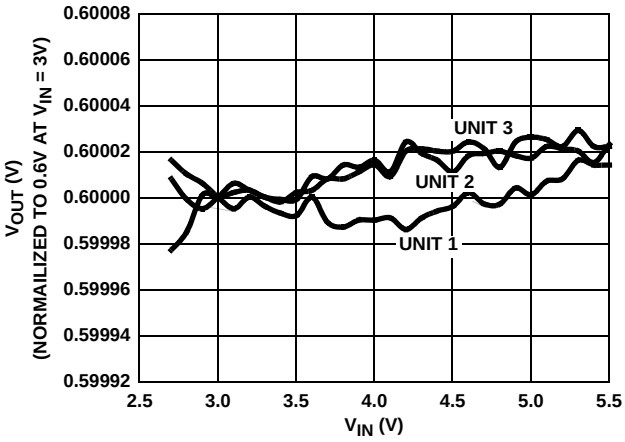


FIGURE 4. LINE REGULATION

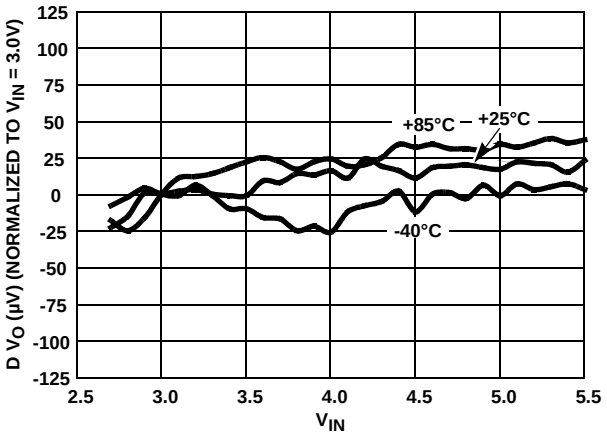


FIGURE 5. LINE REGULATION - 3 TEMPS

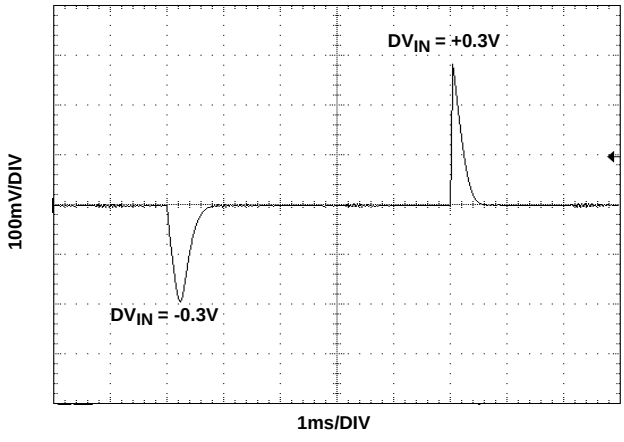


FIGURE 6. LINE TRANSIENT RESPONSE, C_L = 0nF

Typical Performance Curves, ISL21032 Low Voltage Output Reference

V_{IN} = 3.0V, I_{OUT} = 0mA, T_A = +25°C Unless Otherwise Specified **(Continued)**

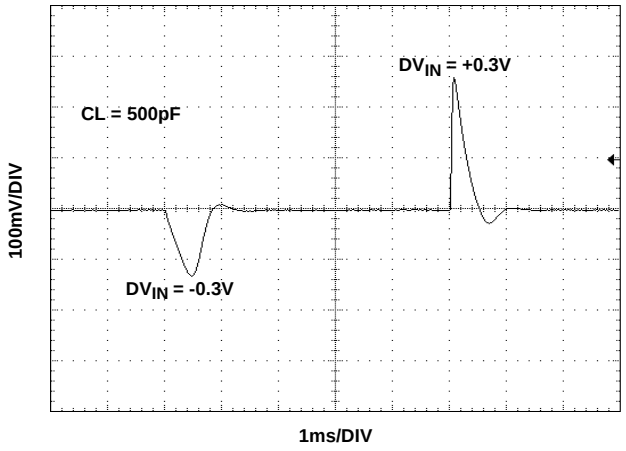


FIGURE 7. LINE TRANSIENT RESPONSE, C_L = 1nF

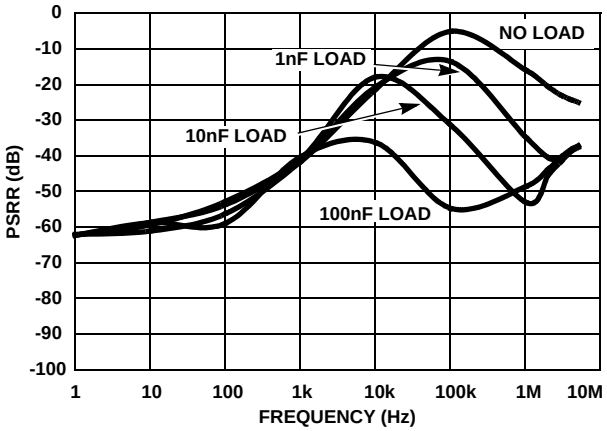


FIGURE 8. PSRR vs f vs C_L

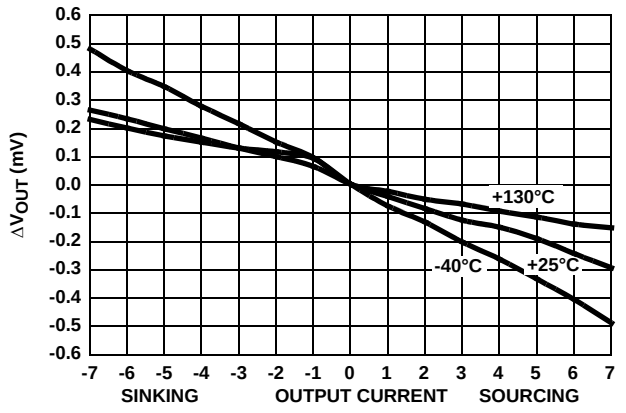


FIGURE 9. LOAD REGULATION vs TEMP

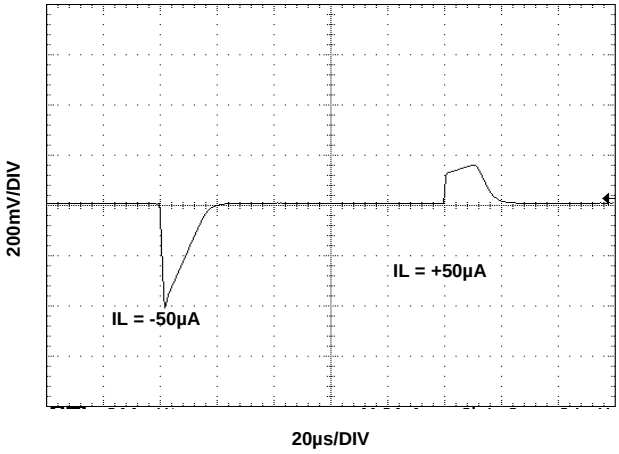


FIGURE 10. LOAD TRANSIENT RESPONSE @ I_L = 50µA, C_L = 1nF

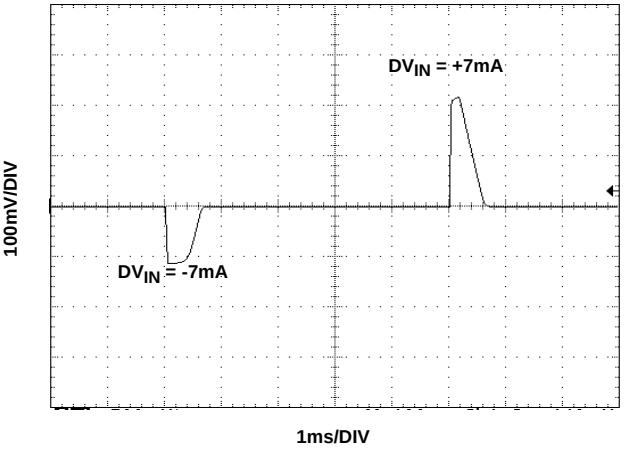


FIGURE 11. LOAD TRANSIENT RESPONSE @ I_L = 7mA, C_L = 1nF

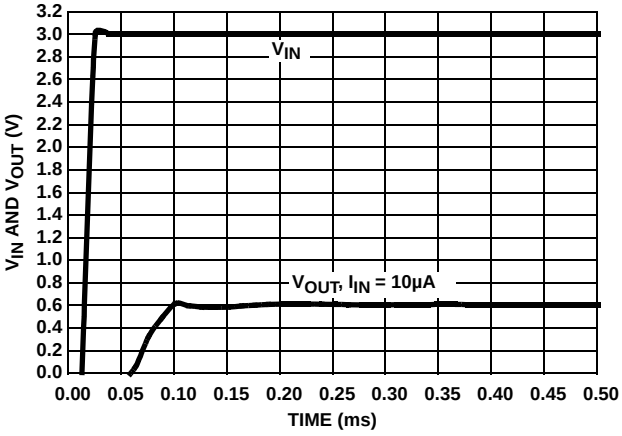


FIGURE 12. TURN-ON TIME @ T_A = +25°C

Typical Performance Curves, ISL21032 Low Voltage Output Reference

V_{IN} = 3.0V, I_{OUT} = 0mA, T_A = +25°C Unless Otherwise Specified **(Continued)**

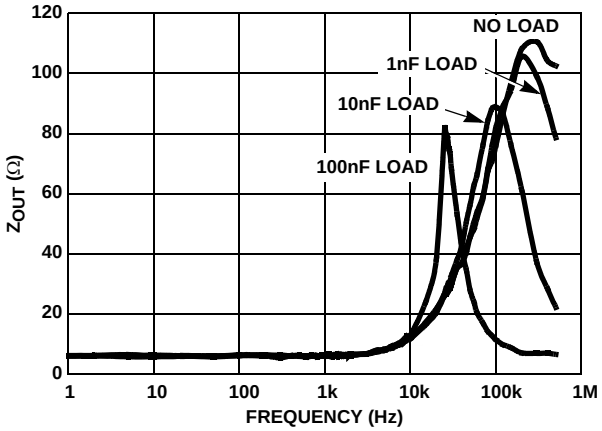


FIGURE 13. Z_{OUT} vs f vs C_L

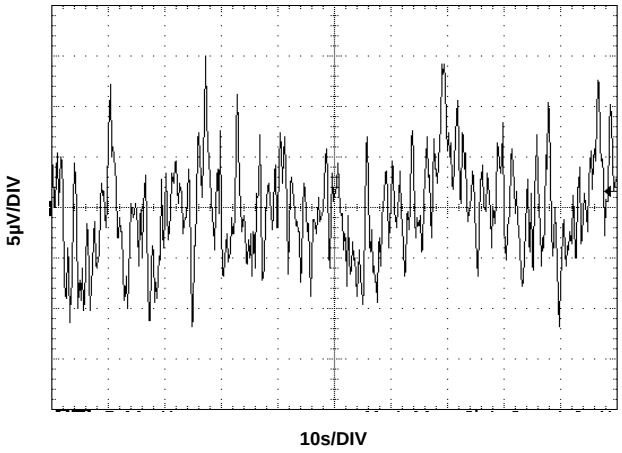


FIGURE 14. V_{OUT} NOISE

FGA Technology

The ISL21032 series of voltage references use the floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

FGA references provide high accuracy and low temperature drift but some PC board assembly precautions are necessary. Normal Output voltage shifts of 100µV to 1mV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

Post-assembly x-ray inspection may also lead to permanent changes in device output voltage and should be minimized or avoided. If x-ray inspection is required, it is advisable to monitor the reference output voltage to verify excessive shift has not occurred. If large amounts of shift are observed, it is best to add an X-ray shield consisting of thin zinc (300µm) sheeting to allow clear imaging, yet block x-ray energy that affects the FGA reference.

Special Applications Considerations

In addition to post-assembly examination, there are also other X-ray sources that may affect the FGA reference long term accuracy. Airport screening machines contain X-rays and will have a cumulative effect on the voltage reference output accuracy. Carry-on luggage screening uses low level X-rays and is not a major source of output voltage shift, although if a product is expected to pass through that type of screening over 100 times it may need to consider shielding with copper or aluminum. Checked luggage X-rays are higher intensity and can cause output voltage shift in much fewer passes, so devices expected to go through those machines should definitely consider shielding. Note that just two layers of 1/2 ounce copper planes will reduce the received dose by over 90%. The leadframe for the device which is on the bottom also provides similar shielding.

If a device is expected to pass through luggage X-ray machines numerous times, it is advised to mount a 2-layer (minimum) PC board on the top, and along with a ground plane underneath will effectively shield it from from 50 to 100 passes through the machine. Since these machines vary in X-ray dose delivered, it is difficult to produce an accurate maximum pass recommendation.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $30\mu V_{P-P}$. The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Wideband noise is reduced by adding capacitor to the output, but the value should be limited to 1nF or less to insure stability.

Temperature Drift

The limits stated for output accuracy over-temperature are governed by the method of measurement. For the -40°C to 130°C temperature range, measurements are made at +25°C and the two extremes. This measurement method combined with the fact that FGA references have a fairly linear temperature drift characteristic insures that the limits stated will not be exceeded over the temperature range.

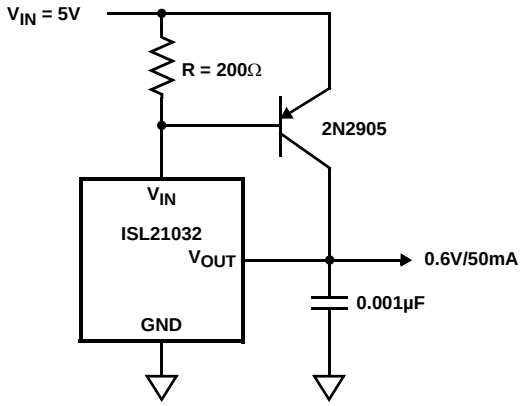
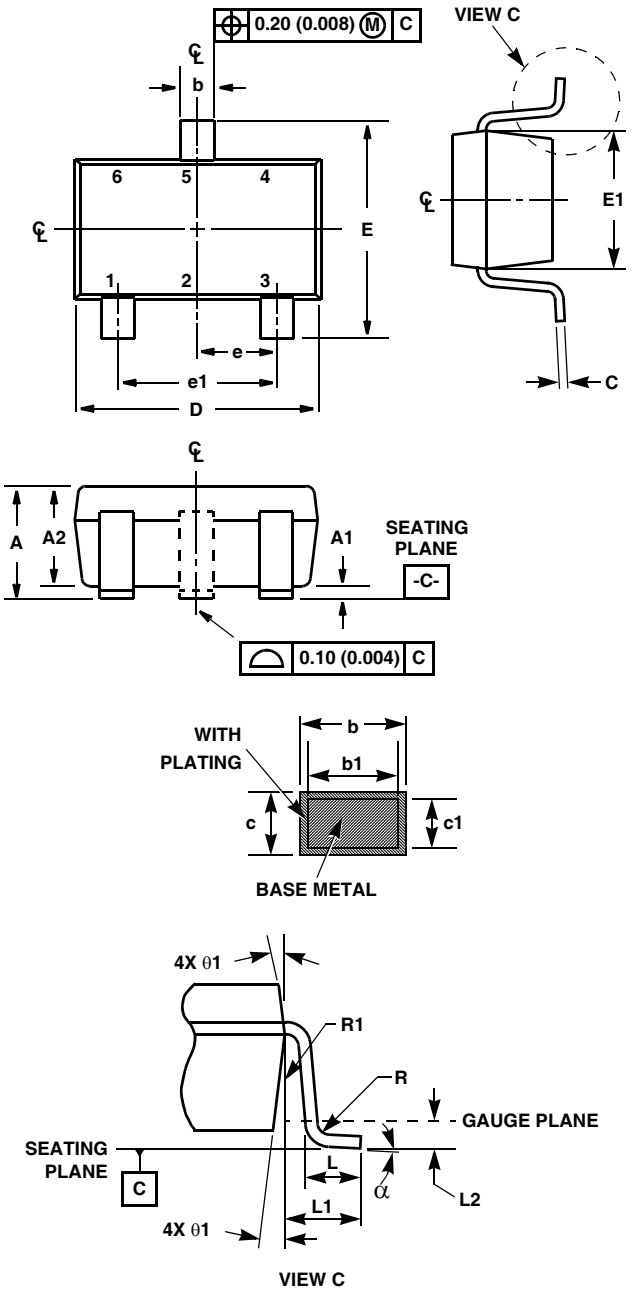


FIGURE 15. PRECISION LOW NOISE, LOW DRIFT, 0.6V, 50mA REFERENCE

Small Outline Transistor Plastic Packages (SOT23-3)



P3.064

3 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.035	0.044	0.89	1.12	-
A1	0.001	0.004	0.013	0.10	-
A2	0.035	0.037	0.88	0.94	-
b	0.015	0.020	0.37	0.50	-
b1	0.012	0.018	0.30	0.45	-
c	0.003	0.007	0.085	0.18	6
c1	0.003	0.005	0.08	0.13	6
D	0.110	0.120	2.80	3.04	3
E	0.083	0.104	2.10	2.64	-
E1	0.047	0.055	1.20	1.40	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	-	0.016	0.21	0.41	4
L1	0.024 Ref		0.60 Ref		-
L2	0.010 Ref		0.25 Ref		-
N	3		3		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.10	0.25	-
a	0°	8°	0°	8°	-

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NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only
8. Die is facing up for mold die and trim-form.