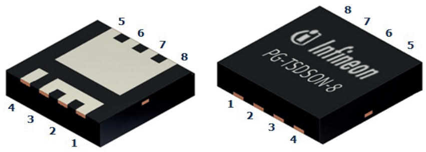
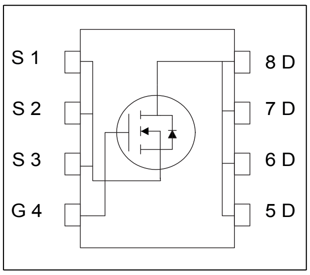
MOSFET

OptiMOS™5 Power-MOSFET, 30 V

TSDSON-8 FL
(enlarged source interconnection)





Features

- Optimized for high performance Wireless charger
- Very low FOM_{QOSS} for high frequency SMPS
- Low FOM_{SW} for high frequency SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	4.4	mΩ
I_D	17	A
Q_{OSS}	7.2	nC
Q_G(0V..4.5V)	5.2	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ0589NS	PG-TSDSON-8 FL	0589NS	-

[1)] J-STD20 and JESD22

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	17 10	A	V_{GS}=10 V, T_A=25 °C V_{GS}=10 V, T_A=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	68	A	T_A=25 °C
Avalanche current, single pulse[2]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	20	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	2.1	-	W	T_A=25 °C, R_{thJA}=60 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.6	K/W	-
Device on PCB, 6 cm² cooling area[3]	R_{thJA}	-	-	60	K/W	-

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=24 V, V_{GS}=0 V, T_j=25 °C V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	4.4 3.5	5.3 4.4	mΩ	V_{GS}=4.5 V, I_D=8 A V_{GS}=10 V, I_D=8 A
Gate resistance[4]	R_G	-	1	1.7	Ω	-
Transconductance	g_{fs}	28	56	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=10 A

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[4] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	700	950	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	220	300	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	16	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	2.3	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2.4	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	13	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	2.0	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=8 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.7	-	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	1.1	-	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	1.3	-	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	1.9	-	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	5.2	-	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 4.5 V
Gate charge total[1]	Q_g	-	11	15	nC	V_{DD}=15 V, I_D=8 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	4.8	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	7.2	-	nC	V_{DD}=15 V, V_{GS}=0 V

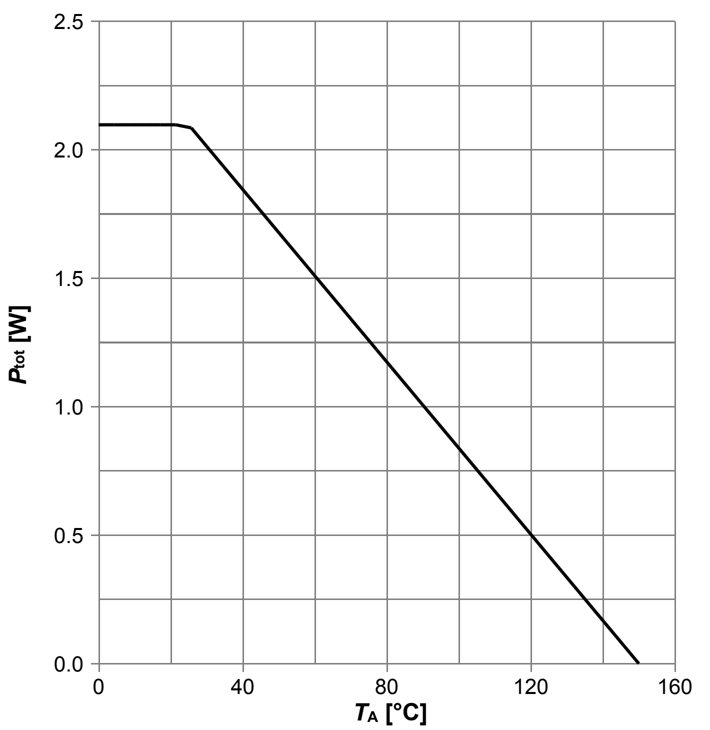
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	2.1	A	T_A=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	68	A	T_A=25 °C
Diode forward voltage	V_{SD}	-	0.71	1.1	V	V_{GS}=0 V, I_F=2.1 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	10	-	nC	V_R=15 V, I_F=30A, di_F/dt=400 A/µs

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

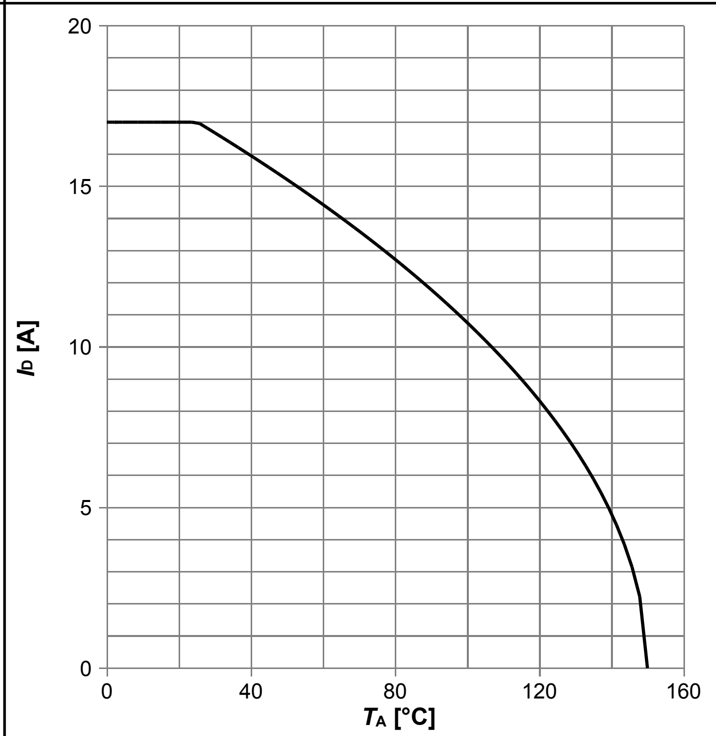
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



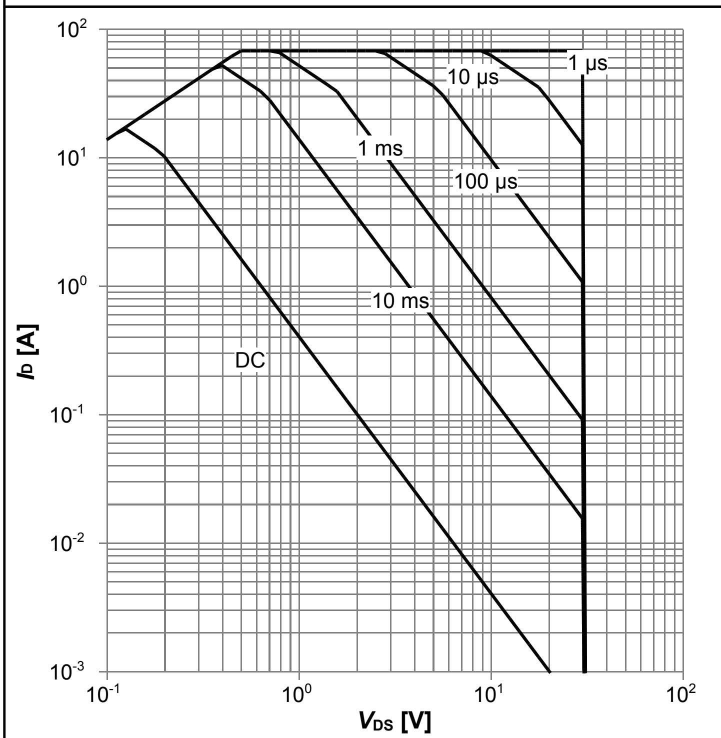
P_{tot}=f(T_A)

Diagram 2: Drain current



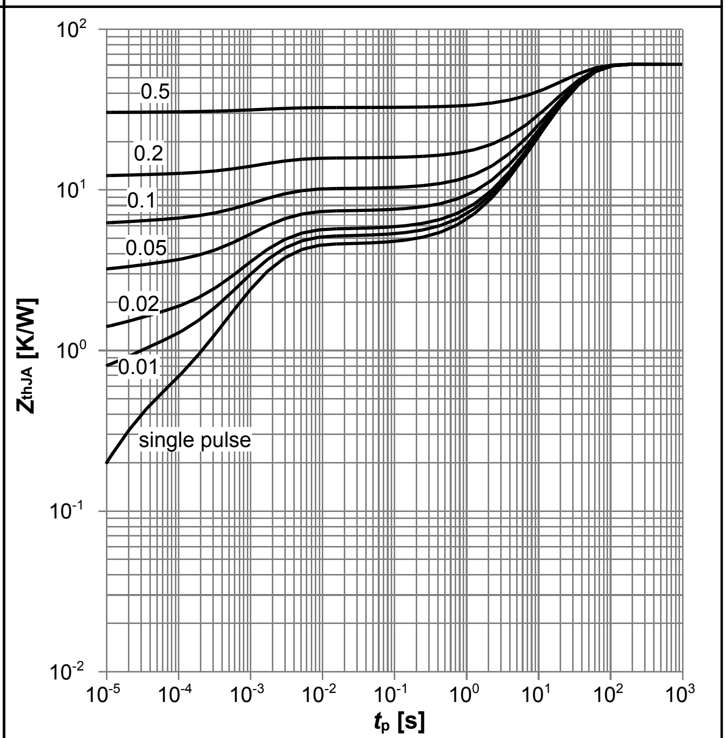
I_D=f(T_A); parameter: V_{GS}

Diagram 3: Safe operating area



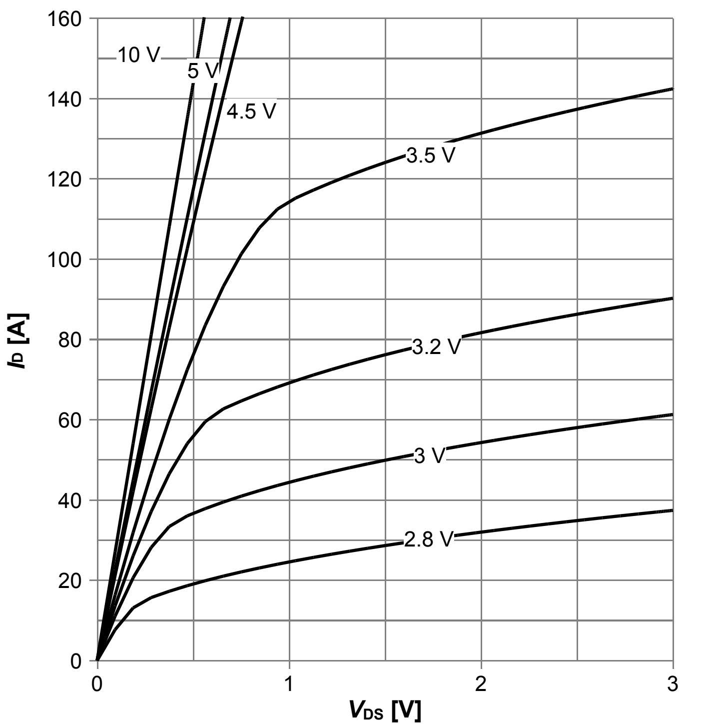
I_D=f(V_{DS}); T_A=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



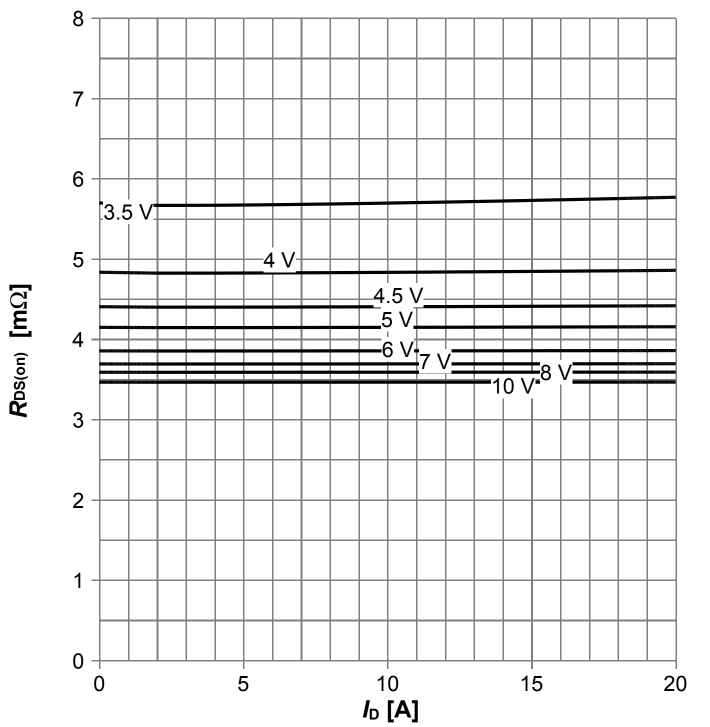
Z_{thJA}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



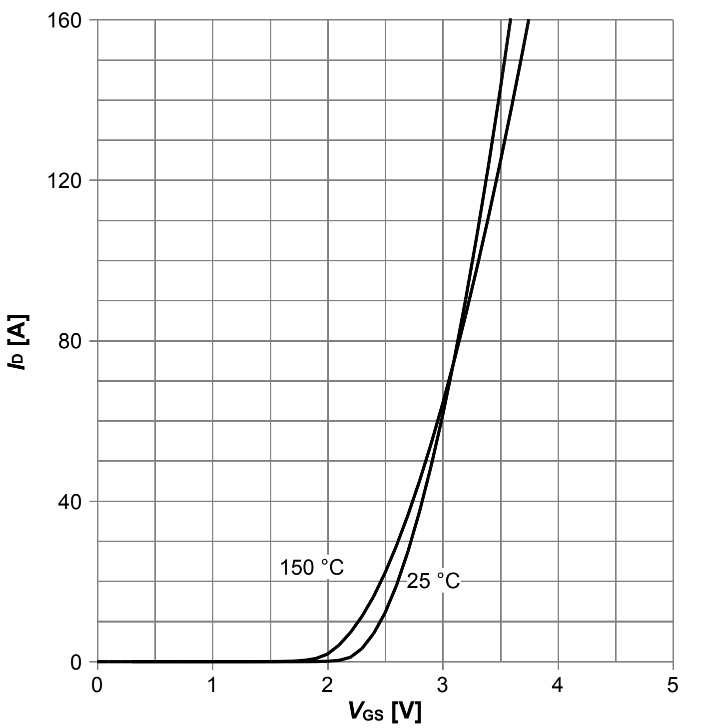
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



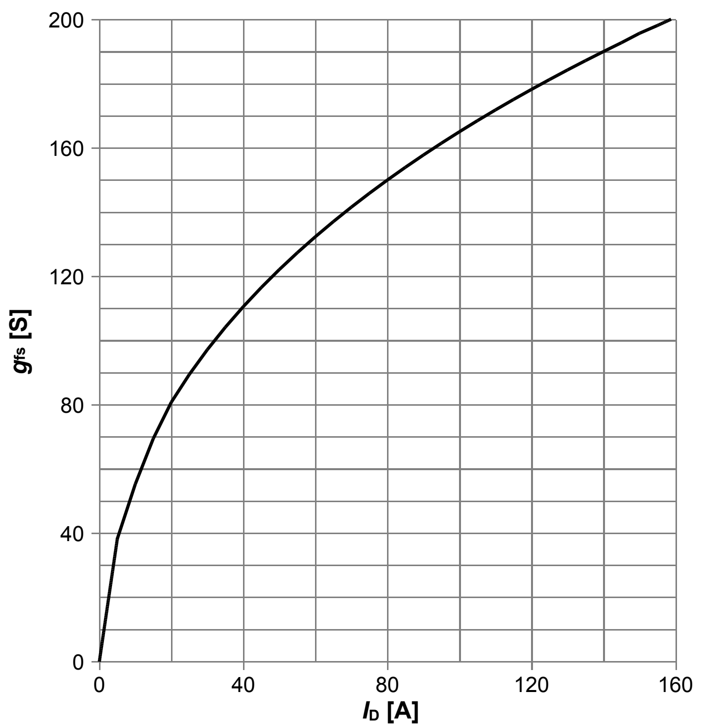
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



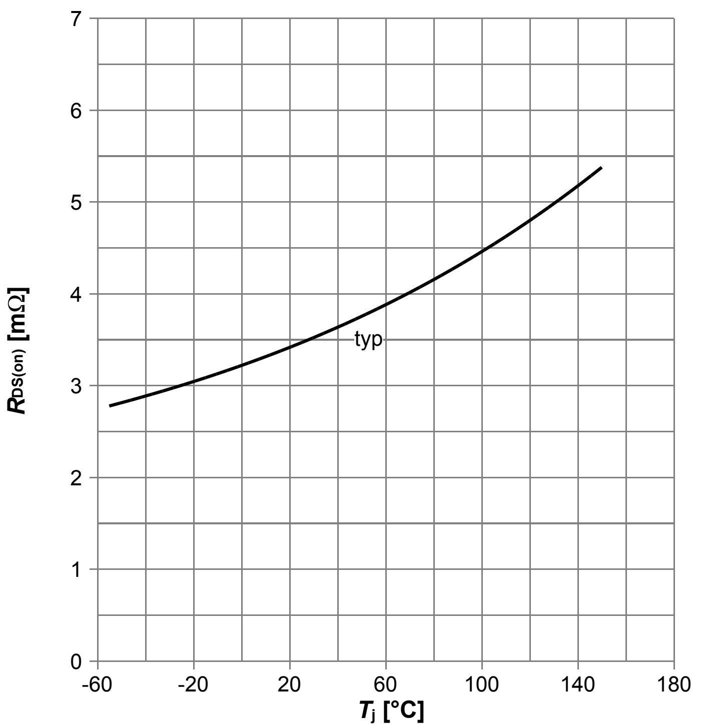
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



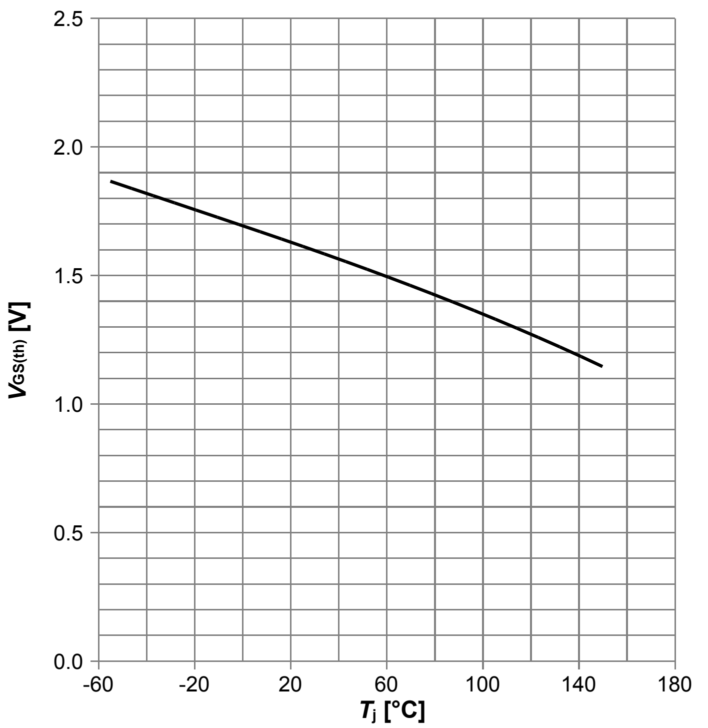
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



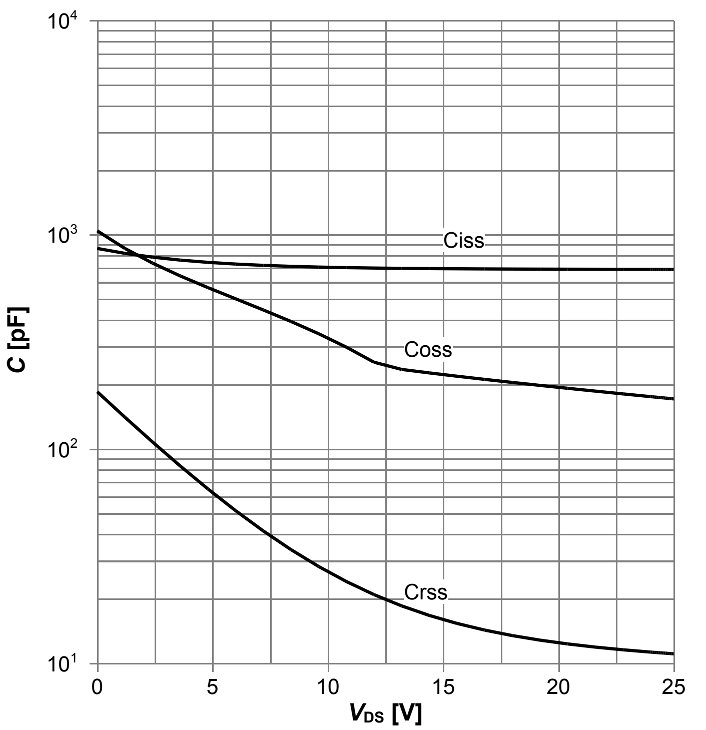
$R_{DS(on)}$=f(T_j); I_D=8 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



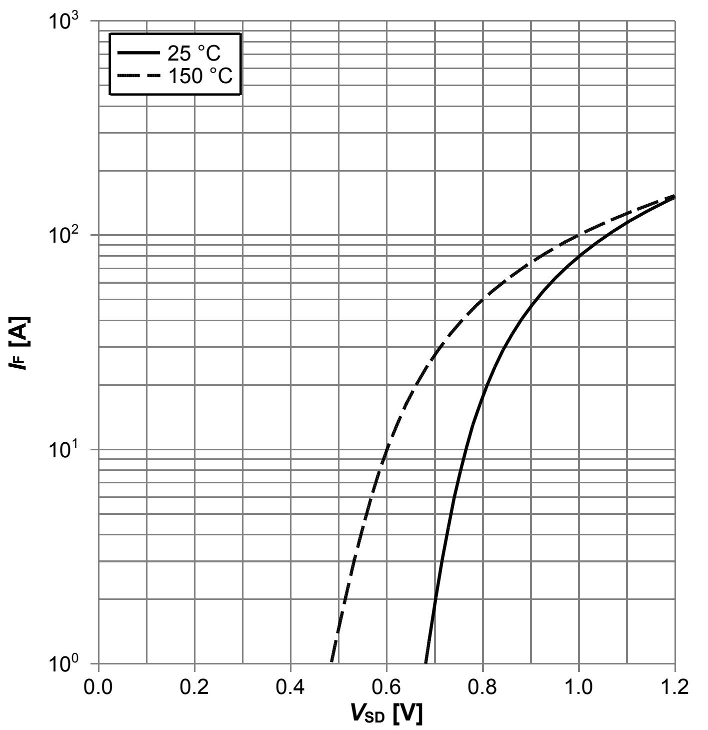
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



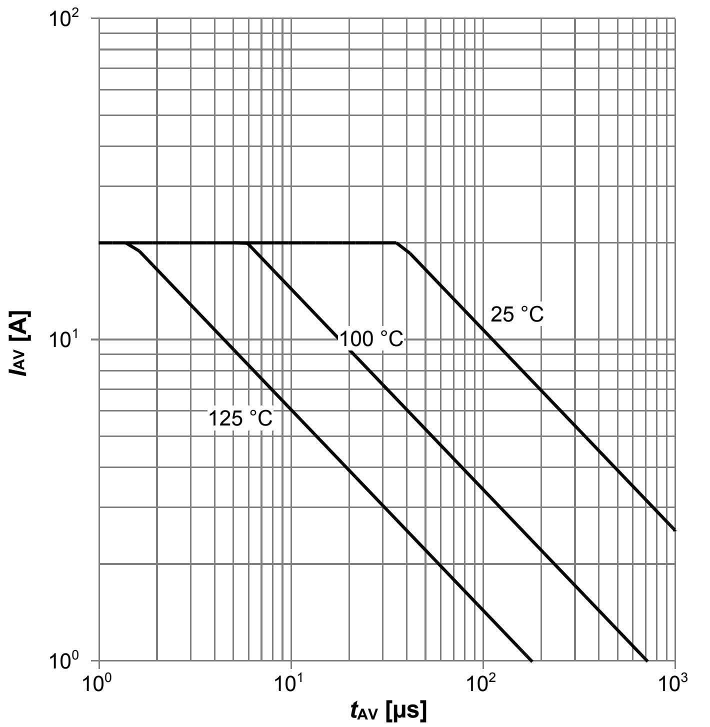
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



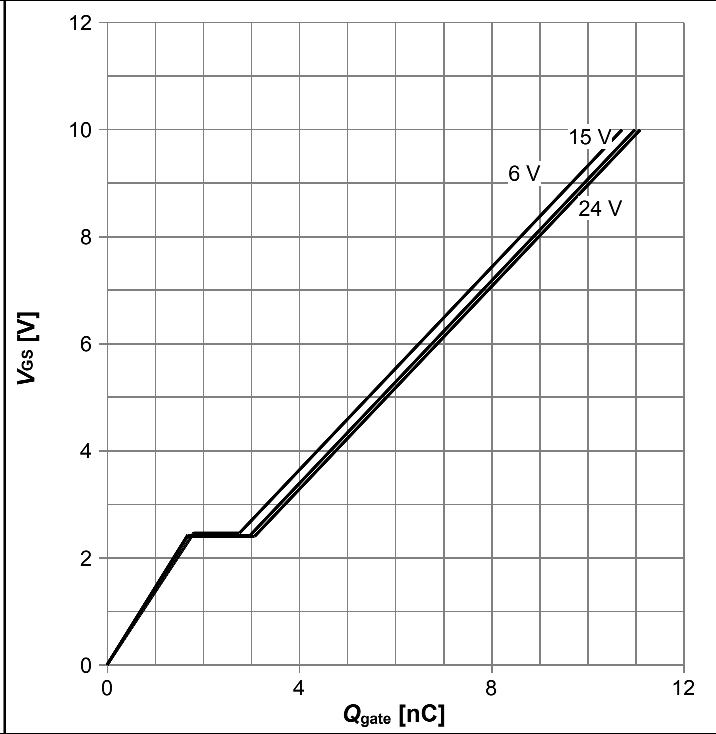
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



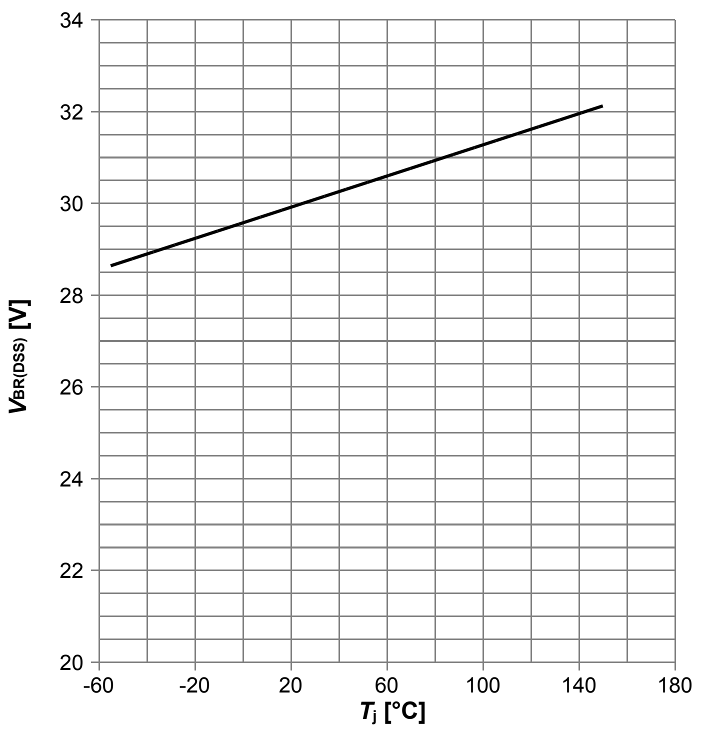
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



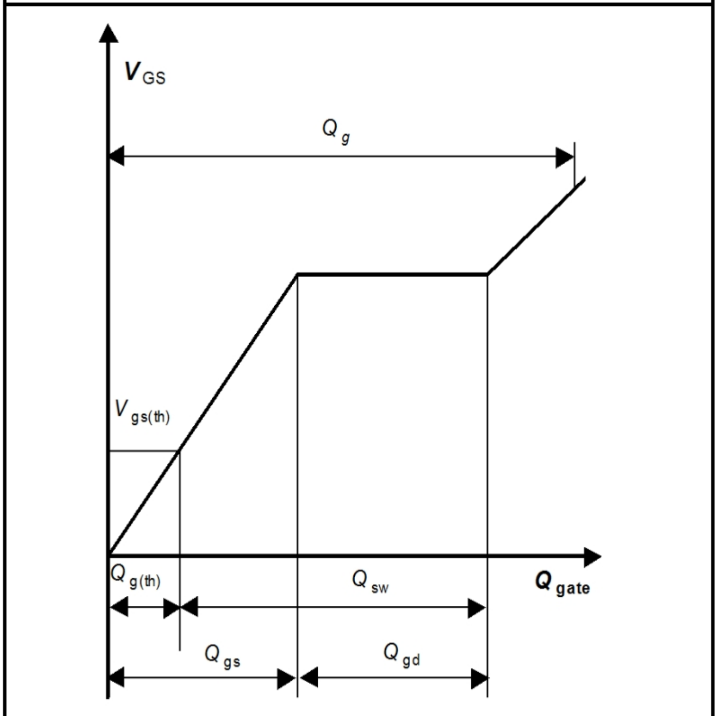
V_{GS}=f(Q_{gate}); I_D=8 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



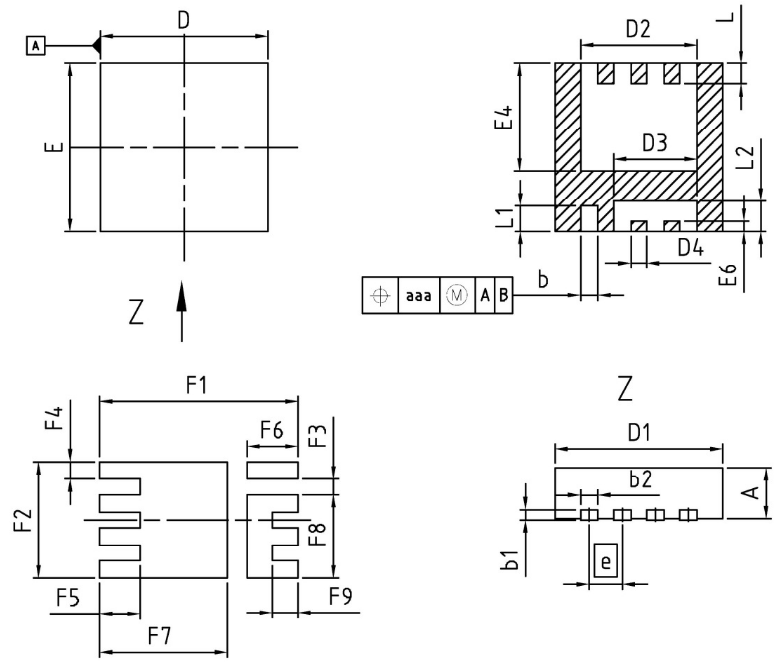
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



5 Package Outlines

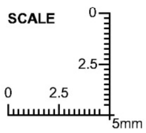
TSDSON-8 (fused Leads)



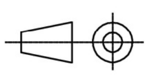
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

DOCUMENT NO.
Z8B00158553

SCALE



EUROPEAN PROJECTION



ISSUE DATE
27-12-2010

REVISION
02

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm/inches

Revision History

BSZ0589NS

Revision: 2016-07-11, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-11	Release of final version

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