ON Semiconductor

Test Procedure for the NCV8852GEVB Evaluation Board

Table 1: DEMONSTRATION BOARD TERMINALS

Pin Name	Function
VIN	Positive dc input voltage
VOUT	Regulated dc output voltage
GND	Common dc return
EN/SYNC	Enable input and external clock synchronization input

Table 2: ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

Rating	Value	Units
Dc supply voltage (VIN)	-0.3 to 36	V
Dc supply voltage (EN/SYNC)	-0.3 to 6.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3: ELECTRICAL CHARACTERISTICS

(T_A = 25°C, 6.0 V ≤ V_{IN} ≤ 36 V, $V_{EN/SYNC}$ = 5.0 V, 0 ≤ I_{OUT} ≤ 2.0 A, unless otherwise specified)

Characteristics	Conditions	Typical Value	Units
Regulation			
Output Voltage		5.0	V
Voltage Accuracy		2	%
Line Regulation	I_{OUT} = 1.0 A	0.04	%
Load Regulation	V_{IN} = 13.2 V	0.12	%
Switching			
Switching Frequency		170	kHz
Soft-start Time		2.0	ms
SYNC Frequency Range		170 to 500	kHz
Current Limit			
Average Current Limit		TBD	A
Cycle-by-cycle Current Limit		TBD	A
Protections			
Input Undervoltage Lockout (UVLO)	V_{IN} decreasing	TBD	V
Thermal Shutdown	T_J rising	170	°C

Operational Guidelines

1. Connect a dc input voltage, within the 6.0 V to 36 V range, between VIN and GND
2. Connect a load between VOUT and GND
3. Connect a dc enable voltage, within the 2.0 V to 5.5 V range, between EN/SYNC and GND
4. Optionally, for external clock synchronization, connect a pulse source between EN/SYNC and GND. The high state level should be within the 2.0 V to 5.5 V range, and the low state level within the 0.0 V to 0.8 V range, with a minimum pulse of TBD and a frequency within the 170 kHz to 500 kHz range.

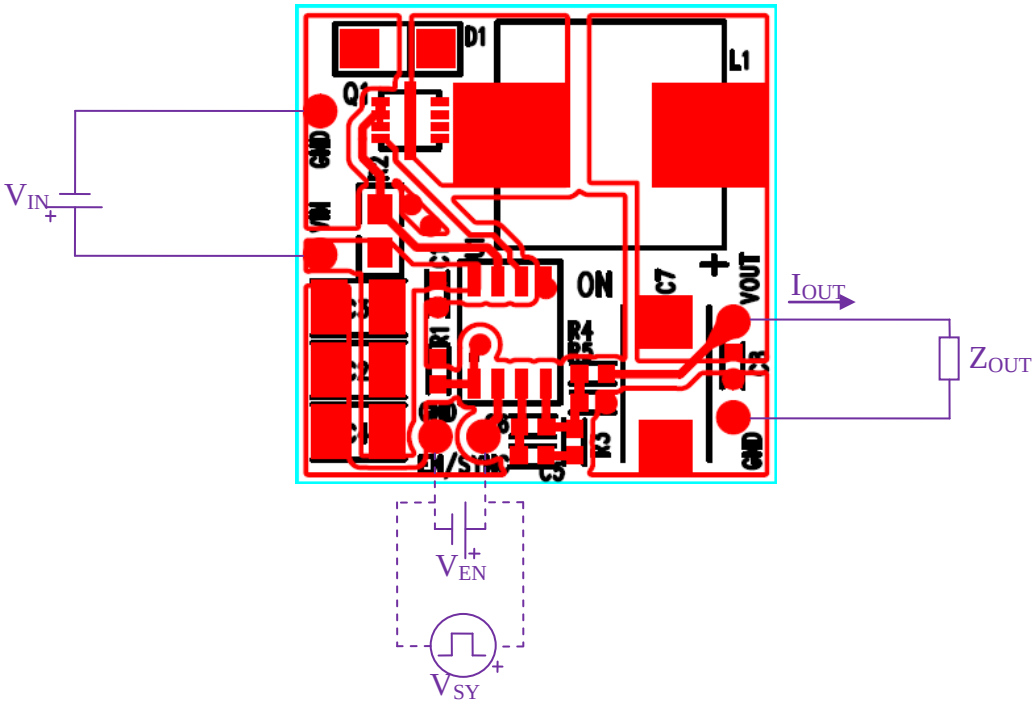

Figure 1: NCV8852EVB Board Connections

Typical Performance

Efficiency

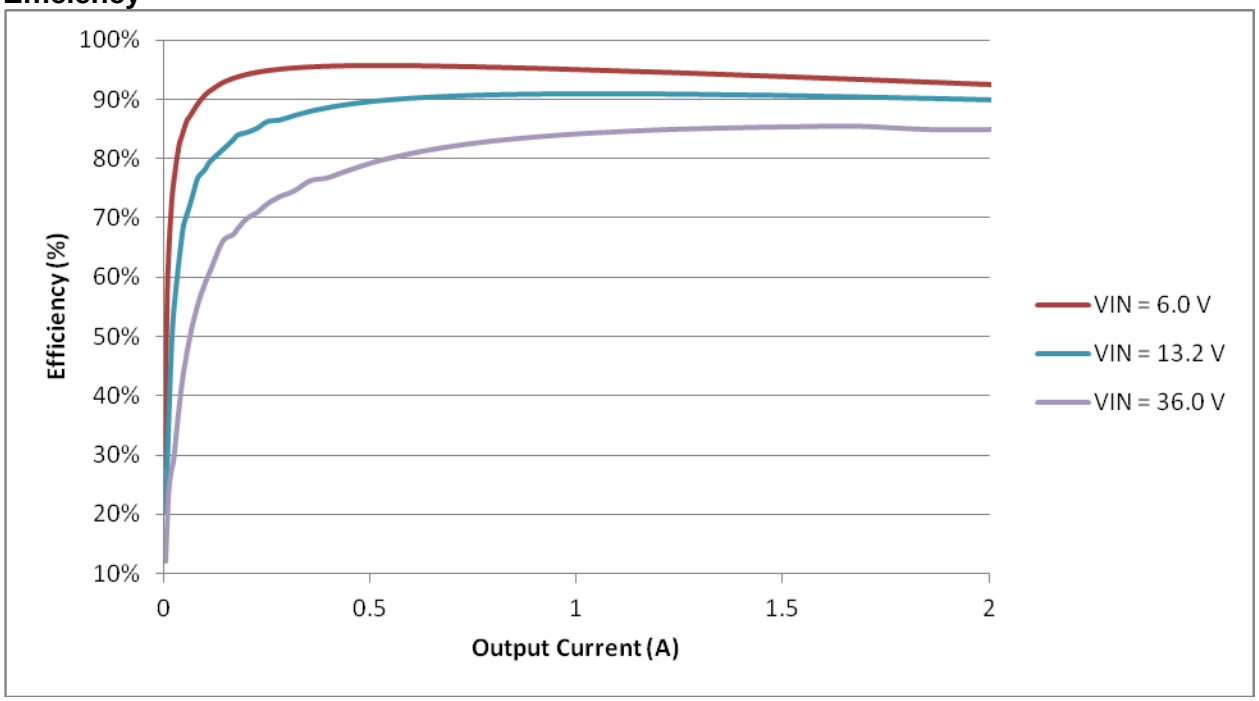

Figure 2: Efficiency at 170 kHz for a 5.0 V output

Regulation

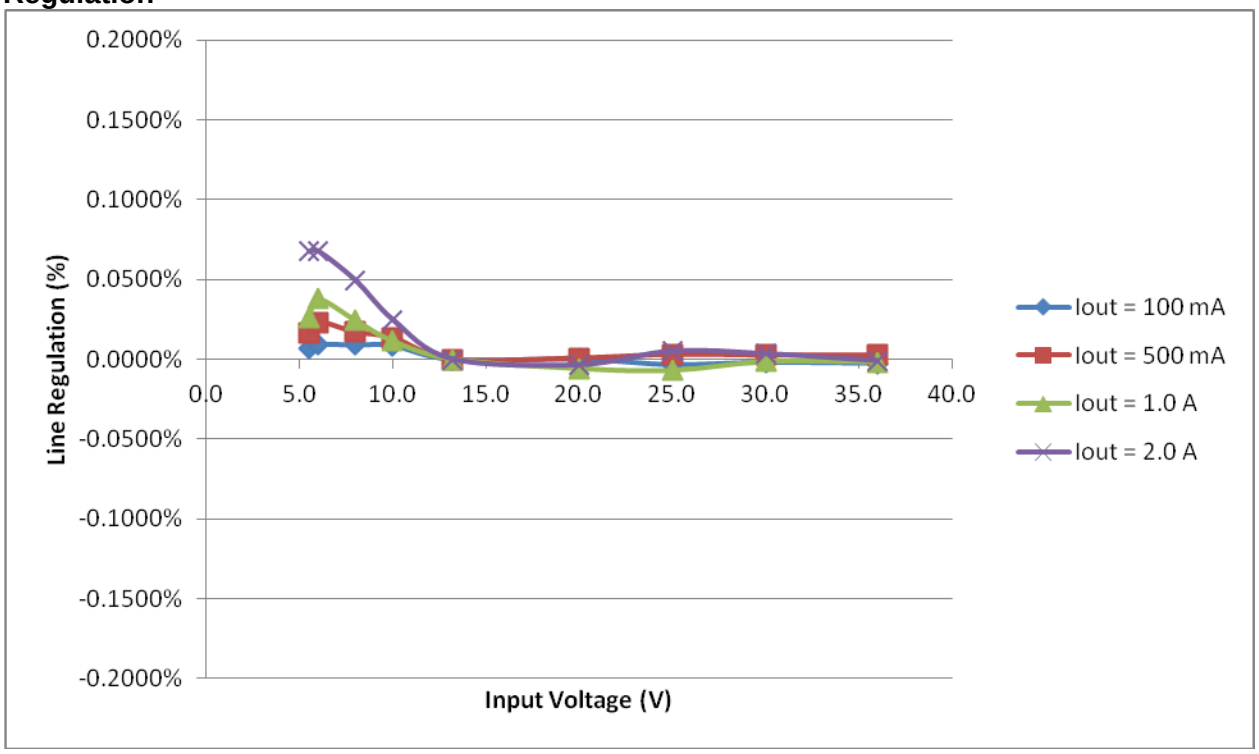

Figure 3: Line Regulation for 170 kHz and a 5.0 V output

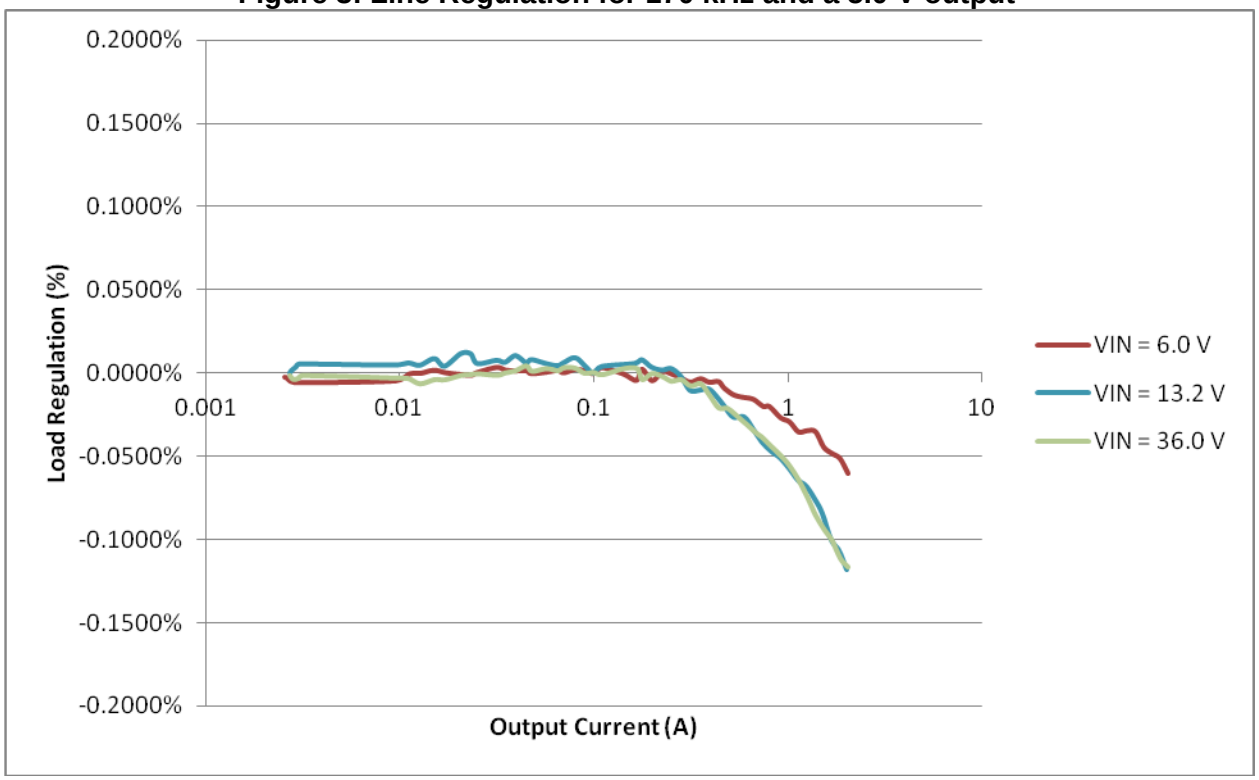

Figure 4: Load Regulation for 170 kHz and a 5.0 V output