EClamp2410PQ
ESD Protection Device for T-Flash/MicroSD Interfaces

PROTECTION PRODUCTS - EMIClamp®

Description

The EClamp®2410PQ is a combination EMI filter and line termination device with integrated TVS diodes for use on Multimedia Card interfaces. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for protection of **T-Flash/MicroSD interfaces** in cellular phones and other portable electronics.

The device consists of six circuits that include series impedance matching resistors and pull up resistors as required by the SD specification. TVS diodes are included on each line for ESD protection. An additional TVS diode connection is included for protection of the voltage (Vdd) bus. Termination resistor value of 45 Ohms is included on the DAT0, DAT1, DAT2, DAT3, CMD, and CLK lines. Pull up resistors of 15k Ohms are included on DAT0, DAT1, DAT2, and CMD lines while a 50k Ohm pull up is inlcuded on the DAT3 line. These may be configured for devices operating in SD or SPI mode . The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4. The EClamp2410PQ is in a 16-pin, RoHS/WEEE compliant, SLP4016P16 package. It measures 4.0 x 1.6 x 0.58mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPdAu. The EClamp2410PQ is qualified to AEC-Q100 Grade1 for Automotive use.

Features

- Bidirectional EMI/RFI filtering and line termination with integrated ESD protection
- ESD protection to IEC 61000-4-2 (ESD) Level 4, ±15kV (air), ±8kV (contact)
- TVS working voltage: 5V
- Termination Resistors: 45Ω
- Pull Up Resistors: 15kΩ (3 each) and 50kΩ
- Typical Capacitance per Line: 12pF (VR = 2.5V)
- Protection and termination for six lines + Vdd
- Solid-state technology
- AEC-Q100 Grade1 Qualified

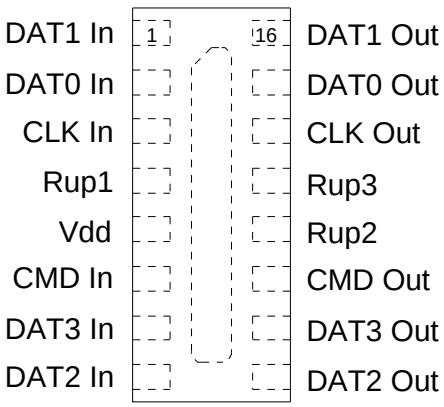
Mechanical Characteristics

- SLP4016P16 16-pin package
- RoHS/WEEE Compliant
- Nominal Dimensions: 4.0 x 1.6 x 0.58 mm
- Lead Pitch: 0.5mm
- Lead finish: NiPdAu
- Marking: Marking Code
- Packaging: Tape and Reel

Applications

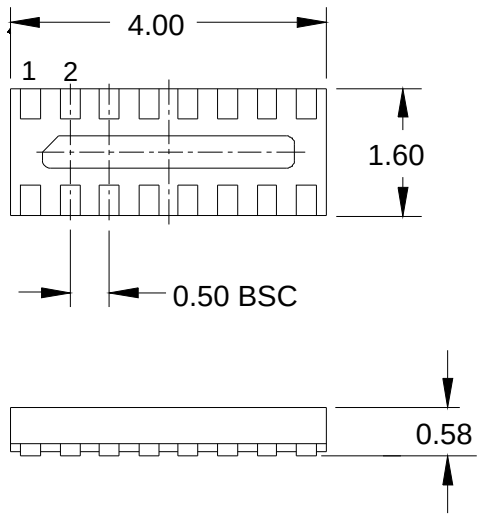
- T-Flash / MicroSD Interfaces
- MMC Interfaces
- CDMA, GSM, 3G Cell Phones
- Automotive Applications

Pin Configuration



Pin Designation (Top View)

Package Configuration



16 Pin SLP package (Bottom Side View)
Nominal Dimensions in mm

Absolute Maximum Ratings

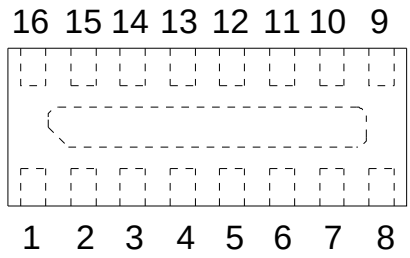
Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 17 +/- 12	kV
Junction Temperature	T_J	125	°C
Ambient Operating Temperature	T_A	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

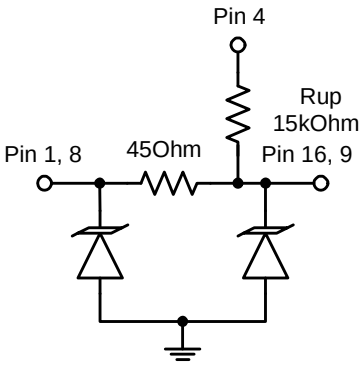
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
TVS Reverse Stand-Off Voltage	V_{RWM}					5	V
TVS Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	T_A = 25°C	6	8	10	V
			T_A = 125°C	6		10	
TVS Reverse Leakage Current	I_R	V_{RWM} = 3.0V	T_A = 25°C			0.5	µA
			T_A = 125°C			100	
Series Resistors	R	Each Line		38	45	52	Ohm
DAT Pull Up Resistor 1	R_{up1}			12	15	17	kOhm
DAT Pull Up Resistor 2	R_{up2}			42	50	58	kOhm
Total Capacitance	C_{in}	Input to Gnd, Each Line V_R = 2.5V, f = 1MHz	T_A = 25°C	10	12	15	pF
			T_A = 125°C		15	20	

Pin Identification and Configuration

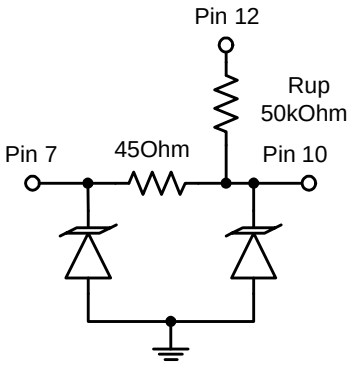
Pin	Symbol	Identification
1, 16	DAT1	Data line #1 input/output with pull-up resistor
2, 15	DAT0	Data line #0 Input/Output
3, 14	Clock	Clock line Input/Output
4	Rup1	15K Pull-up resistor from DAT1 & DAT2
5	Vdd	Power Supply ESD Protection
6, 11	CMD	Command Line Input/Output
7, 10	DAT3	Data line #3 input/output with pull-up resistor
8, 9	DAT2	Data line #2 input/output with pull-up resistor
12	Rup2	50K Pull-Up Resistor from DAT3
13	Rup3	VCC Circuit 3A
Center tab	GND	Ground connection



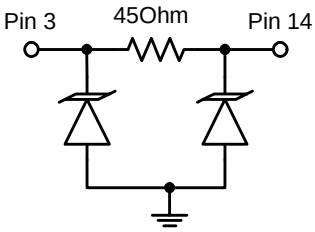
Schematics and Component Values



DAT1, DAT2

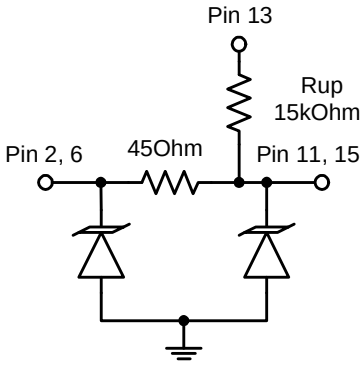


DAT3



CLK

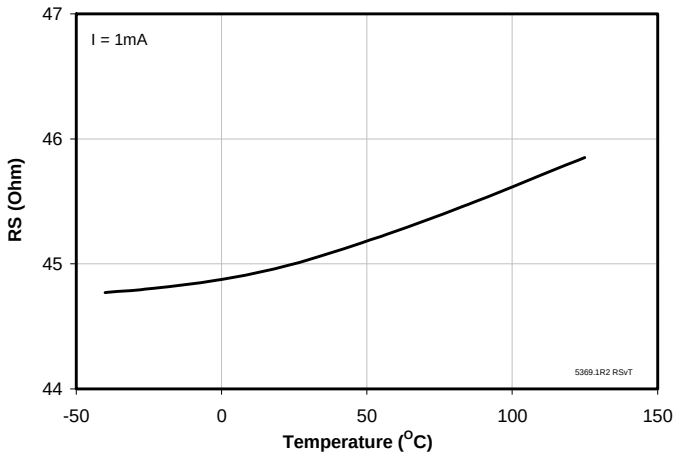
VDD



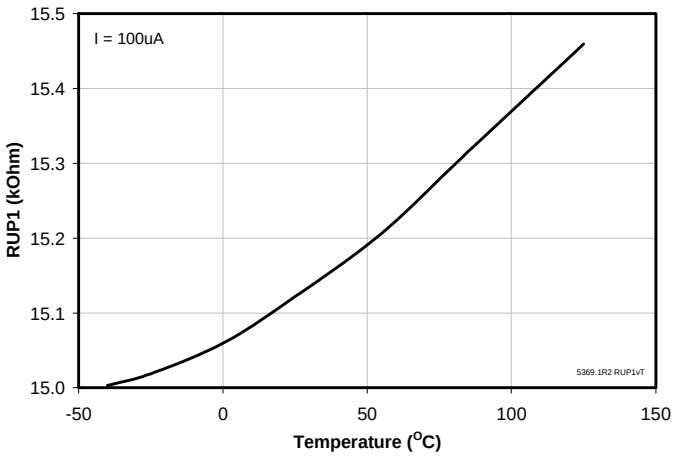
DAT0, CMD

Typical Characteristics

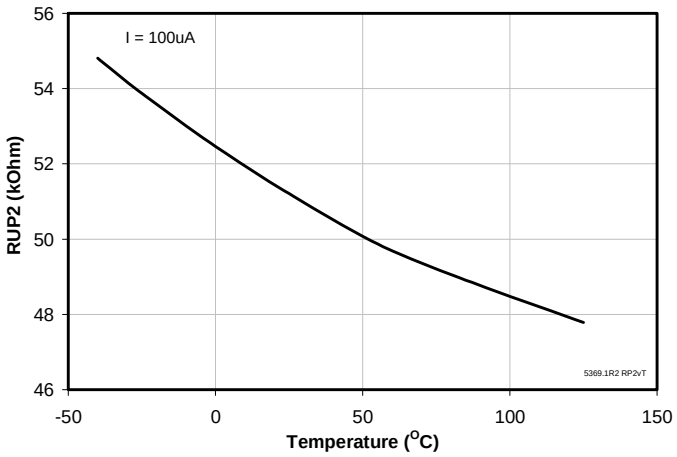
Series Resistance vs. Temperature



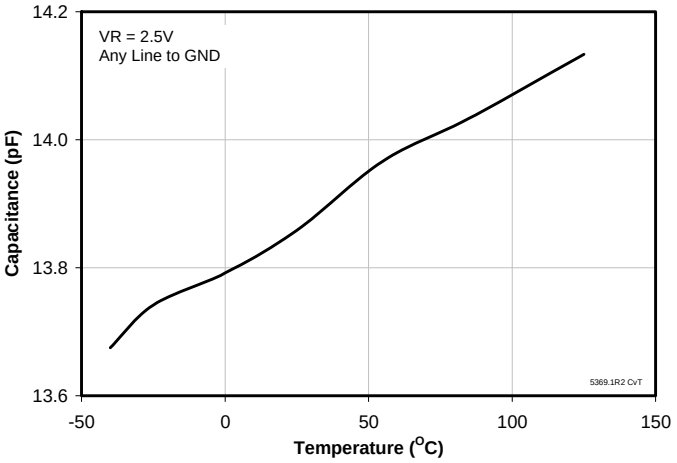
Pull Up Resistance (Rup1) vs. Temperature



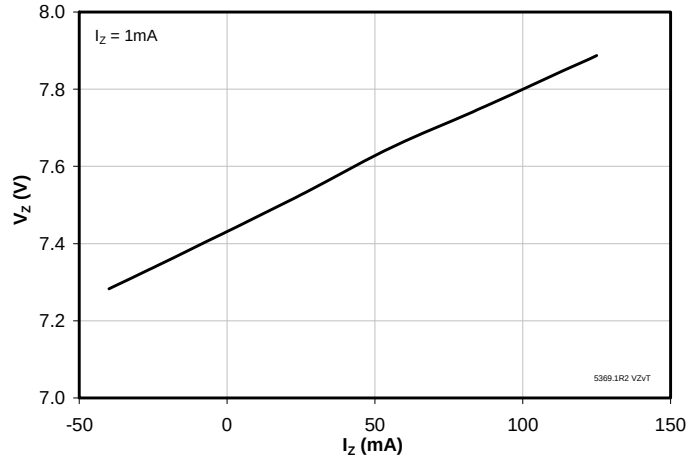
Pull Up Resistance (Rup2) vs. Temperature



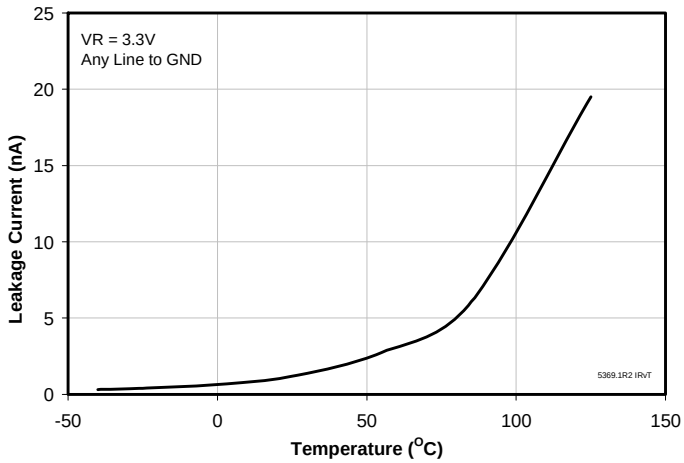
Capacitance vs. Temperature



Reverse Breakdown Voltage vs. Temperature

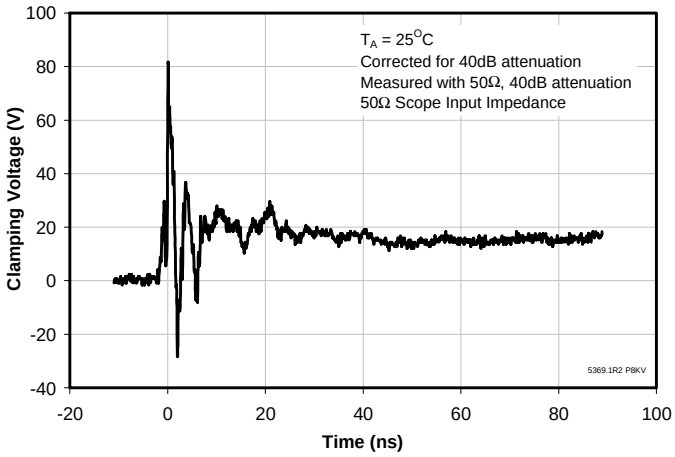


Reverse Leakage Current vs. Temperature

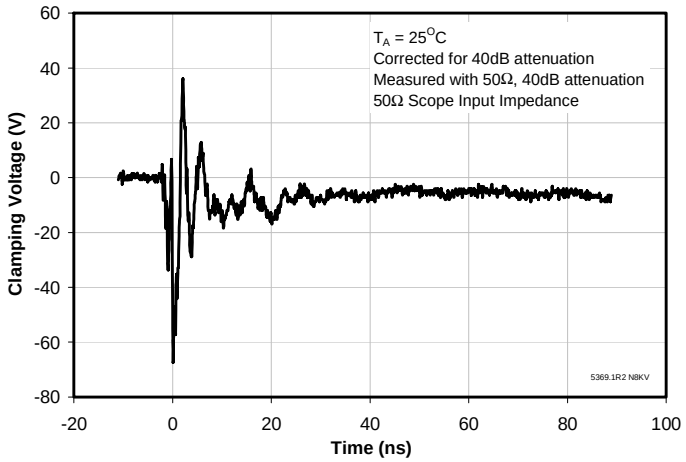


Typical Characteristics

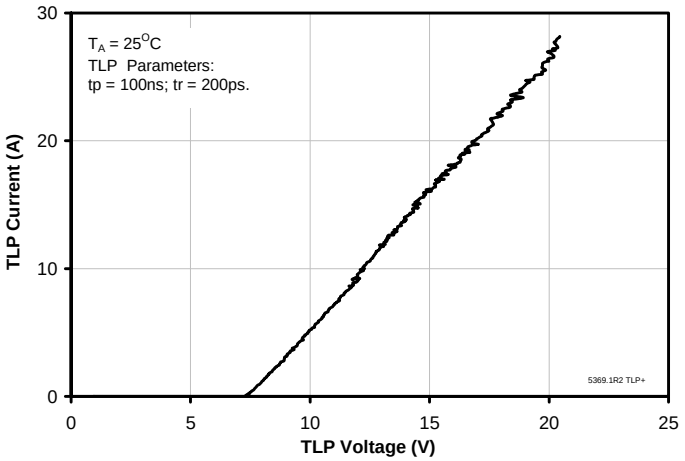
Positive ESD Clamping (8kV Contact per IEC 61000-4-2)



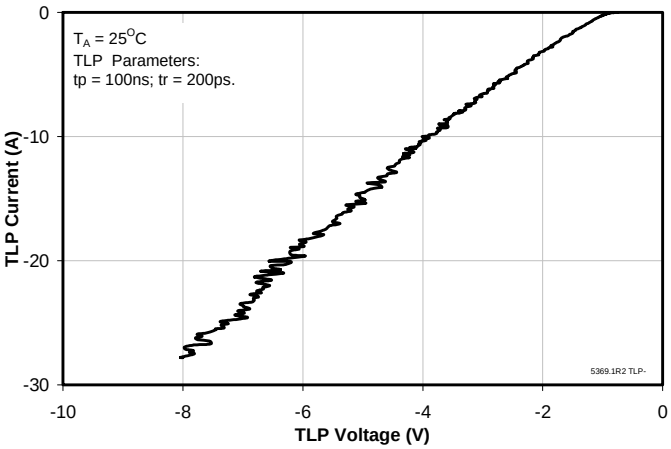
Negative ESD Clamping (8kV Contact per IEC 61000-4-2)



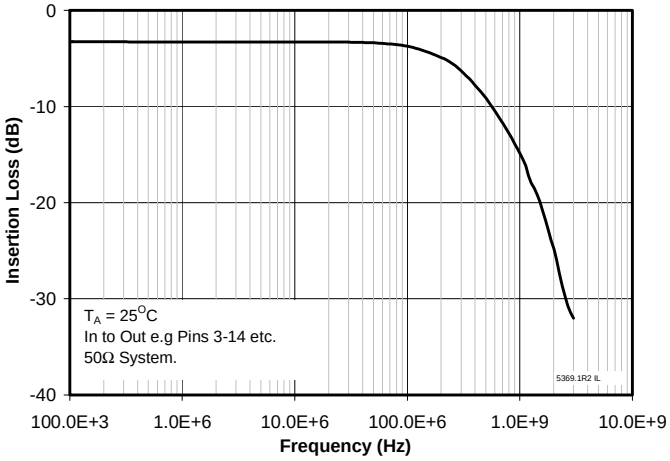
Positive TLP Plot



Negative TLP Plot



Insertion Loss S21 (Each Line)

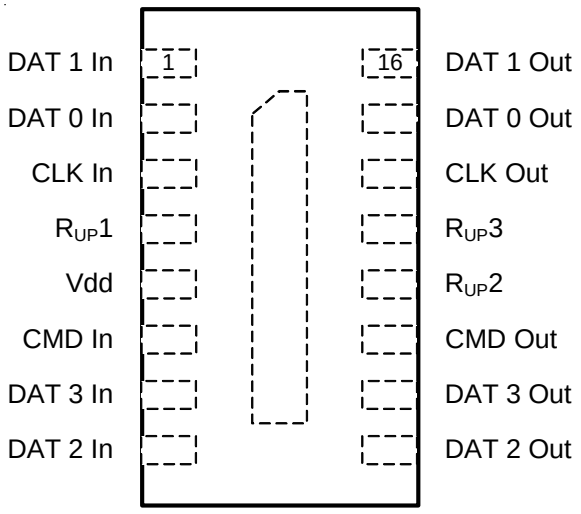


Applications Information

Device Connection

The EClamp2410PQ is a microSD/T-Flash interface device designed for use in cell phones and other portable electronic devices. The EClamp2410PQ is comprised of series and pull up resistors required on the microSD interface. Each line also includes TVS diodes for ESD protection. The device may be configured for SD or SPI mode operation. In SD mode for example, the 15k Ohm pull up resistors (Rup 1 and Rup 3) are connected to VDD. In SPI mode pin 4 is not connected (Rup 1) since these are reserved lines. The 50k Ohm pull up resistor is used for card detection or SPI mode selection during power up and is disconnected by the user during regular data transfer. The EClamp2410PQ is in a 16-pin SLP package. Electrical connection is made to the 16 pins located at the bottom of the device. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. A center tab serves as the ground connection. Recommendations for the ground connection are given below.

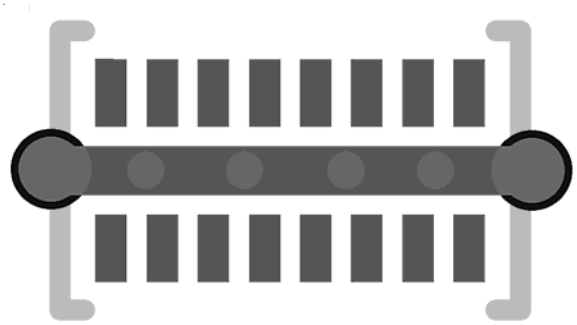
Figure 1 - Pin Identification and Configuration (Top Side View)



Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering and ESD performance of the device. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Figure 2 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance.

Figure 2 - Recommended Layout using Ground Vias



Layout Guidelines for Optimum ESD Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

1: Place the device as close to the connector as possible. This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.

2: The ESD transient return path to ground should be kept as short as possible. Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.

3: Avoid running critical signals near board edges.

Applications Information

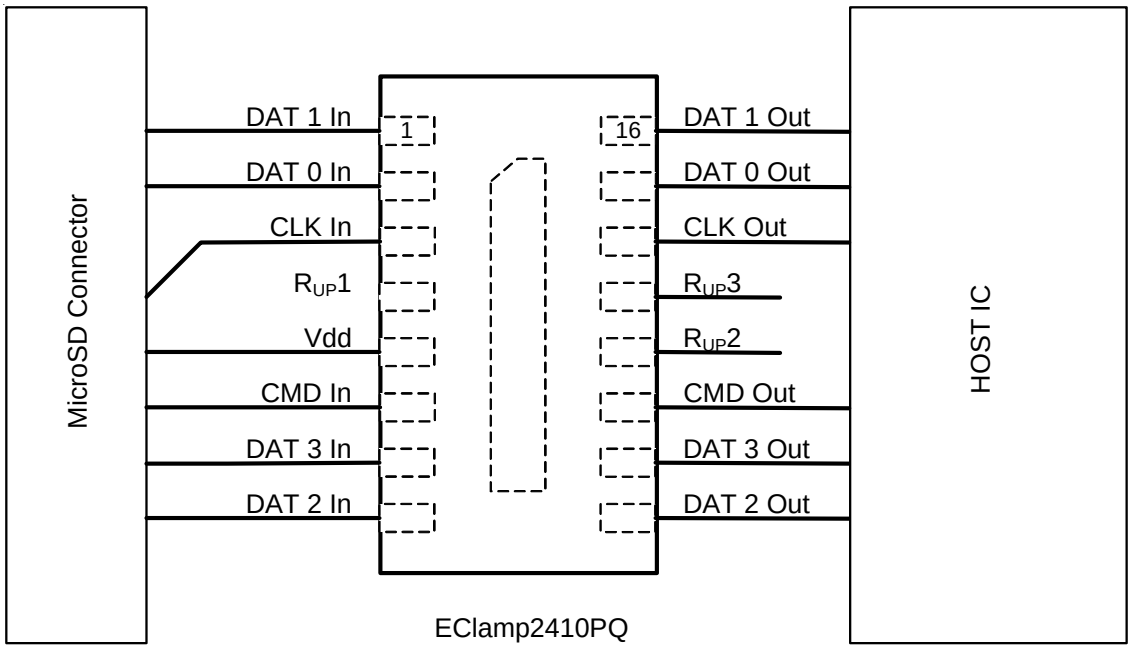
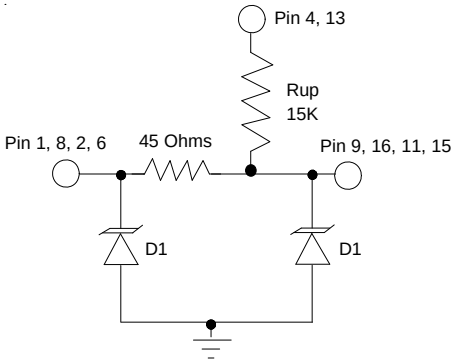
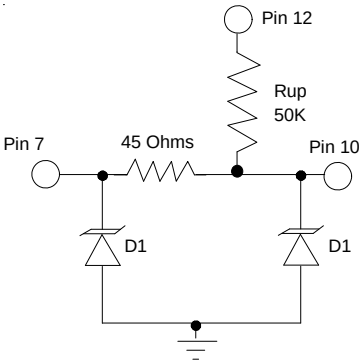


Figure 3 - MicroSD Protection

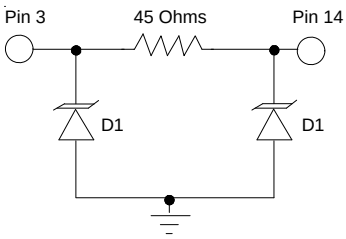
Applications Information - Spice Model



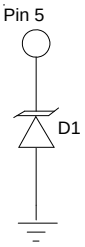
DAT1, DAT2, DAT0, CMD



DAT3



CLK

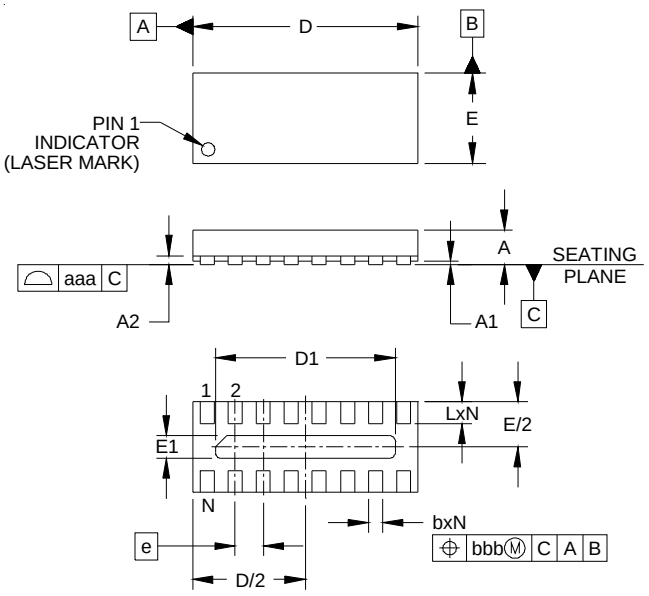


Vdd

EClamp2410PQ Spice Model

EClamp2410PQ Spice Parameters		
Parameter	**Unit**	**D1 (TVS)**
IS	Amp	2E-15
BV	Volt	7.46
VJ	Volt	0.777
RS	Ohm	1.00
IBV	Amp	1E-3
CJO	Farad	10E-12
TT	sec	2.541E-9
M	--	0.246
N	--	1.1
EG	eV	1.11

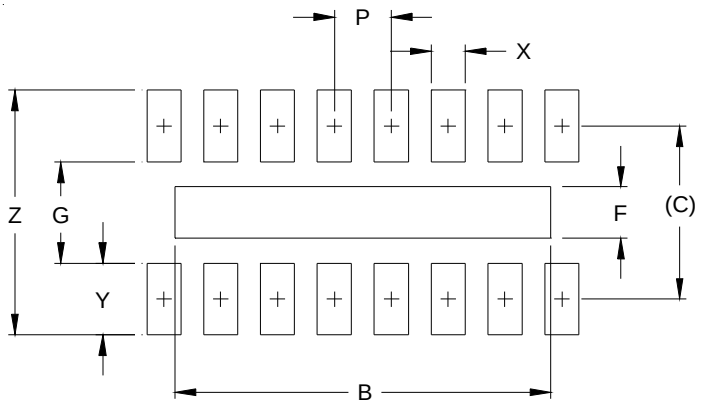
Outline Drawing - SLP4016P16



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	.023	.026	0.50	0.58	0.65
A1	.000	.001	.002	0.00	.003	0.05
A2		(.005)			(0.13)	
b	.007	.010	.012	0.20	0.25	0.30
D	.153	.157	.161	3.90	4.00	4.10
D1	.122	.126	.130	3.10	3.20	3.30
E	.059	.063	.067	1.50	1.60	1.70
E1	.010	.016	.020	0.25	0.40	0.50
e		.020 BSC			0.50 BSC	
L	.011	.013	.015	0.28	0.33	0.38
N		16			16	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

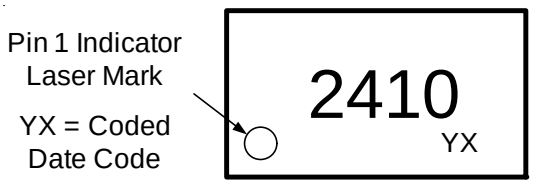
Land Pattern - SLP4016P16



DIMENSIONS		
DIM	INCHES	MILLIMETERS
B	.130	3.30
C	.060	1.52
F	.018	0.45
G	.035	0.89
P	.020	0.50
X	.012	0.30
Y	.025	0.63
Z	.085	2.15

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking

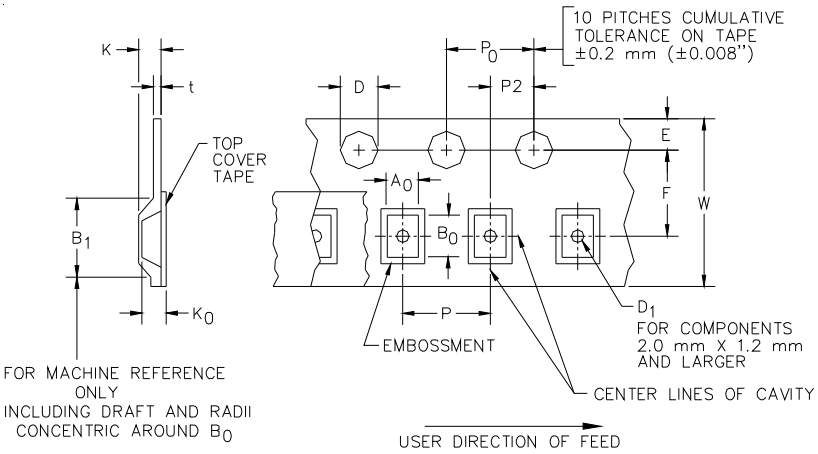


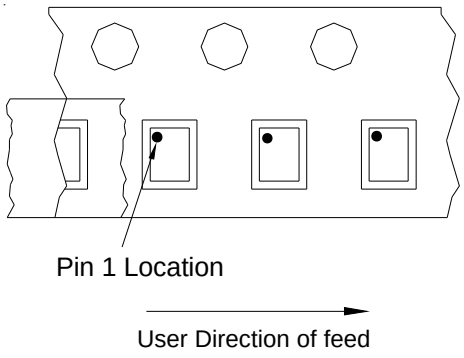
Ordering Information

Part Number	Qty per Reel	Reel Size
EClamp2410PQTCT	3000	7 Inch

EMIClamp and EClamp are marks of Semtech Corporation

Tape and Reel Specification





Device Orientation in Tape

A0	B0	K0
1.78 +/-0.10 mm	4.30 +/-0.10 mm	0.74 +/-0.10 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
12 mm	8.2 mm (.476)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	1.0 mm ±0.05 (.039)	1.750±.10 mm (.069±.004)	5.5±0.05 mm (.217±.002)	4.5 mm (.177)	4.0±0.1 mm (.157±.00-4)	4.0±0.1 mm (.157±.00-4)	2.0±0.05m-m (.079±.002)	0.4 mm (.016)	12.0 mm + 0.3 mm - 0.1 mm (.472±.012)

Contact Information

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