EVB-LAN9252-4PORT

EtherCAT® ESC Expansion Mode Evaluation Board User's Guide

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This declaration of conformity is issued by the manufacturer.

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Signed for and on behalf of Microchip Technology Inc. at Chandler, Arizona, USA

Derek Carlson
VP Development Tools

12-Sep-14
Date

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Preface

NOTICE TO CUSTOMERS

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Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9252-4PORT. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9252-4PORT as a development tool for the Microchip LAN9252 EtherCAT® slave controller. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9252-4PORT.
- **Chapter 2. "Board Details & Configuration"** – Includes details and instructions for using the EVB-LAN9252-4PORT.
- **Appendix A. "EVB-LAN9252-4PORT Evaluation Board"** – This appendix shows the EVB-LAN9252-4PORT.
- **Appendix B. "EVB-LAN9252-4PORT Evaluation Board Schematics"** – This appendix shows the EVB-LAN9252-4PORT schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9252-4PORT Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (November 2014)

- Initial Release of this Document.

Revision B (August 2015)

- Updated Figure 1-1.
- Updated Figure 2-2.
- Updated **Section 2.4.1 "Expansion Mode"**.
- Updated Table 2-7.
- Added **Section 2.4.2.5 "Copper and Fiber Mode Selections"** and all its subsections.

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9252 is a 2-port EtherCAT® slave controller with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver.

Each port receives an EtherCAT frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards the frames to the next logical port if there is either no link at a port, if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT Processing Unit (EPU). The loop settings can be controlled by the EtherCAT master.

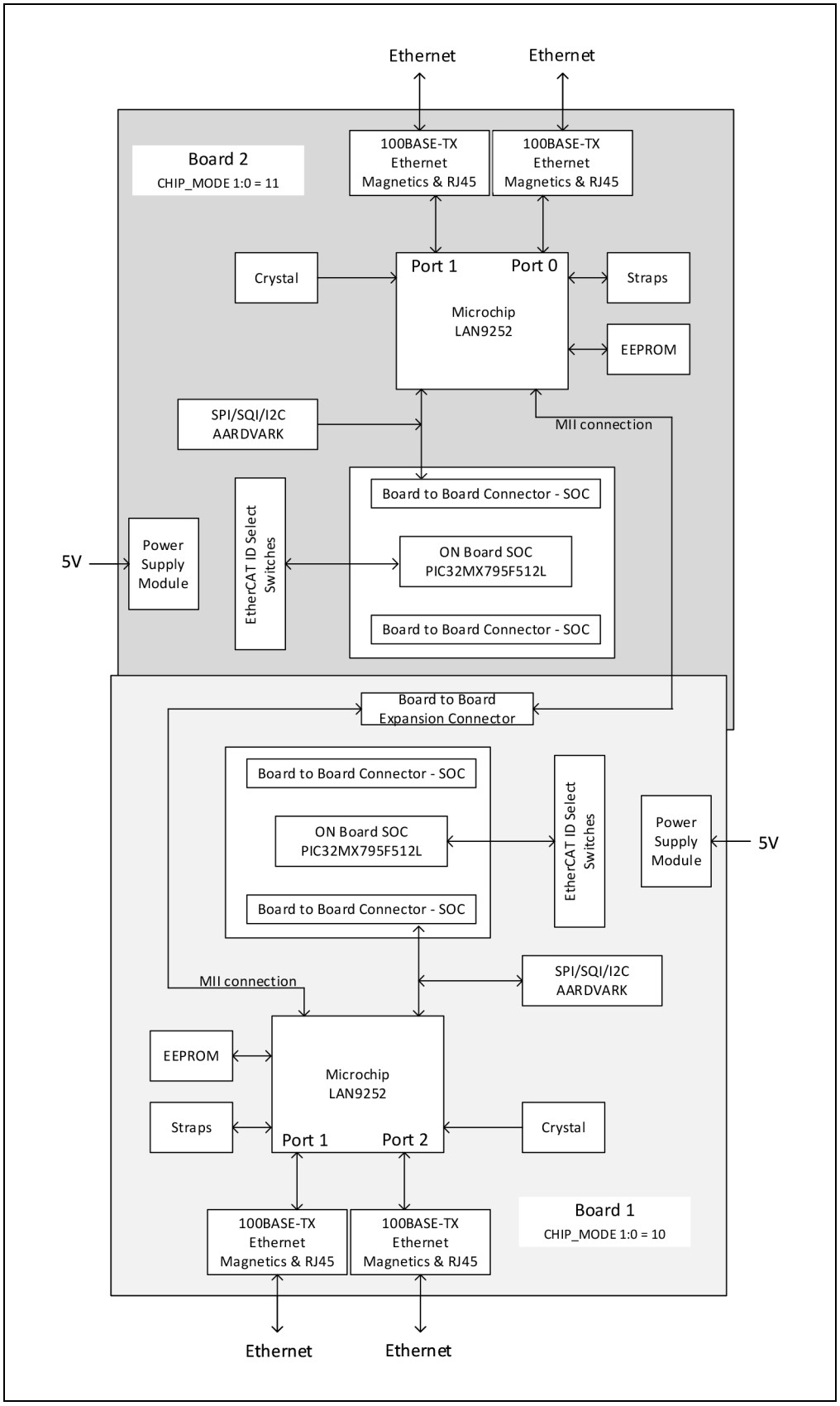
Packets are forwarded in the following order:

Port 0 -> EtherCAT Processing Unit -> Port 1 -> Port 2 -> Port 3.

The EtherCAT Processing Unit receives, analyzes and processes the EtherCAT data stream. The main purpose of the EtherCAT Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT master and from the local application. Data exchange between master and slave applications is comparable to a dual-ported memory (process memory), enhanced by special functions for consistency checking (SyncManager) and data mapping (FMMU). Each FMMU performs bitwise mapping of logical EtherCAT system addresses to physical device addresses.

The scope of this document is to describe the EVB-LAN9252-4PORT setup, which supports Expansion Mode and corresponding jumper configurations. The LAN9252 is connected to an RJ45 Ethernet jack with integrated magnetics for 100BASE-TX connectivity. A simplified block diagram of the EVB-LAN9252-4PORT is shown in Figure 1-1.

FIGURE 1-1: EVB-LAN9252-4PORT BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- LAN9252 Datasheet
- AN 8.13 Suggested Magnetics
- EVB-LAN9252-4PORT Schematics

NOTES:

Chapter 2. Board Details & Configuration

This section includes sub-sections on the following EVB-LAN9252-4PORT details:

- Power
- Reset
- Clock
- Configuration
- Mechanicals

2.1 POWER

2.1.1 +5V Power

Power is supplied to the EVB-LAN9252-4PORT by a +3.3V on-board regulator, which is powered by a +5V external wall adapter. The LAN9252 includes an internal +1.2V regulator which supplies power to the internal core logic. Assertion of the D1 Green LED indicates successful generation of +3.3V o/p. The SW1 switch must be in the ON position for the +5V to power the +3.3V regulator.

2.2 RESET

A power-on reset occurs whenever power is initially applied to the LAN9252 or if the power is removed and reapplied to the LAN9252. This event resets all circuitry within the LAN9252. After initial power-on, the LAN9252 can be reset by pressing the reset switch SW2. The reset LED D2 will assert (red) when the LAN9252 is in reset condition. For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.3 CLOCK

The EVB-LAN9252-4PORT utilizes an external 25Mhz 25ppm crystal from Cardinal Components Inc. (P/N: CSM1Z-A5B2C5-40-25.0D18-F).

2.4 CONFIGURATION

The following sub-sections describe the various board features and configuration settings.

2.4.1 Expansion Mode

Two EtherCAT slave controllers can be connected back-to-back using the MII interface, as shown in Figure 2-1. In this Expansion Mode, two EVB-LAN9252-4PORT boards (Board 1 and Board 2) are used as shown in Figure 2-2. Board 1 and Board 2 use identical PCBs, but have different bills of material. The timing of RX_DV and RXD with respect to RX_CLK has to be checked at both ESCs (LAN9252) to be compliant with the IEEE 802.3 requirements of min.10 ns setup time and min. 10 ns hold time. The timing can be adjusted by configuring the TX Shift settings of each ESC (LAN9252). These differences are detailed in the following subsections.

FIGURE 2-1: BACK-TO-BACK CONNECTION VIA MII

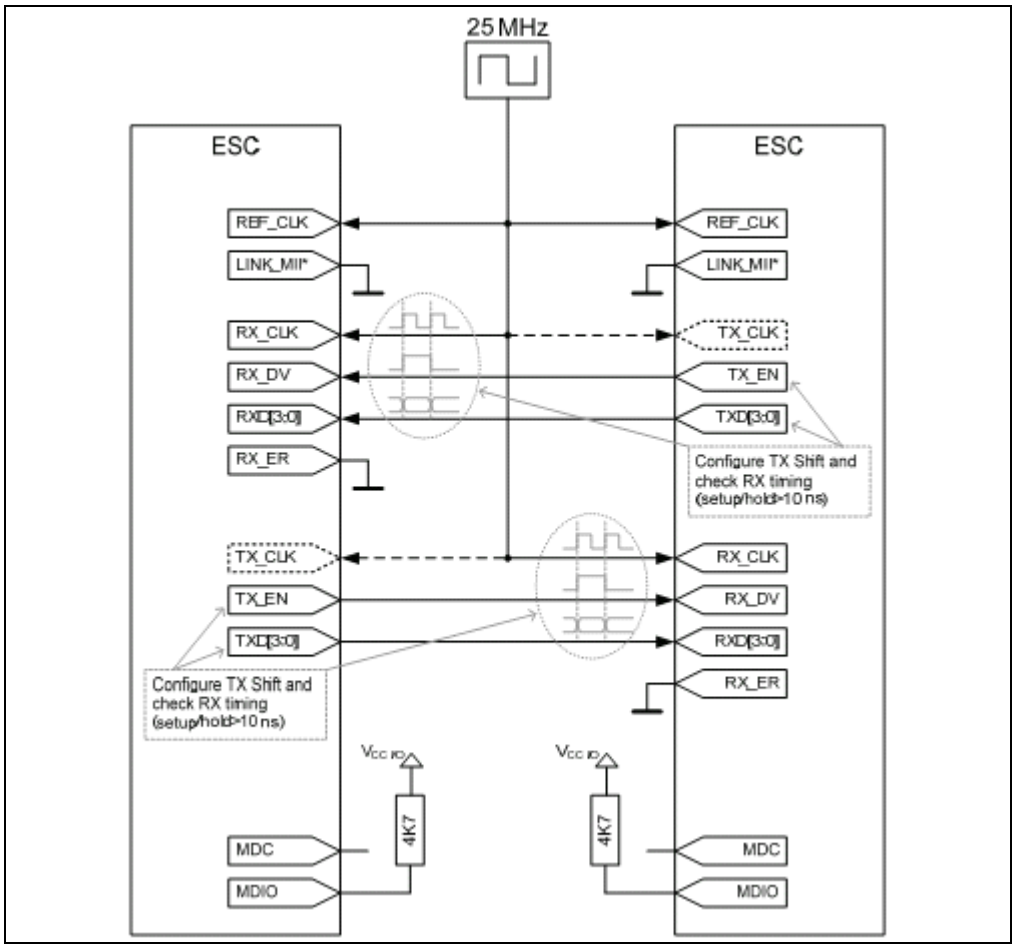
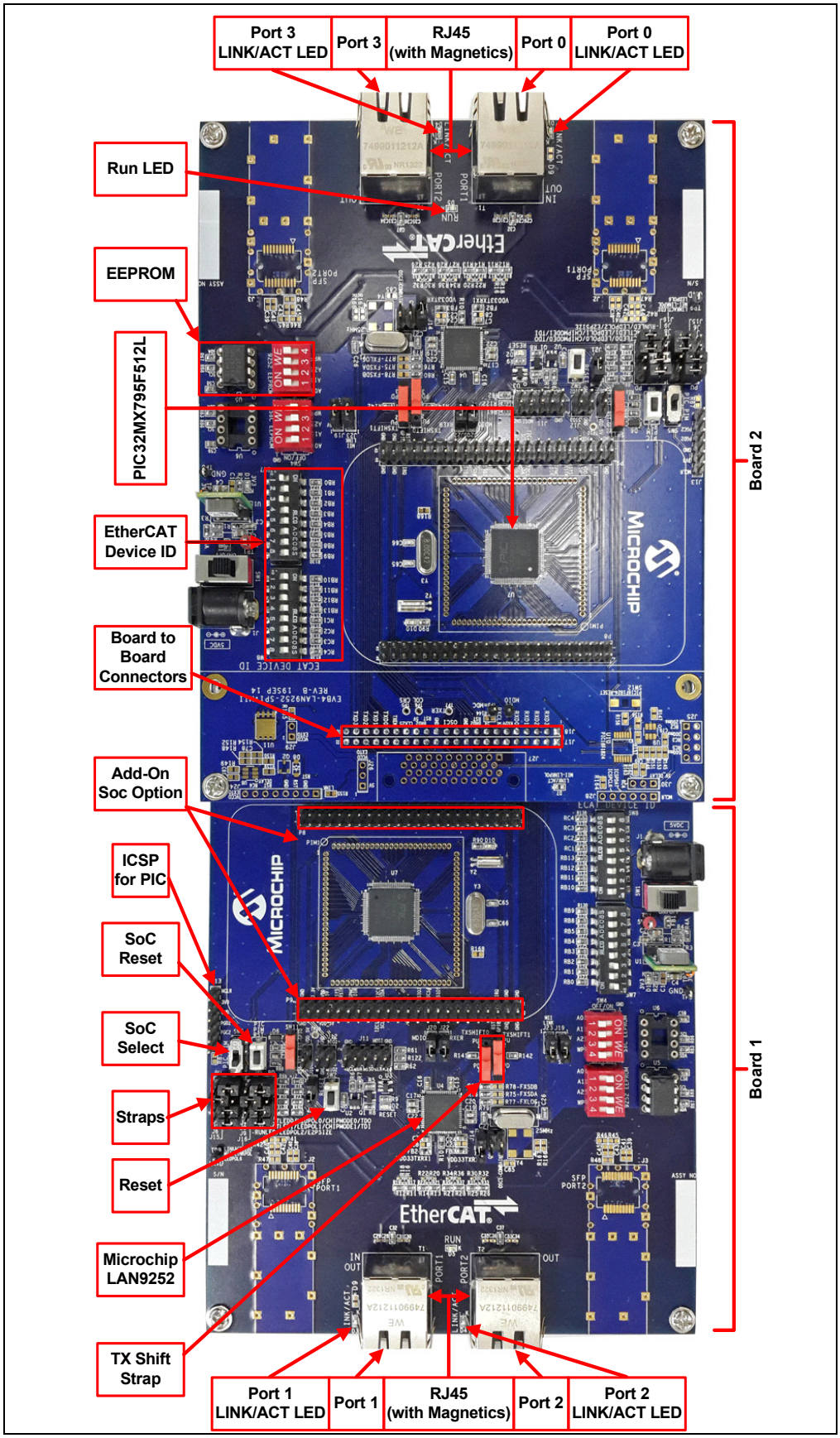


FIGURE 2-2: EVB-LAN9252-4PORT TOP VIEW WITH CALLOUTS



2.4.1.1 BOARD ASSEMBLY

J17 and J18 are used to stack the boards. On Board 1, thru-hole Berg stick headers (gold plated 2.54mm) are placed on the top side of the PCB. On Board 2, thru-hole Berg stick sockets (gold plated 2.54mm) are placed on the bottom side of the PCB. To use these boards in Expansion Mode, Board 2 must be stacked on top of Board 2 via J17 and J18 (see Figure 2-2 and Table 2-1).

TABLE 2-1: EXPANSION MODE JUMPERS J17 & J18

Jumper	Board 1	Board 2
J17 & J18	Thru-hole Berg stick headers on top side	Thru-hole Berg stick sockets on bottom side

2.4.1.2 JUMPER SETTINGS

The default jumpers settings for Board 1 and Board 2 are shown in Table 2-2.

TABLE 2-2: DEFAULT JUMPER SETTINGS

Jumper	Board 1 (Short)	Board 2 (Short)	Signal
J14	1-2	1-2	CLK (25 MHz)
J4 & J7	2-3	1-2	CHIPMODE0
J5 & J8	1-2	1-2	CHIPMODE1
J6 & J9	2-3	2-3	RUNLED
J15 & J16	2-3	2-3	MII_LINKPOL
J19	1-2	1-2	5V
J20	1-2	1-2	MII_MDIO
J21	1-2	1-2	RESET
J22	1-2	1-2	MII_RXER
J23	1-2	1-2	MII_LINK

2.4.1.3 CLOCK, POWER, RESET CONFIGURATIONS

In Expansion Mode, there are two different sub-modes available:

- **Separate Mode (Default):** The LAN9252 clock on each board is provided separately (P/N: CSM1Z-A5B2C5-40-25.0D18-F). Power and reset are common for this setup.
- **Combined Mode:** The LAN9252 clock on each board is provided via a single 25MHz oscillator (P/N: CB3LV-3C-25M0000). To enable Combined Mode, the J14 jumpers must be configured as shown in Table 2-3.

TABLE 2-3: J14 COMBINED MODE JUMPER SETTINGS

Jumper	Board 1 (Short)	Board 2 (Short)
J14	3-4 & 5-6	5-6

2.4.2 Strap Options

The following LAN9252 strap options are available.

2.4.2.1 CHIP MODE SELECTION

Table 2-4 details the LAN9252 chip mode configuration straps.

TABLE 2-4: CHIP MODE CONFIGURATION STRAP

Jumper	Board 1 (Short)	Board 2 (Short)	Mode
J4 & J7	2-3	1-2	3-port downstream mode
J5 & J8	1-2	1-2	3-port upstream mode

Note: For proper operation, Board 1 must be in 3-port downstream mode and Board 2 must be in 3-port upstream mode. This requires J4, J5, J7, and J8 to be configured as shown in Table 2-4. All other configurations are not supported.

2.4.2.2 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (J6 & J9) determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512. Table 2-5 details the LAN9252 chip mode configuration straps.

TABLE 2-5: EEPROM SIZE CONFIGURATION STRAP

Header	Description	Pins	Settings
J6, J9	EEPROM size configuration strap inputs. This strap determines the supported EEPROM size range.	1-2 2-3	Short 1-2 for high (pull-up) (default) Short 2-3 for low (pull-down)

2.4.2.3 MII_LINKPOL

This strap determines the polarity of the MII_LINK pin. On the EVB-LAN9252-4PORT it is tied low. In this mode MII_LINK low equates to “100/Mbit/s Full-Duplex Link is Established”.

2.4.2.4 TX SHIFT STRAPS

The EtherCAT MII Port TX Timing Shift straps determine the value of the MII TX timing shift. The SW9 and SW10 switches are used to determine the TX Shift straps as detailed in Table 2-6 and Table 2-7.

TABLE 2-6: TX_SHIFT DEFINITIONS

TX_SHIFT1	TX_SHIFT0	TX Timing Shift (ns)
0	0	20
0	1	30 (Default)
1	0	0
1	1	10

TABLE 2-7: SW9 & SW10 SETTINGS

Switch	Short Pins	Switch Knob Position
SW9 (TX_SHIFT0=1)	1-2	Down
SW10 (TX_SHIFT=0)	1-3	Up

Note: For switch P/N: 450301014042, pin 1 is at the middle of the switch. To short 1-2, knob position must be in the 1-3 position, and vice versa.

2.4.2.5 COPPER AND FIBER MODE SELECTIONS

The LAN9252 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) in SFP mode. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must to be configured.

Note: Vendor part number for SFP Transceiver: Finisar/FTLF1217P2.

2.4.2.5.1 Copper Mode

The EVB-LAN9252 is set to Copper Mode by default. Table 2-8 details the required strap resistors settings for Copper Mode operation.

TABLE 2-8: COPPER MODE STRAP RESISTORS

Resistors	Signal Names	Description
R79 (10K)	FXLOSEN	Copper twisted pair for ports A and B further determined by FXSDENA and FXSDENB
R76, R80 (10K)	FXSDA/FXSDB	Configures Port 0 and Port 1 to Copper Mode

Note: R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-9 must be assembled for Copper Mode operation.

TABLE 2-9: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19,R21, R23	Port 0 Copper mode is Enabled
R31, R33, R35, R37	Port 1 Copper mode is Enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

2.4.2.5.2 Fiber Mode

The LAN9252 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resisters must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (see Section 2.4.2.5.1 “Copper Mode”).

Table 2-10 details the required strap resistor settings for Fiber Mode operation

TABLE 2-10: FIBER MODE STRAP RESISTORS

Resistors	Description
R77 (10K)	Configures Port 0 & 1 to FX_LOS Mode
R75, R78 (10K)	Configures Port 0 & 1 to Fiber mode, respectively

Note: R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-11 must be assembled for Fiber Mode operation

TABLE 2-11: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19,R21, R23	Port 0 Copper mode is Enabled
R31, R33, R35, R37	Port 1 Copper mode is Enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

2.4.2.5.3 FX-LOS Fiber Mode Strap

FX-LOS strap details are shown in Table 2-12. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 2-12: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port 1
Populate	Populate	1.5	A level of 1.5V selects FX-LOS for Port 0 and FX-SD / Copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / Copper twisted pair for Ports 0 and 1, further determined by FXSDA, FXSDB

Note: The above strap details describe the LAN9252 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

2.4.3 LED Indicators

The D3, D4, and D9 LEDs are used to indicate the Link/Activity status on the corresponding EVB ports, as detailed in Table 2-13. The Link/Act LED should be ON at each port. If the Link/Act LED is not ON, it indicates there is an issue with the connection or cable.

TABLE 2-13: D3 AND D4 LINK/ACTIVITY LED STATUS INDICATORS

State	Description
Off	Link is down
Flashing Green	Link is up with activity
Steady Green	Link is up with no activity

Additionally, the D5 LED is used as a RUN indicator (green) to shows the status of the EtherCAT State Machine (ESM), as detailed in Table 2-14.

TABLE 2-14: D5 RUN LED STATUS INDICATOR

State	Description
Off	The device is in the INITIALIZATION state
Blinking (on 200ms, off 200ms)	The device is in the PRE-OPERATIONAL state
Single Flash (on 200ms, off 1000ms)	The device is in the SAFE-OPERATIONAL state
On	The device is in the OPERATIONAL state
Flickering (on 50ms, off 50ms)	The device is booting and has not yet entered the INITIALIZATION state, or the device is in the BOOTSTRAP state and firmware download is in progress. (Optional. Off when not implemented.)

Table 2-15 details which LEDs are populated on Board 1 and Board 2 (Expansion Mode).

TABLE 2-15: BOARD 1 & BOARD 2 LED POPULATION LIST

LED	Board 1	Board 2	Signal	Color
D1	Populated	Populated	3V3	Green
D2	Populated	Populated	RESET	Red

TABLE 2-15: BOARD 1 & BOARD 2 LED POPULATION LIST (CONTINUED)

LED	Board 1	Board 2	Signal	Color
D3	Populated	Not Populated	LINK/ACT (Port 0)	Green
D4	Populated	Populated	LINK/ACT (Port 1 on Board 1, Port 4 on Board 2)	Green
D5	Populated	Populated	RUNLED	Green
D7	Not Populated	Not Populated	MII LINK	Green
D9	Not Populated	Populated	LINK/ACT (Port 3)	Green
D10	Populated	Populated	ERROR LED	Green

2.4.4 EEPROM Switch

The EVB-LAN9252-4PORT utilizes 0x50 (7-bit) I^2C slave addressing. The SW3 switch can be used to select the A0, A1, and A2 address bits, as shown in Figure 2-3 and Table 2-16. The eighth bit of the slave address determines if the master device wants to read or write to the 24FC512.

FIGURE 2-3: SLAVE ADDRESS ALLOCATION

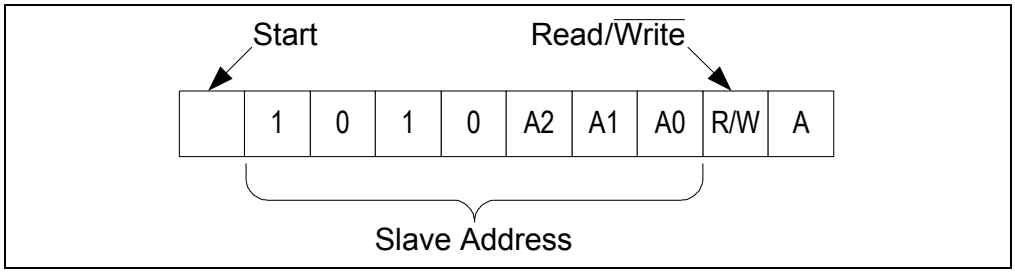


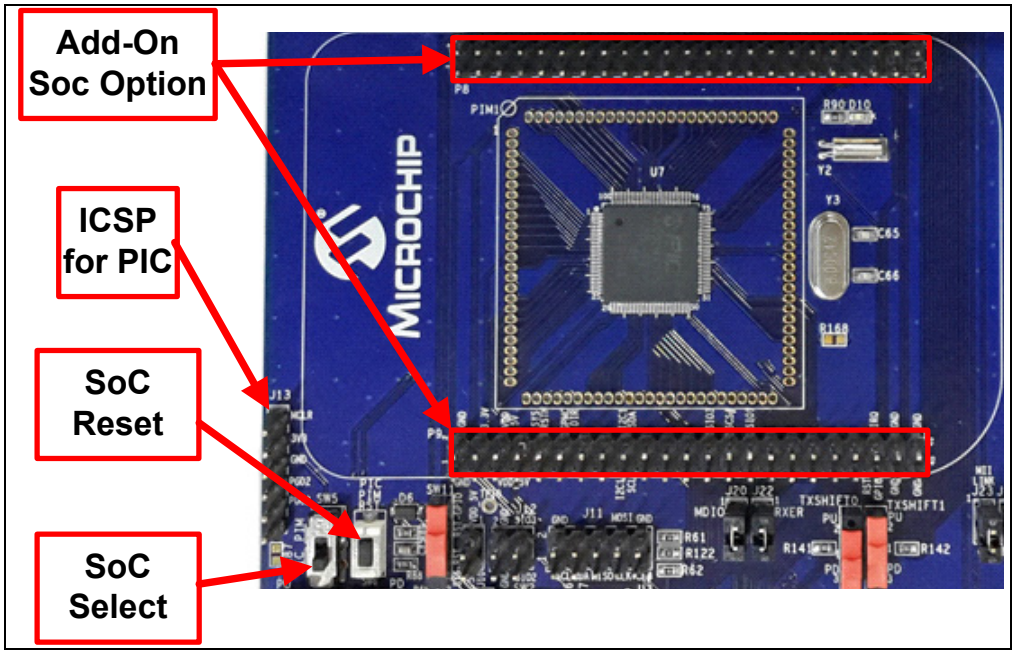
TABLE 2-16: EEPROM SWITCH

Switch	Description	Settings
SW3	I^2C EEPROM address selection switch (A0, A1, A2). See Figure 2-3.	ON for logic 0 (default) OFF for logic 1

2.4.5 SoC

The EVB-LAN9252-4PORT supports both an on-board SoC and add-on SoC. By default, the on-board SoC is enabled. However, an external add-on SoC can be connected via the add-on SoC headers. The SoC selection is configured via the SW5 switch, as detailed in the following subsections.

FIGURE 2-4: EVB-LAN9252-4PORT SOC SECTION



2.4.5.1 ON-BOARD SOC/PIC

By default, the on-board Microchip PIC32MX795F512L (U7) is used as the default SoC, which supports SPI.

2.4.5.1.1 Reset

SW6 is used to reset the on-board PIC. Additionally, when the LAN9252 is reset, it also forces the PIC into a reset state. For stability, a delay of approximately 180ms is added from the 3.3V o/p to reset release.

2.4.5.1.2 PIC Selection

The SW5 switch selects the enabled SoC. The SW5 switch knob position must be down to select the on-board PIC. If the switch knob position is up, then the on-board PIC is always in the reset state. Whenever an add-on board/SoC is used, the switch knob must be in the up position.

TABLE 2-17: SOC SELECTION

Switch	Position	Settings
SW5	Down	On-board PIC enabled
SW5	Up	Add-on board/SoC enabled

2.4.5.1.3 ICSP Header

SoC programing is performed using the ICSP header J13. Table 2-18 details the ICSP header pinout

TABLE 2-18: J13 ICSP HEADER PINOUT

J13 Pin	Settings
1	MLCR
2	3V3
3	GND
4	PGD2
5	PGC2

TABLE 2-18: J13 ICSP HEADER PINOUT (CONTINUED)

J13 Pin	Settings
6	NC

2.4.5.1.4 SoC EEPROM

The EVB-LAN9252-4PORT provides an optional SoC EEPROM. TI based SoCs require an EEPROM. However, the PIC on-board SoC and PIC based add-on SoC boards do not require this EEPROM.

2.4.5.2 ADD-ON SOC

An add-on board can be attached to the EVB-LAN9252-4PORT to use an add-on SoC. The add-on board must be mounted to the P8 and P9 connectors (2x23, 100mil normal gold plated Berg stick). The SW5 switch must be in the up position when using an add-on SoC. Additionally, the J10 2-pin jumper must be shorted to route power to the add-on board.

2.4.5.3 ID SELECT

The signals shown in Table 2-19 are used for ID selection. Switches SW7, SW8 and respective pull-up resistors are used to configure the ID select signals high or low. By default, the EtherCAT Device ID value is set to 5. To achieve this, ID0 and ID2 must be high while the remaining ID select signals (ID1 and ID3 through ID15) must be low.

Signals are high via the pull-up resistors. When required, setting the respective switch knob to the on position will change the ID select signal to low.

TABLE 2-19: ID SELECT SIGNALS

ID Selection Signal	Signal Name	PIC Pin Number	Switch Pin Number	Reference Designator
ID0	ID_SELECT_RB0	25	SW7.1	R123
ID1	ID_SELECT_RB1	24	SW7.2	R124
ID2	ID_SELECT_RB2	23	SW7.3	R126
ID3	ID_SELECT_RB3	22	SW7.4	R125
ID4	ID_SELECT_RB4	21	SW7.5	R127
ID5	ID_SELECT_RB5	20	SW7.6	R128
ID6	ID_SELECT_RB8	32	SW7.7	R129
ID7	ID_SELECT_RB9	33	SW7.8	R130
ID8	ID_SELECT_RB10	34	SW8.1	R131
ID9	ID_SELECT_RB11	35	SW8.2	R133
ID10	ID_SELECT_RB12	41	SW8.3	R134
ID11	ID_SELECT_RB13	42	SW8.4	R132
ID12	ID_SELECT_RC1	6	SW8.5	R135
ID13	ID_SELECT_RC2	7	SW8.6	R136
ID14	ID_SELECT_RC3	8	SW8.7	R137
ID15	ID_SELECT_RC4	9	SW8.8	R138

2.4.6 SPI/SQI/I²C Aardvark®

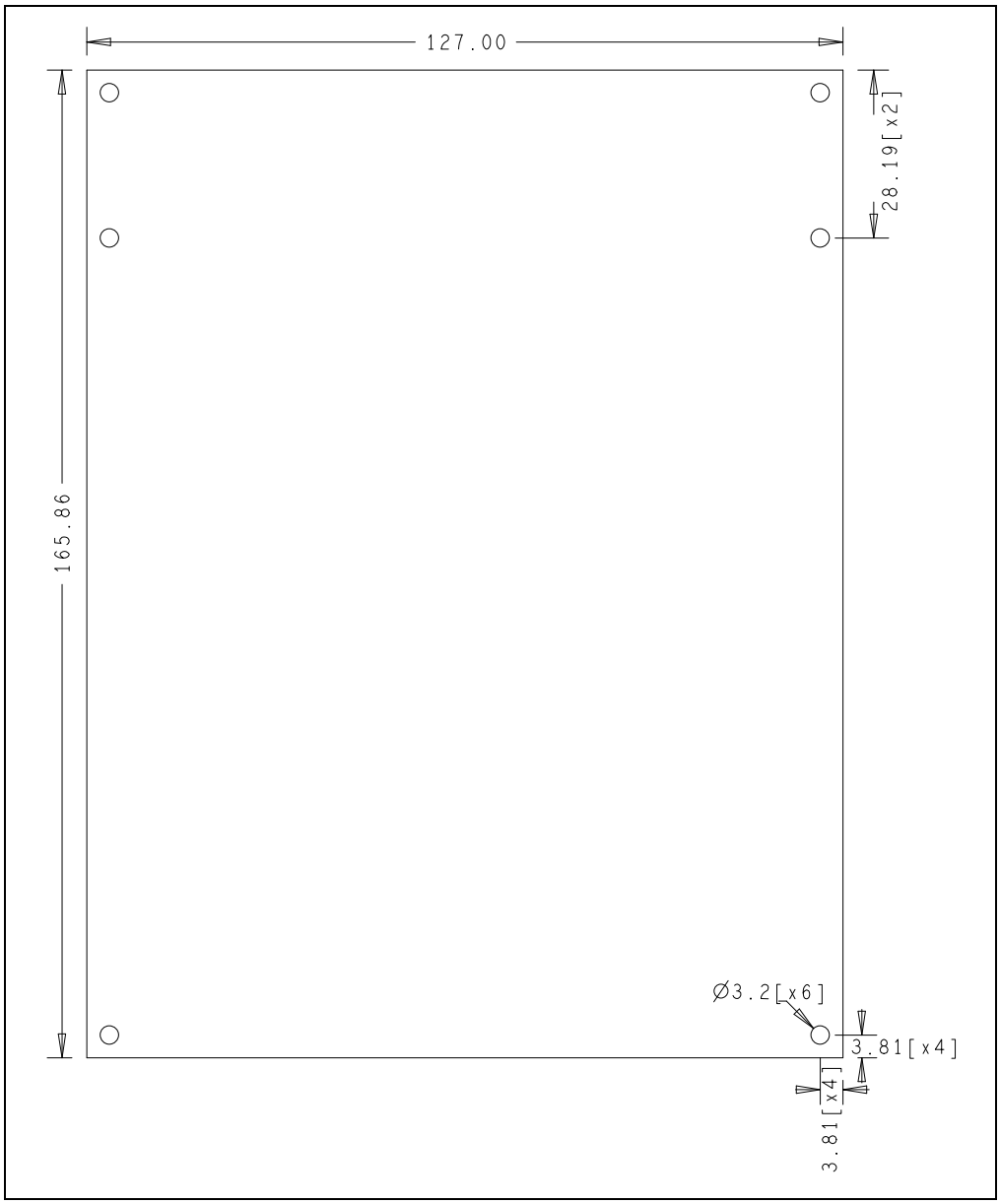
J11 and J12 are used as Aardvark/SPI headers. The respective pin details are shown in Table 2-20. Registers R61, R62, and R122 must be populated to use this option. By default, R61, R62, and R122 are not populated (DNP).

TABLE 2-20: J11 & J12 HEADER PINOUT

Signal	Pin Number
SCL	J11.1
SDA	J11.3
SCK	J11.7
SCS#	J11.9
SI(SIO0)	J11.8
SO(SIO1)	J11.5
SIO2	J12.3
SIO3	J12.4

2.5 MECHANICALS

FIGURE 2-5: EVB-LAN9252-4PORT MECHANICAL DIMENSIONS



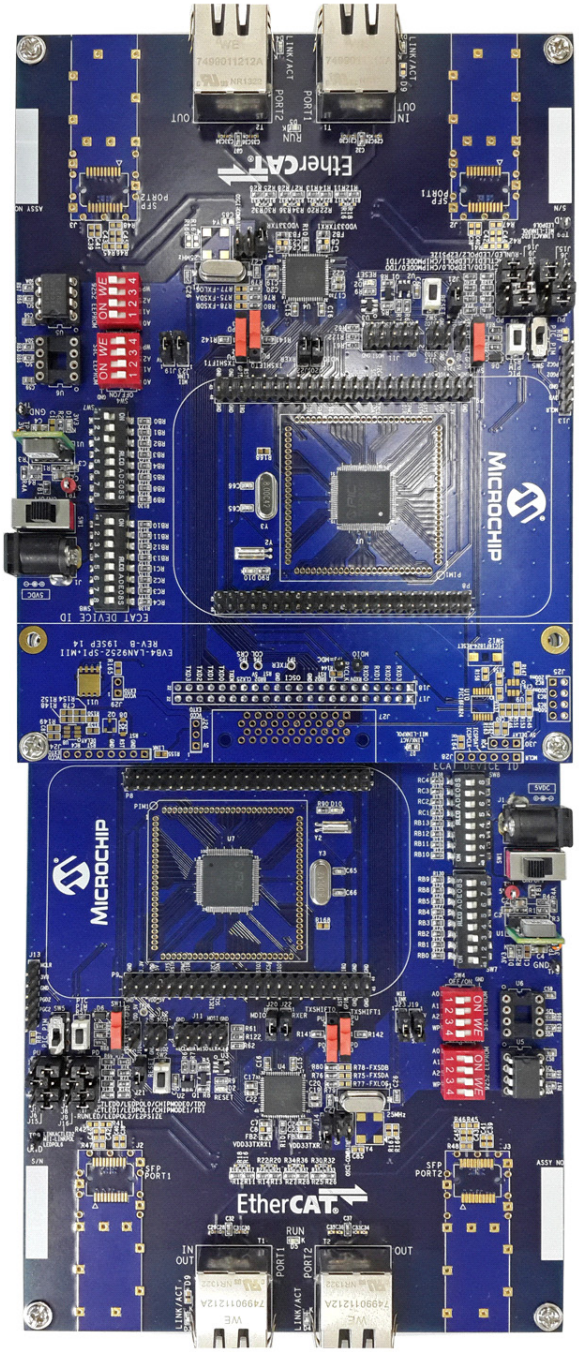
NOTES:

Appendix A. EVB-LAN9252-4PORT Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN9252-4PORT Evaluation Board.

FIGURE A-1: EVB-LAN9252-4PORT EVALUATION BOARD



NOTES:

Appendix B. EVB-LAN9252-4PORT Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9252-4PORT Evaluation Board Schematics.

FIGURE B-1: EVB-LAN9252-4PORT SCHEMATIC POWER SUPPLY & RESET

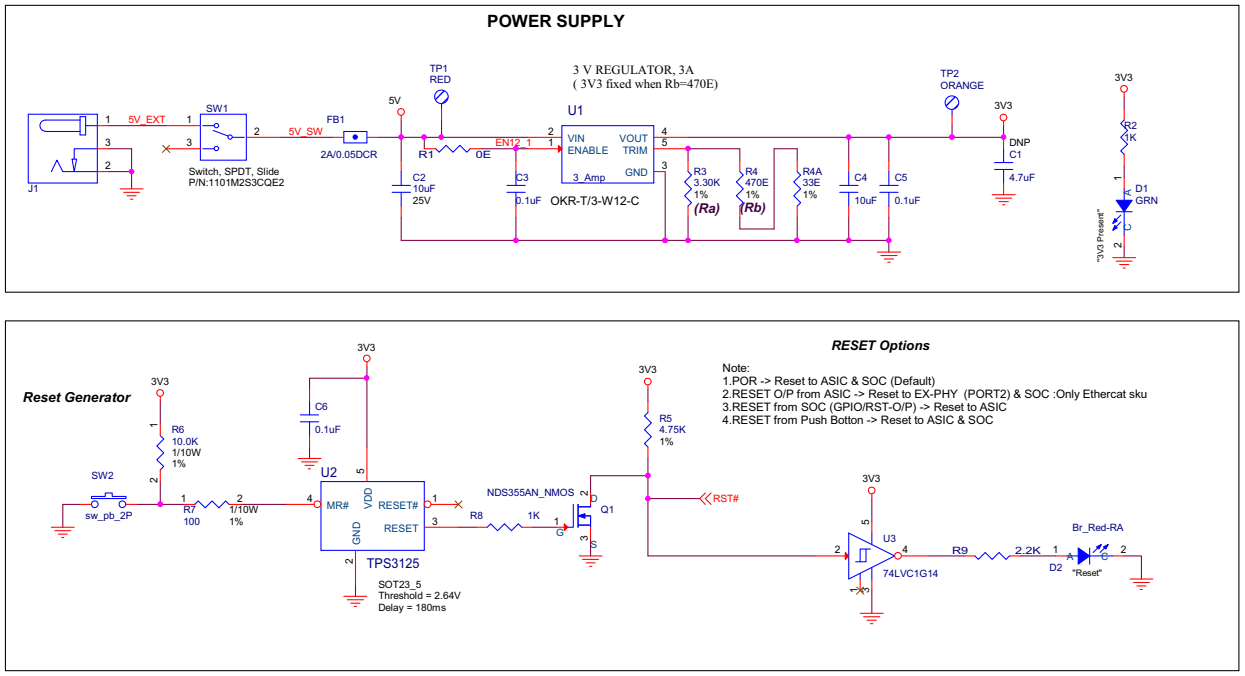


FIGURE B-2: EVB-LAN9252-4PORT SCHEMATIC LAN9252

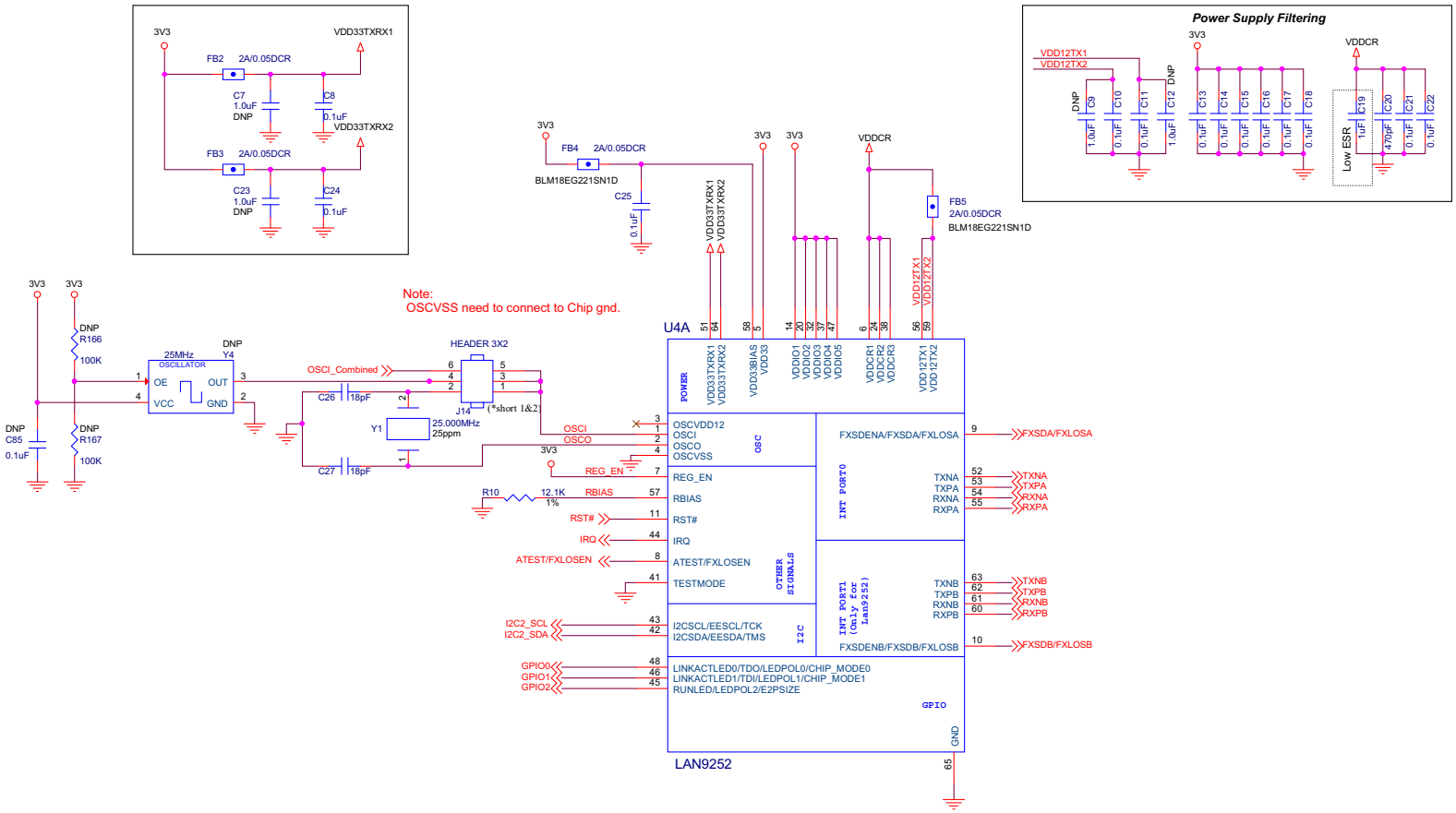


FIGURE B-3: EVB-LAN9252-4PORT SCHEMATIC COPPER MODE INTERFACE

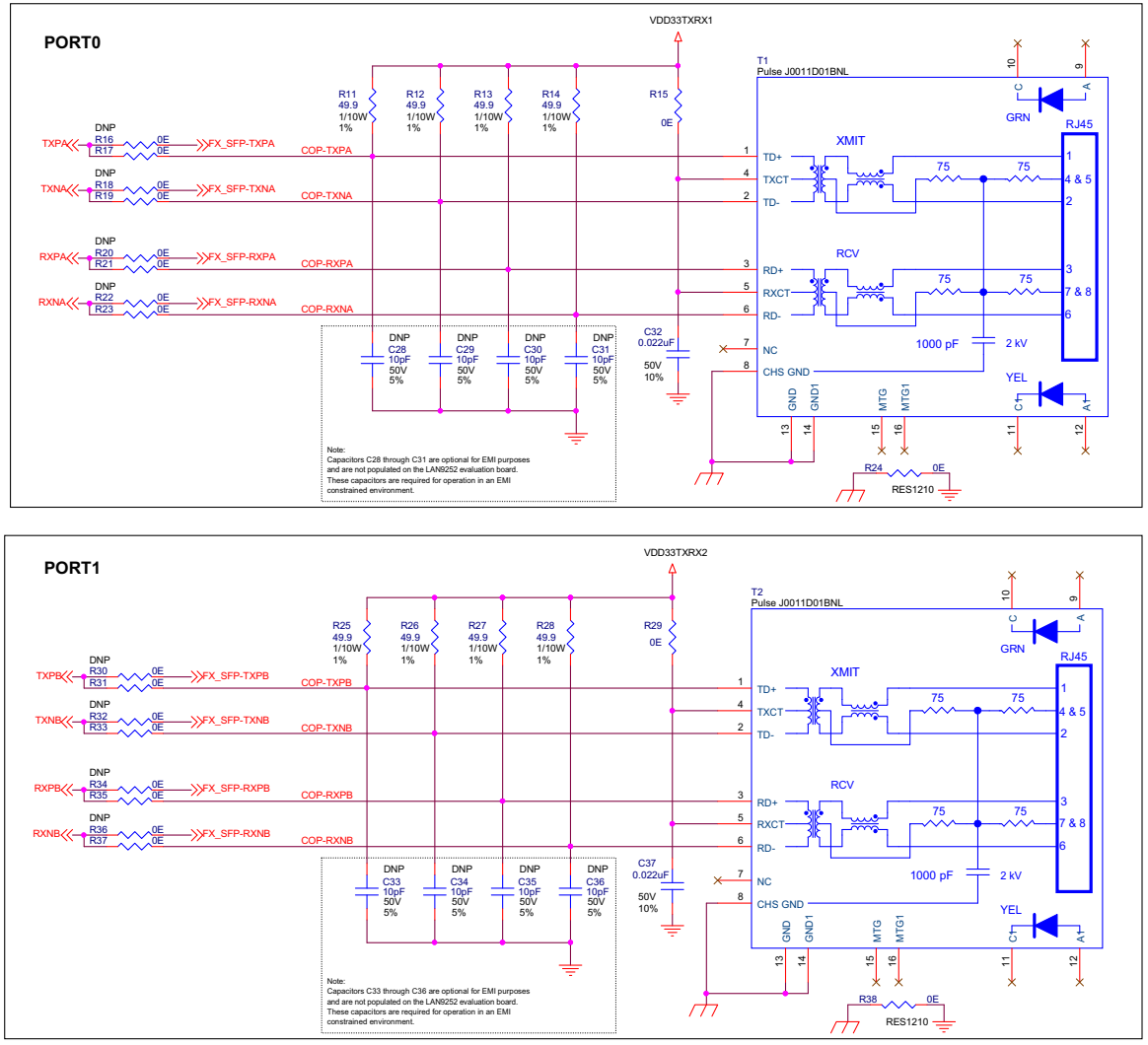


FIGURE B-4: EVB-LAN9252-4PORT SCHEMATIC SFP INTERFACE

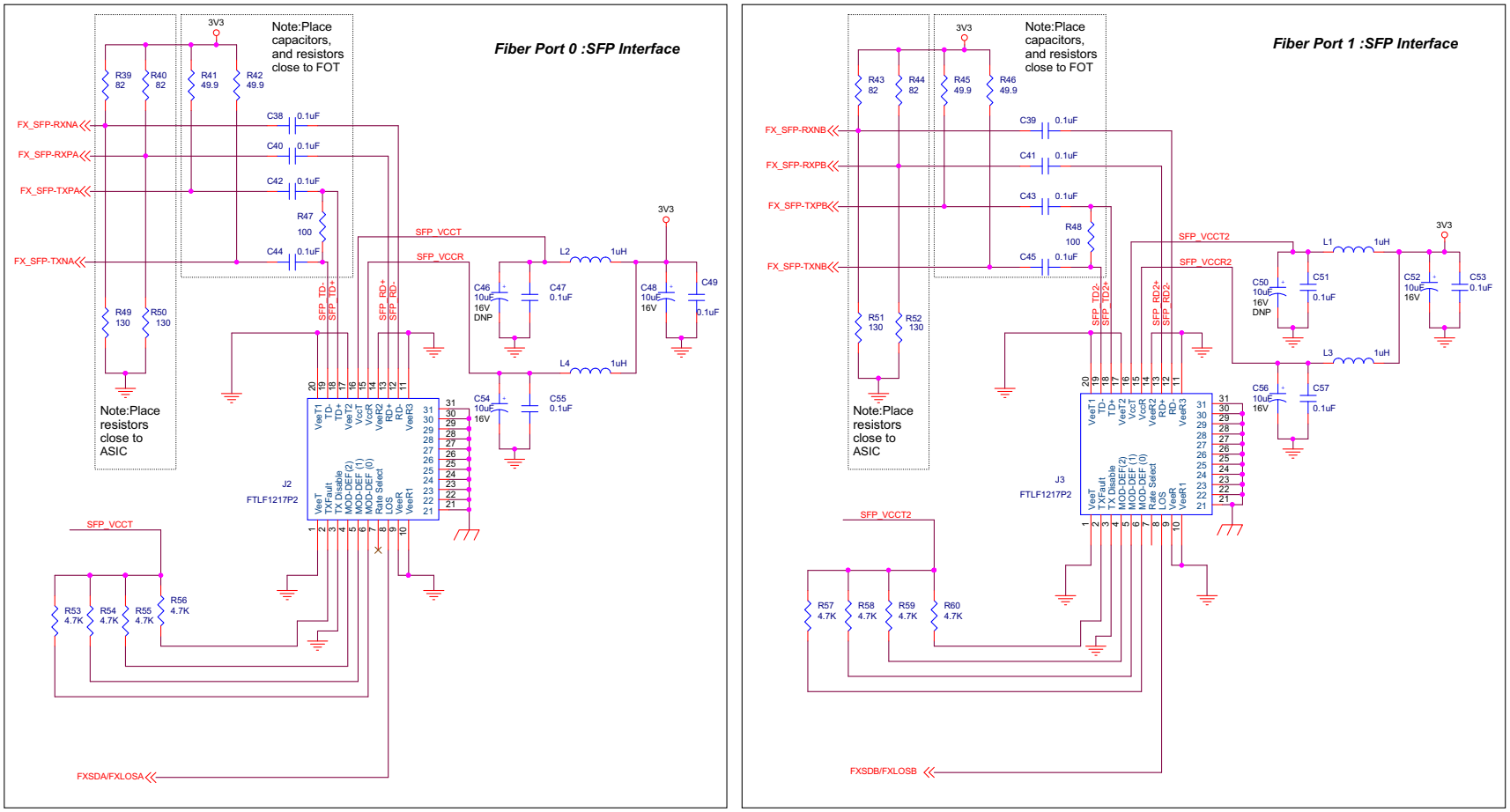
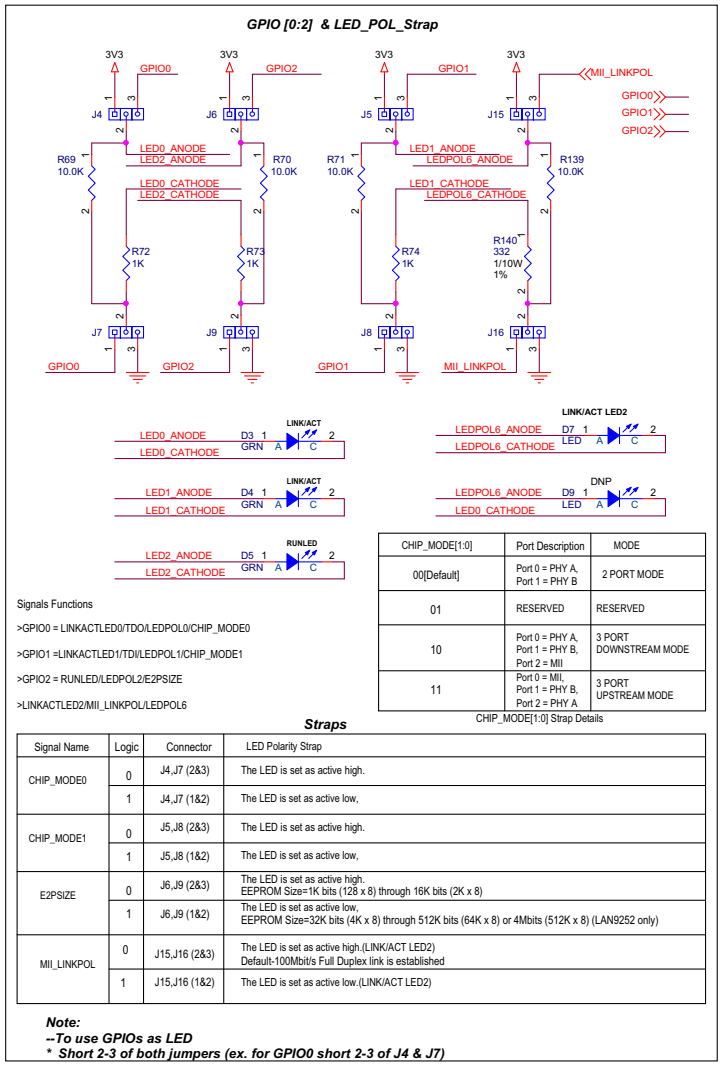


FIGURE B-5: EVB-LAN9252-4PORT STRAPS, GPIO, I²C, AND FXLOS



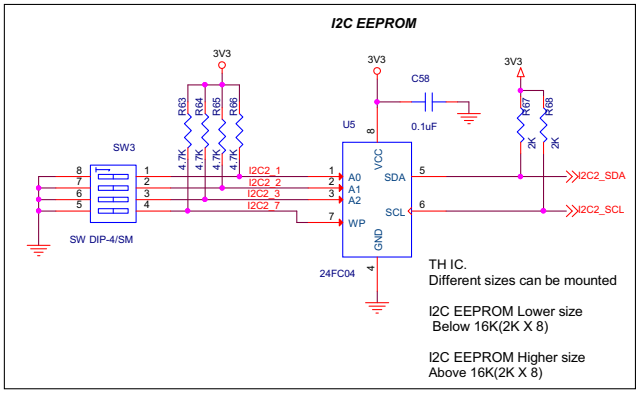
CHIP_MODE[1:0]	Port Description	MODE
00[Default]	Port 0 = PHY A, Port 1 = PHY B	2 PORT MODE
01	RESERVED	RESERVED
10	Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII	3 PORT DOWNSTREAM MODE
11	Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A	3 PORT UPSTREAM MODE

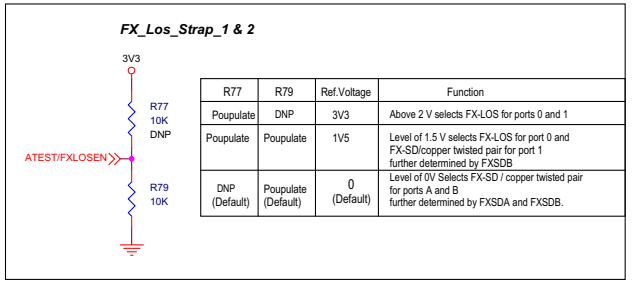
CHIP_MODE[1:0] Strap Details

Straps

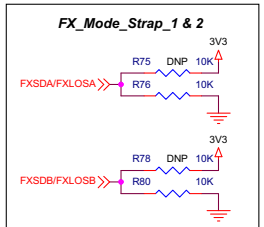
Signal Name	Logic	Connector	LED Polarity Strap
CHIP_MODE0	0	J4,J7 (2&3)	The LED is set as active high.
	1	J4,J7 (1&2)	The LED is set as active low,
CHIP_MODE1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
E2PSIZE	0	J6,J9 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)
MII_LINKPOL	0	J15,J16 (2&3)	The LED is set as active high.(LINK/ACT LED2) Default-100Mbit/s Full Duplex link is established
	1	J15,J16 (1&2)	The LED is set as active low.(LINK/ACT LED2)

Note:
--To use GPIOs as LED
**** Short 2-3 of both jumpers (ex. for GPIO0 short 2-3 of J4 & J7)***

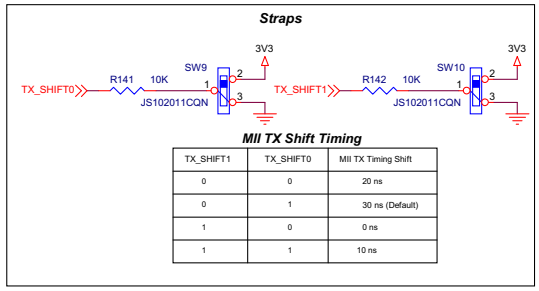




R77	R79	Ref.Voltage	Function
Poupulate	DNP	3V3	Above 2 V selects FX-LOS for ports 0 and 1
Poupulate	Poupulate	1V5	Level of 1.5 V selects FX-LOS for port 0 and FX-SD/copper twisted pair for port 1 further determined by FXSDB
DNP (Default)	Poupulate (Default)	0 (Default)	Level of 0V Selects FX-SD / copper twisted pair for ports A and B further determined by FXSDA and FXSDB.



PORT	MODE	Poupulate	DNP
PORT0	Copper (Default)	R76	R75
	Fiber	R75	R76
PORT1	Copper (Default)	R80	R78
	Fiber	R78	R80



MII TX Shift Timing

TX_SHIFT1	TX_SHIFT0	MII TX Timing Shift
0	0	20 ns
0	1	30 ns (Default)
1	0	0 ns
1	1	10 ns

FIGURE B-6: EVB-LAN9252-4PORT SCHEMATIC BOARD TO BOARD INTERFACE

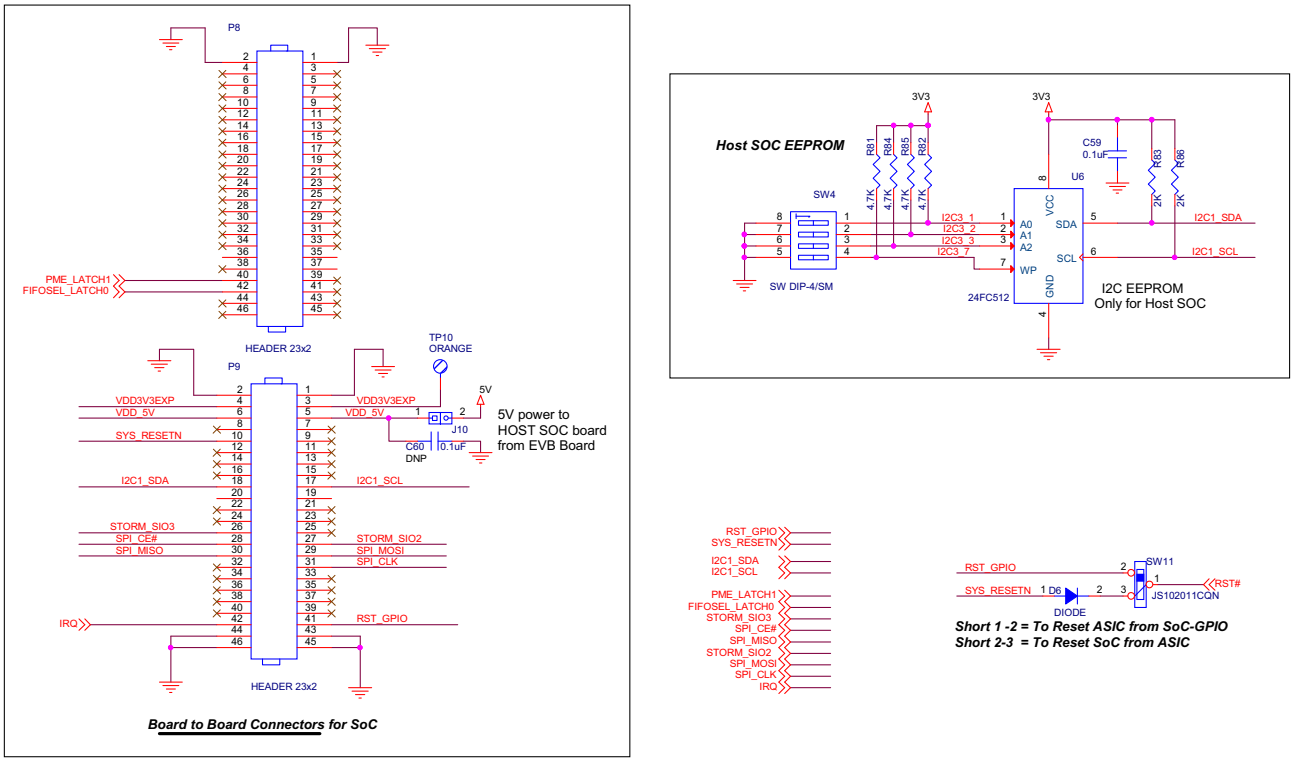


FIGURE B-7: EVB-LAN9252-4PORT SCHEMATIC PIM AND PIC32MX

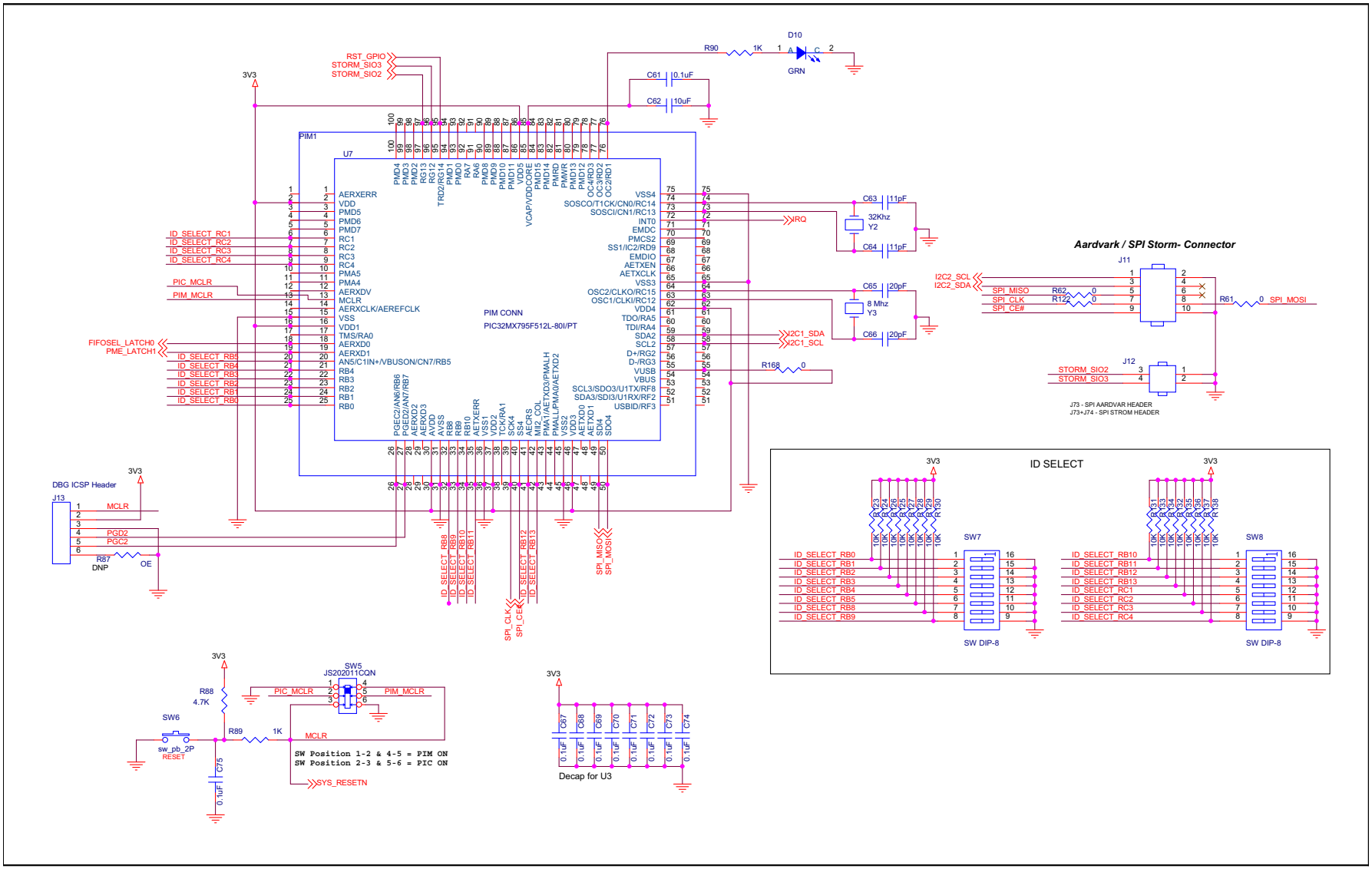
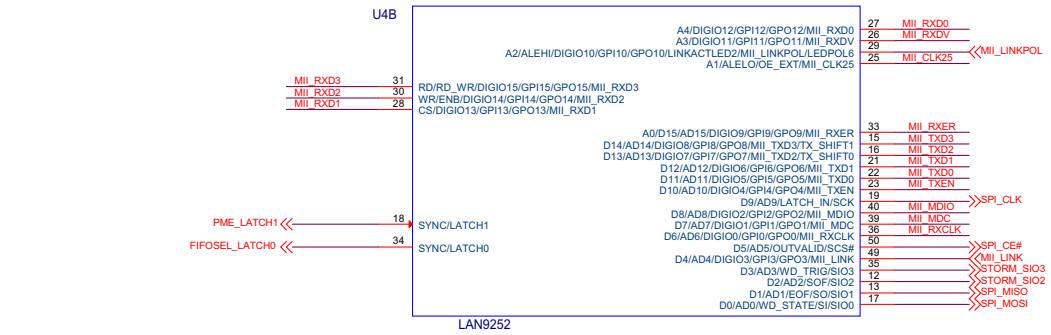
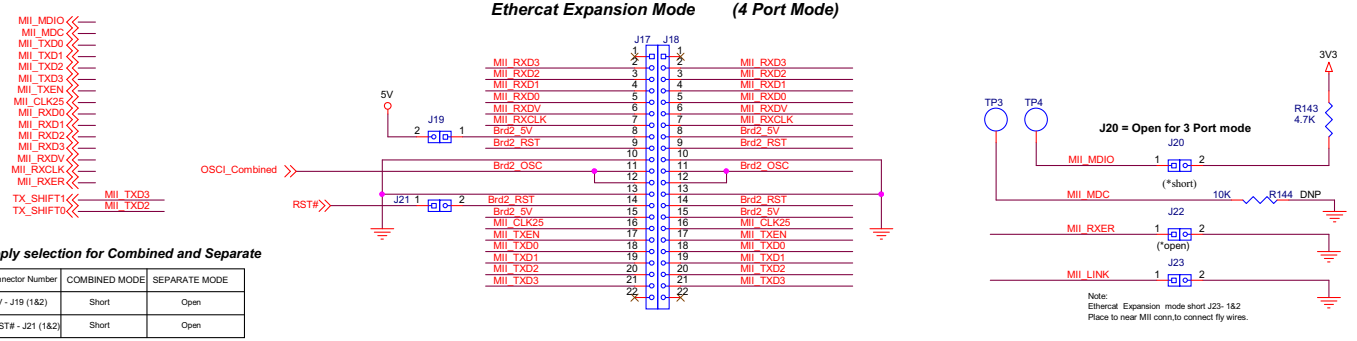


FIGURE B-8: EVB-LAN9252-4PORT SCHEMATIC EXPANSION MODE INTERFACE

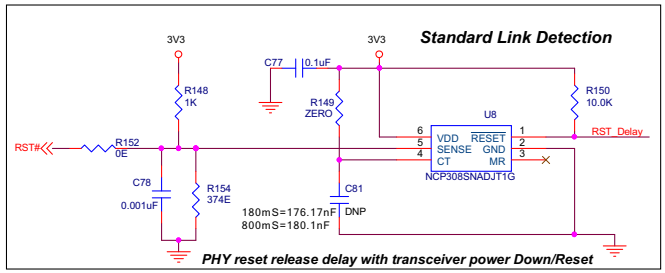


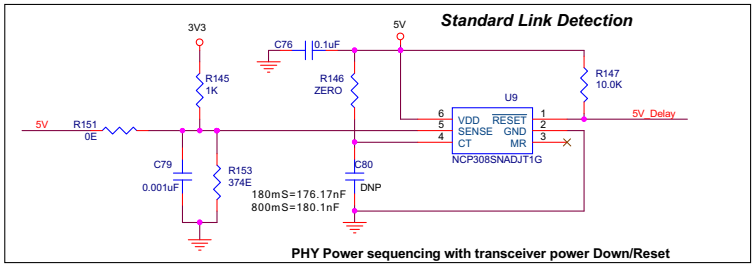


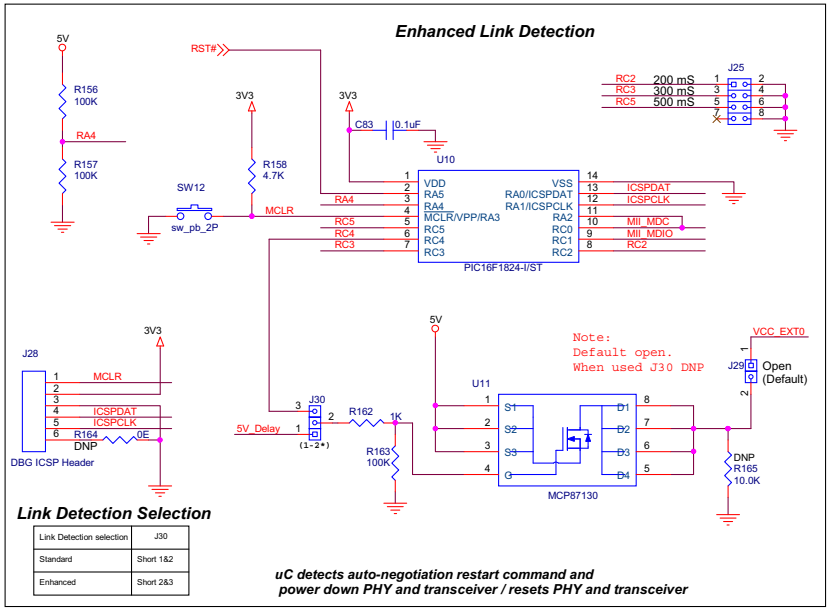
Supply selection for Combined and Separate

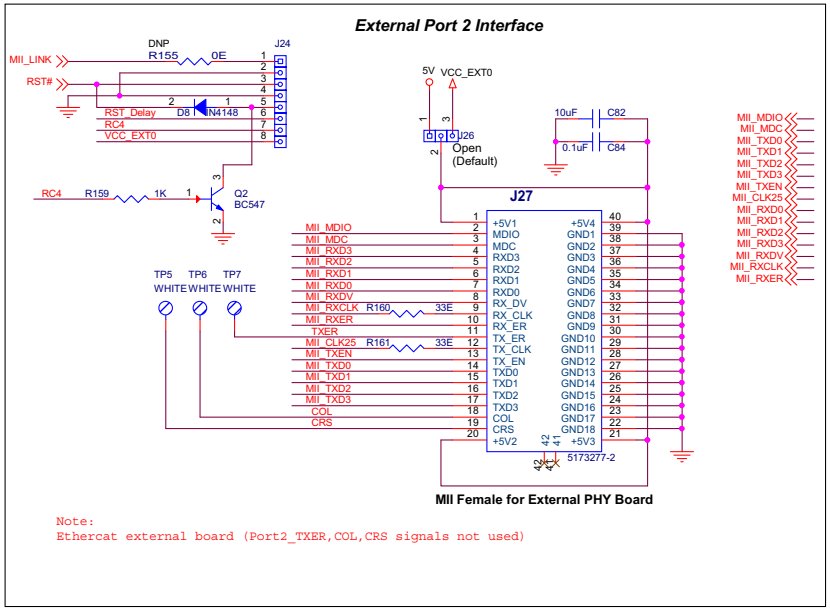
Connector Number	COMBINED MODE	SEPARATE MODE
5V - J19 (1&2)	Short	Open
RST# - J21 (1&2)	Short	Open

FIGURE B-9: EVB-LAN9252-4PORT SCHEMATIC ENHANCED LINK DETECTION









Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9252-4PORT Evaluation Board Bill of Materials (BOM).

Item	Qty	Reference	Part	PCB Footprint	DNP	Vendor	Vendor PN
2	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
3	28	C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17, C18,C21,C22,C24,C25,C58,C59,C61,C67,C68, C69,C70,C71,C72,C73,C74,C75	0.1uF	CAP0603	No	Murata	GRM188R71E104KA01D
5	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
6	1	C20	470pF	CAP0603	No	Murata	GRM033R71E471KA01D
7	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
9	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
12	1	C62	10uF	CAP0603	No	TDK	C1608X5R0J106K080AB
13	2	C63,C64	11pF	CAP0603	No	Murata	GRM1885C1H110JA01D
14	2	C65,C66	20pF	CAP0603	No	Murata	GRM1885C1H200JA01D
17	5	D1,D3,D4,D5,D10	GRN	LED0603	No	Stanley Electric	BG1111C-TR
18	1	D2	Br_Red-RA	LED0603	No	Stanley Electric	FR1113F
19	1	D6	DIODE	SOD123	No	Micro Commercial Co	1N4148W-TP
20	1	D7	LED	LED0603	No	Stanley Electric	BG1111C-TR
22	5	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
23	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
25	8	J4,J5,J6,J7,J8,J9,J15,J16	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
26	1	J11	HEADER 5X2	TH_CONN_2X5P	No	FCI	67997-210HLF
27	1	J12	HEADER 2X2	TH_CONN_2X2P	No	FCI	67997-204HLF
28	1	J13	DBG ICSP Header	TH_CONN_1x6P	No	FCI	68000-106HLF
29	1	J14	HEADER 3X2	TH_CONN_2X2P	No	FCI	67997-206HLF
30	2	J17,J18	1x22	TH_CONN_1X22P	No	FCI	68000-122HLF
31	4	J10,J19,J21,J23	HDR_1x2	TH_CONN_1X2P	No	FCI	68000-102HLF
38	2	P8,P9	HEADER 23x2	TH_CONN_2X23P	No	FCI	67997-246HLF
39	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN
41	6	R1,R15,R29,R61,R62,R122	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V
42	7	R2,R8,R72,R73,R74,R89,r90	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V

43	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
44	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF
45	1	R4A	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF
46	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
47	5	R6,R69,R70,R71,R139	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
48	1	R7	100E	RES0603	No	Panasonic	ERJ-3EKF1000V
49	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
50	1	R10	12.1K	RES0603	No	Rohm	CR03ERTF1212
51	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9	RES0603	No	Yageo America	9C06031A49R9FKHFT
54	8	R17,R19,R21,R23,R31,R33,R35,R37	0E	RES0402	No	Panasonic	ERJ-2GE0R00X
55	2	R24,R38	0E	RES1210	No	Vishay	CRCW12100000Z0EA
61	10	R63,R64,R65,R66,R81,R82,R84,R85,R88,R143	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
62	4	R67,R68,R83,R86	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
64	21	R76,R79,R80,R123,R124,R125,R126,R127, R128,R129,R130,R131,R132,R133,R134, R135,R136,R137,R138,R141,R142	10K	RES0603	No	Panasonic	ERJ-3GEYJ103V
66	1	R140	332	RES0603		Panasonic	ERJ-3EKF3320V
73	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2
74	2	SW2,SW6	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K
75	2	SW3,SW4	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904
76	1	SW5	JS202011CQN	TH_SW_DPDT_6P	No	C&K	401-2001-ND
77	2	SW7,SW8	SW DIP-8	SW_DIP_SMT_8P-ADE08S04	No	TE	1-1825058-9/ade08s04
78	3	SW9,SW10,SW11	450301014042	TH_SW_SPST_3P_10x2p5	No	Wurth electronics	450301014042
79	1	TP1	RED	TH_TP_60D40	No	Keystone	5005
80	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
	2	TP8,TP9	TEST POINT	TH_TP_60D40	No	Keystone	5001
83	2	T1,T2	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	553-1483-ND
84	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
85	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
86	1	U3	74LVC1G14	SOT23_5	No	TI	SN74LVC1G14DCKR
87	1	U4	LAN9252	IC_QFN64	No	Microchip	LAN9252

88	1	U5	24FC04	IC_DIP8_300	No	Microchip	24AA04
89	1	U6	24FC512	IC_DIP8_300	No	Microchip	24FC512-IP
90	1	U7	PIC32MX795F512L-80I/PT	IC_TQFP100_12x12x1-0p4mm	No	Microchip	PIC32MX795F512L-80I/PT-ND
94	1	Y1	Citizen America	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D18-F
95	1	Y2	32Khz	TH_XTAL_ECS-31X_32KHZ	No	ECS INC	XC1392-ND
96	1	Y3	8 Mhz	th_hc49us_2p	No	Citizen Finetech	300-6017-ND

Do NOT Populate Components

Item	Qty	Reference	Part	PCB Footprint	DNP	Vendor	Vendor PN
15	2	C78,C79	0.001uF	CAP0603	DNP	Murata	GRM188R71H102KA01D
3	4	C76,C77,C83,C84	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
71	3	R156,R157,R163	100K	RES0603	DNP	Panasonic	ERJ-3EKF1003V
12	1	C82	10uF	CAP0603	DNP	TDK	C1608X5R0J106K080AB
42	4	R145,R148,R159,R162	1K	RES0603	DNP	Panasonic	ERJ-3GEYJ102V
34	1	J25	2x4	Th_CONN_2X4P	DNP		
45	2	R160,R161	33E	RES0603	DNP	BOURNS	CR0603-FX-33R0ELF
69	2	R153,R154	374E	RES0603	DNP	Panasonic	ERJ-3EKF3740V
61	1	R158	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
35	1	J27	5173277-2	TH_CONN_TE-5173277_40P	DNP	TE	5173277-2-ND
40	1	Q2	BC547	SOT23	DNP	Diodes Incorporated	MMBT4401-7-F
31	1	J29	CONN_2P	TH_CONN_1X2P	DNP		
33	1	J24	CONN_8P	TH_CONN_1X8P	DNP		
28	1	J28	DBG ICSP Header	TH_CONN_1x6P	DNP		
25	2	J26,J30	HDR_1x3	TH_CONN_1X3P	DNP		
21	1	D8	IN4148	SOD123	DNP	Micro Commercial Co	1N4148W-TP
93	1	U11	MCP87130	IC_PDFN8_5x6mm_MCP8713	DNP	Microchip	MCP87130T-U/LCTR-ND
91	2	U8,U9	NCP308SNADJT1G	SOT23_6	DNP	ON Semiconductor	NCP308SNADJT1G-ND
92	1	U10	PIC16F1824-I/ST	IC_TSSOP14-4P5X5MM	DNP	Microchip	PIC16F1824-I/ST-ND
82	3	TP5,TP6,TP7	WHITE	TH_TP_60D40	DNP	Keystone	5002
31	1	J20	CONN_2P	TH_CONN_1X2P	DNP		

32	1	J22	CONN_2P	th_conn_1x2p	DNP		
74	1	SW12	sw_pb_2P	sw_pb_2P	DNP	Panasonic	EVQ-PJU04K
1	1	C1	4.7uF	CAP0603	DNP	Murata	GRM188R60J475KE19D
4	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP	Murata	GRM188R61C105KA93D
8	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP	Murata	GRM188R61C105KA93D
10	14	C38,C39,C40,C41,C42,C43,C44,C45,C47,C49, C51,C53,C55,C57	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
11	6	C46,C48,C50,C52,C54,C56	10uF	CAP_B_3528	DNP	Kemet	B45190E3106K209
16	2	C80,C81	TBD	CAP0603	DNP		
24	2	J2,J3	FTLF1217P2	CONN_FX_SFP_FTLF1217P2	DNP	Finisar	775-1011-ND
36	4	L1,L2,L3,L4	1uH	L0805	DNP	Panasonic	ERJ-3GEY0R00V
53	8	R16,R18,R20,R22,R30,R32,R34,R36	0	RES0402	DNP	Panasonic	ERJ-2GE0R00X
56	4	R39,R40,R43,R44	82	RES0603	DNP	BOURNS	CR0603-FX-82R0ELF
57	4	R41,R42,R45,R46	49.9	RES0603	DNP	Yageo America	9C06031A49R9FKHFT
58	2	R47,R48	100	RES0603	DNP	Panasonic	ERJ-3EKF1000V
59	4	R49,R50,R51,R52	130	RES0603	DNP	Panasonic	ERJ-3EKF1300V
60	8	R53,R54,R55,R56,R57,R58,R59,R60	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
63	4	R75,R77,R78,R144	10K	RES0603	DNP	Panasonic	ERJ-3GEYJ103V
70	7	R155,R146,R149,R151,R152,R164,R168	ZERO	RES0603	DNP		
72	1	R165,R147,R150	10.0K	RES0603	DNP	Panasonic	ERJ-3EKF1002V
37	1	PIM1	PIM CONN	TH_CONN_PIM100	DNP		
81	2	TP3,TP4	TEST POINT	TH_TP_60D40	DNP	FCI	68000-201HLF

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