TEA1742T

GreenChip PFC controller

Rev. 01 — 10 February 2009 Objective data sheet

1. General description

The TEA1742T is a controller for Power Factor Correction (PFC). Its high level of integration allows the design of a cost-effective power supply with a very low number of external components.

The special built-in green functions provide high efficiency at all power levels. This applies to quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping.

The TEA1742T enables highly efficient and reliable supplies with power requirements of up to 500 W, to be designed easily and with the minimum number of external components.

2. Features

2.1 Distinctive features

- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Dual boost PFC with accurate output voltage (NXP patented)
- High level of integration, resulting in a very low external component count and a cost-effective design
- Low start-up supply voltage

2.2 Green features

- Valley/zero voltage switching for minimum switching losses (NXP patented)
- Frequency limitation to reduce switching losses
- High ohmic resistive dividers possible to minimize losses

2.3 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection (NXP patented)
- Accurate OverVoltage Protection (OVP)
- Open control loop protection
- IC OverTemperature Protection (OTP)
- Low and adjustable OverCurrent Protection (OCP) trip level

3. Applications

- The device can be used in all applications that require an efficient and cost-effective PFC solution up to 500 W. PC power supplies in particular can benefit from the high level of integration and high efficiency

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1742T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

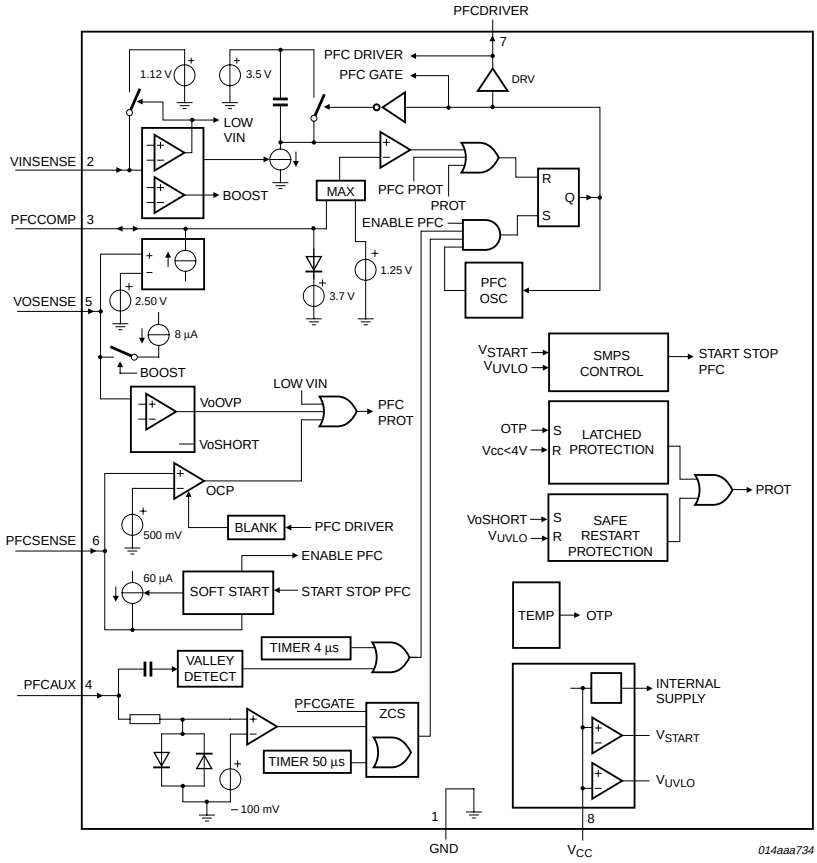


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

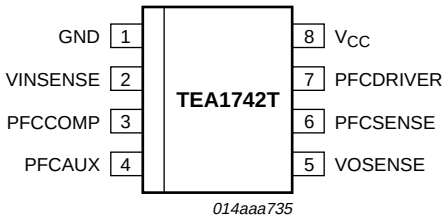


Fig 2. Pin configuration: TEA1742T (SOT96-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1	ground
VINSENSE	2	sense input for mains voltage
PFCCOMP	3	frequency compensation pin for PFC
PFCAUX	4	input from auxiliary winding for demagnetization timing for PFC
VOSENSE	5	sense input for PFC output voltage
PFCSENSE	6	programmable current sense input for PFC
PFCDRIVER	7	gate driver output for PFC
V_{CC}	8	supply voltage

7. Functional description

7.1 General control

The TEA1742T contains a controller for a power factor correction circuit. A typical configuration is shown in Figure 3.

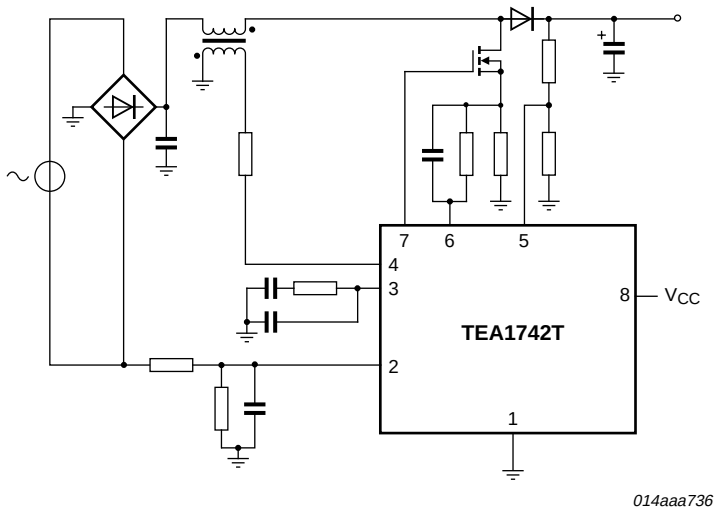


Fig 3. Typical configuration

7.1.1 Start-up and UnderVoltage LockOut (UVLO)

The control logic activates the internal circuitry when the voltage on pin V_{CC} passes the $V_{startup}$ level. First, the soft start capacitor on the PFCSENSE pin is charged. When the soft start capacitor on the PFCSENSE pin is charged, the PFC circuit is activated. See Figure 4.

When one of the protection functions is activated, the converter stops switching. For a restart protection the V_{CC} has to be pulled below $V_{th(UVLO)}$ to reset the protection. For a latched protection (OTP), the V_{CC} has to drop below about 4 V (typ).

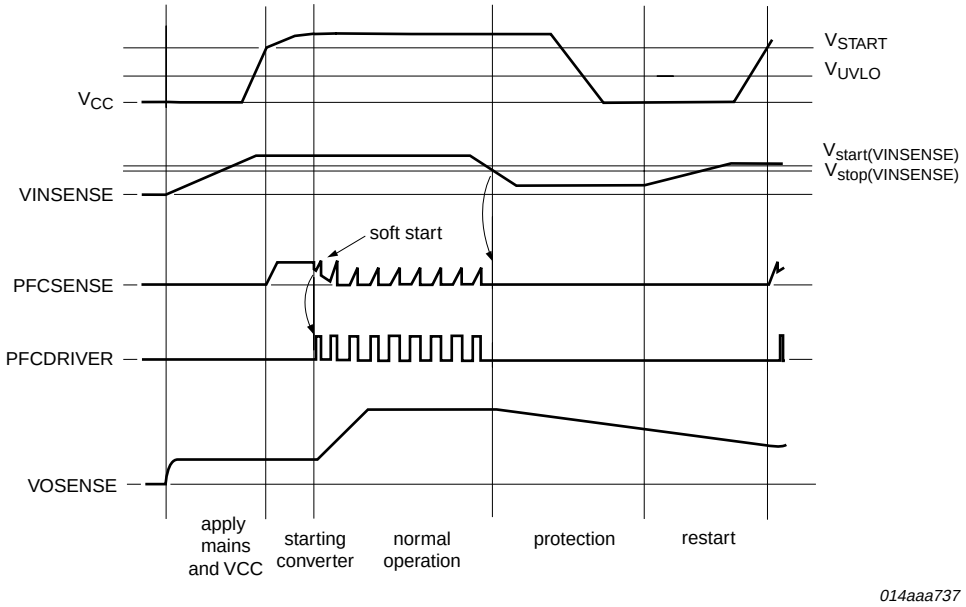


Fig 4. Start-up sequence, normal operation and restart sequence

7.1.2 Supply management

All internal reference voltages are derived from a temperature compensated and trimmed on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

7.1.3 OverTemperature Protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching.

OTP is a latched protection. It can be reset by removing the voltage on pin V_{CC}.

7.2 Power factor correction circuit

The power factor correction circuit operates in quasi-resonant or discontinuous conduction mode with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. The voltage on the PFCAUX pin is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

7.2.1 t_{on} control

The power factor correction circuit is operated in t_{on} control. The resulting mains harmonic reduction of a typical application is well within the class-D requirements.

7.2.2 Valley switching and demagnetization (PFCAUX pin)

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next stroke is started if the voltage across the PFC MOSFET is at its minimum in order to reduce switching losses and ElectroMagnetic Interference (EMI) (valley switching).

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 ms (typ) after the last PFCGATE signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal 4 ms (typ) after demagnetization was detected.

To protect the internal circuitry, for example during lightning events, it is advisable to add a 5 kΩ series resistor to this pin. To prevent incorrect switching due to external disturbance, the resistor should be placed close to the IC on the printed circuit board.

7.2.3 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation is above the $f_{sw(PFC)max}$ limit, the system switches over to discontinuous conduction mode. Also here, the PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching).

7.2.4 Mains voltage compensation (VINSENSE pin)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application this results in a low bandwidth for low mains input voltages, while at high mains input voltages the Mains Harmonic Reduction (MHR) requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA1742T contains a correction circuit. Via the VINSENSE pin the average input voltage is measured and the information is fed to an internal compensation circuit. With this compensation it is possible to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

In a typical application, the bandwidth of the regulation loop is set by a resistor and two capacitors on the PFCCOMP pin.

7.2.5 Soft start-up (pin PFCSENSE)

To prevent audible transformer noise at start-up or during hiccup, the transformer peak current, I_{DM}, is increased slowly by the soft start function. This can be achieved by inserting R_{SS1} and C_{SS1} between pin PFCSENSE and current sense resistor R_{SENSE1}. An internal current source charges the capacitor to $V_{PFCSENSE} = I_{start(soft)PFC} \times R_{SS1}$. The voltage is limited to $V_{start(soft)PFC}$.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS1} and C_{SS1}.

$$\tau softstart = 3 \times R_{SS1} \times C_{SS1}$$

The charging current $I_{start(soft)PFC}$ flows as long as the voltage on pin PFCSENSE is below 0.5 V (typ). If the voltage on pin PFCSENSE exceeds 0.5 V, the soft start current source starts limiting the current $I_{start(soft)PFC}$. As soon as the PFC starts switching, the $I_{start(soft)PFC}$ current source is switched off; see Figure 5.

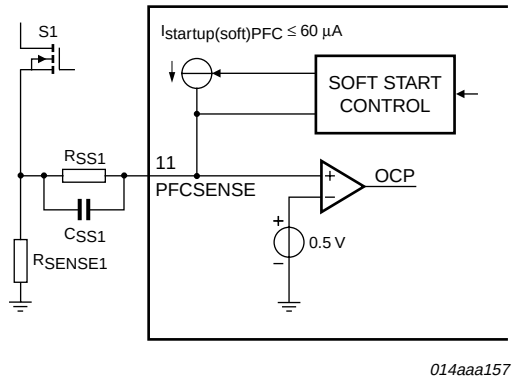


Fig 5. Soft start-up of PFC

7.2.6 Dual boost PFC

The PFC output voltage is modulated by the mains input voltage. The mains input voltage is measured via the VINSENSE pin. The current is sourced from the VOSENSE pin if the voltage on the VINSENSE pin drops below 2.2 V (typ). To ensure the stability of the switch-over 200 mV is inserted around the 2.2 V, see Figure 6.

For low VINSENSE input voltages, the output current is 8 mA (typ). This output current, in combination with the resistors on the VOSENSE pin, sets the lower PFC output voltage level at low mains voltages. At high mains input voltages the current is switched to zero. The PFC output voltage will then be at its maximum. As this current is zero in this situation, it does not effect the accuracy of the PFC output voltage.

For proper switch-off behavior, the VOSENSE current is switched to its maximum value, 8 mA (typ), as soon as the voltage on pin VOSENSE drops below 2.1 V (typ).

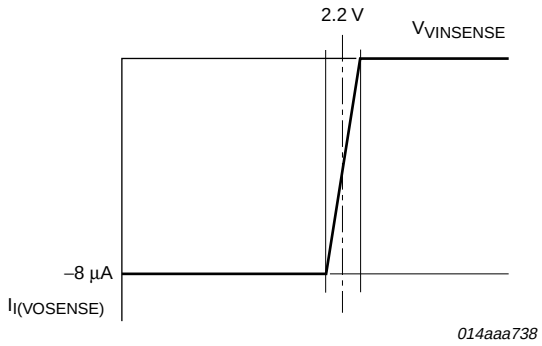


Fig 6. Voltage to current transfer function for dual boost PFC

7.2.7 Overcurrent protection (PFCSENSE pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor, R_{SENSE1}, on the source of the external MOSFET. The voltage is measured via the PFCSENSE pin.

7.2.8 Mains undervoltage lockout / brownout protection (VINSENSE pin)

To prevent the PFC from operating at very low mains input voltages, the voltage on the VINSENSE pin is sensed continuously. As soon as the voltage on this pin drops below the $V_{stop(VINSENSE)}$ level, switching of the PFC is stopped.

The voltage on pin VINSENSE is clamped to a minimum value, $V_{start(VINSENSE)} + \Delta V_{pu(VINSENSE)}$, for a fast restart as soon as the mains input voltage is restored after a mains dropout.

7.2.9 Overvoltage protection (VOSENSE pin)

To prevent output overvoltage during load steps and mains transients, an overvoltage protection circuit is built in.

As soon as the voltage on the VOSENSE pin exceeds the $V_{ovp(VOSENSE)}$ level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences as soon as the VOSENSE pin voltage drops below the $V_{OVP(VOSENSE)}$ level again.

When the resistor between pin VOSENSE and ground is open, the overvoltage protection is also triggered.

7.2.10 PFC open-loop protection (VOSENSE pin)

The power factor correction circuit does not start switching until the voltage on the VOSENSE pin is above the $V_{th(ol)(VOSENSE)}$ level. This protects the circuit from open-loop and VOSENSE short situations.

7.2.11 Driver (pin PFCDRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically –500 (TBF) mA and a current sink capability of typically 1.2 (TBF) A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		–0.4	+38	V
$V_{PFCCOMP}$	voltage on pin PFCCOMP		–0.4	+5	V
$V_{VINSENSE}$	voltage on pin VINSENSE		–0.4	+5	V
$V_{VOSENSE}$	voltage on pin VOSENSE		–0.4	+5	V
V_{PFCAUX}	voltage on pin PFCAUX		–25	+25	V
$V_{PFCSENSE}$	voltage on pin PFCSENSE	current limited	–0.4	+5	V

Table 3. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Currents						
$I_{PFCSENSE}$	current on pin PFCSENSE			–1	+10	mA
$I_{PFCDRIVER}$	current on pin PFCDRIVER	duty cycle < 10 %		–0.8	+2	A
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.45	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
	human body model		[1]	-	2000	V
	machine model		[2]	-	200	V
	charged device model			-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	150	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin V_{CC})						
$V_{startup}$	start-up voltage			10.6		V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage			10.3		V
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$		0.3		V
$I_{CC(oper)}$	operating supply current	no load on pin PFCDRIVER	-	<tbd>	-	mA
$V_{rst(latch)}$	latched reset voltage			4		V
Input Voltage Sensing PFC (pin VINSENSE)						
$V_{stop(VINSENSE)}$	stop voltage on pin VINSENSE		0.86	0.89	0.92	V
$V_{start(VINSENSE)}$	start voltage on pin VINSENSE		1.11	1.15	1.19	V
$\Delta V_{pu(VINSENSE)}$	pull-up voltage difference on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	-	–100	-	mV

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{pu(VINSENSE)}$	pull-up current on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	–55	–47	–40	µA
$V_{mvc(VINSENSE)max}$	maximum mains voltage compensation voltage on pin VINSENSE		4.0	-	-	V
$I_{I(VINSENSE)}$	input current on pin VINSENSE	VINSENSE > $V_{stop(VINSENSE)}$ after $V_{start(VINSENSE)}$ is detected	5	33	100	nA
$V_{bst(dual)}$	dual boost voltage	current switch-over point	-	2.2	-	V
		switch-over region	-	200	-	mV
Loop compensation PFC (pin PFCCOMP)						
g_m	transconductance	$V_{VOSENSE}$ to $I_{O(PFCCOMP)}$	60	80	100	µA/V
$I_{O(PFCCOMP)}$	output current on pin PFCCOMP	$V_{VOSENSE}$ = 2.0V	33	39	45	µA
		$V_{VOSENSE}$ = 3.3V	–45	–39	–33	µA
$V_{clamp(PFCCOMP)}$	clamp voltage on pin PFCCOMP	Low power mode, PFC off, lower clamp voltage [1]	2.5	2.7	2.9	V
		Upper clamp voltage [1]	-	3.9	-	V
$V_{ton(PFCCOMP)zero}$	zero on-time voltage on pin PFCCOMP		3.4	3.5	3.6	V
$V_{ton(PFCCOMP)max}$	maximum on-time voltage on pin PFCCOMP		1.20	1.25	1.30	V
Pulse width modulator PFC						
$t_{on(PFC)}$	PFC on-time	$V_{VINSENSE}$ = 3.3 V, $V_{PFCCOMP}$ = $V_{ton(PFCCOMP)max}$	3.6	4.5	5.0	µs
		$V_{VINSENSE}$ = 0.9 V, $V_{PFCCOMP}$ = $V_{ton(PFCCOMP)max}$	30	40	53	µs
Output voltage sensing PFC (pin VOSENSE)						
$V_{th(ol)(VOSENSE)}$	open-loop threshold voltage on pin VOSENSE		-	1.15	-	V
$V_{reg(VOSENSE)}$	regulation voltage on pin VOSENSE	for $I_{O(PFCCOMP)}$ = 0	2.475	2.500	2.525	V
$V_{ovp(VOSENSE)}$	overvoltage protection voltage on pin VOSENSE		2.60	2.63	2.67	V
$I_{bst(dual)}$	dual boost current	$V_{VINSENSE}$ < $V_{bst(dual)}$ or $V_{VOSENSE}$ < 2.1 V	-	-8	-	µA
		$V_{VINSENSE}$ > $V_{bst(dual)}$	-	-30	-	nA
Overcurrent protection PFC (pin PFCSENSE)						
$V_{sense(PFC)max}$	maximum PFC sense voltage	ΔV/Δt = 50 mV/µs	0.49	0.52	0.55	V
		ΔV/Δt = 200 mV/µs	0.51	0.54	0.57	V
$t_{leb(PFC)}$	PFC leading edge blanking time		250	310	370	ns
$I_{prot(PFCSENSE)}$	protection current on pin PFCSENSE		–50	-	–5	nA

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Soft start PFC (pin PFCSENSE)							
$I_{start(soft)PFC}$	PFC soft start current			–75	–60	–45	µA
$V_{start(soft)PFC}$	PFC soft start voltage	enabling voltage		0.46	0.50	0.54	V
$R_{start(soft)PFC}$	PFC soft start resistance			12	-	-	kΩ
Oscillator PFC							
$f_{sw(PFC)max}$	maximum PFC switching frequency			100	125	150	kHz
$t_{off(PFC)min}$	minimum PFC off-time			1.1	1.4	1.7	µs
Valley switching PFC (pin PFCAUX)							
$(\Delta V/\Delta t)_{vrec(PFC)}$	PFC valley recognition voltage change with time			-	-	1.7	V/µs
$t_{vrec(PFC)}$	PFC valley recognition time	V_{PFCAUX} = 1 V peak-peak	[2]	-	-	50	ns
$t_{to(vrec)PFC}$	PFC valley recognition time-out time			3	4	6	µs
Demagnetization management PFC (pin PFCAUX)							
$V_{th(comp)PFCAUX}$	comparator threshold voltage on pin PFCAUX			–150	–100	–50	mV
$t_{to(demag)PFC}$	PFC demagnetization time-out time			40	50	60	µs
$I_{prot(PFCAUX)}$	protection current on pin PFCAUX	V_{PFCAUX} = 50 mV		–75	-	–5	nA
Driver (pin PFCDRIVER)							
$I_{src(PFCDRIVER)}$	source current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V		-	–0.5 TBF	-	A
$I_{sink(PFCDRIVER)}$	sink current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V		-	0.7 TBF	-	A
		$V_{PFCDRIVER}$ = 10 V		-	1.2 TBF	-	A
$V_{O(PFCDRIVER)max}$	maximum output voltage on pin PFCDRIVER			-	11	12	V
Temperature protection							
$T_{pl(IC)}$	IC protection level temperature			130	140	150	°C
$T_{pl(IC)hys}$	hysteresis of IC protection level temperature			-	10	-	°C

[1] For a typical application with a compensation network on pin PFCCOMP, like the example in Figure 3.

[2] Minimum required voltage change time for valley recognition on pin PFCAUX.

11. Application information

Capacitor C_{VCC} buffers the IC supply voltage, which has to be supplied by external means. Sense resistor R_{SENSE1} converts the current through the MOSFET S1 into a voltage at pin PFCSENSE. The value of R_{SENSE1} defines the maximum primary peak current in MOSFETS S1.

R_{S1} is added to prevent the soft start capacitor from being charged during normal operation due to negative voltage spikes across the sense resistor.

Resistor R_{AUX1} is added to protect the IC from damage during lightning events.

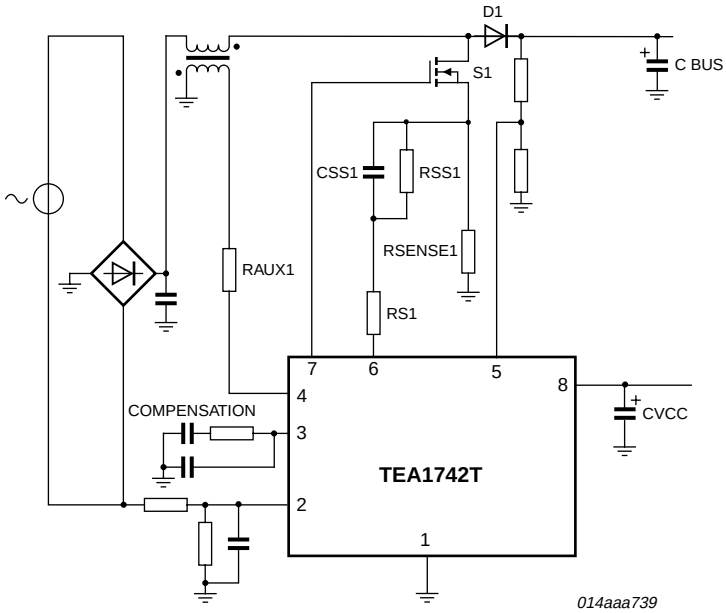
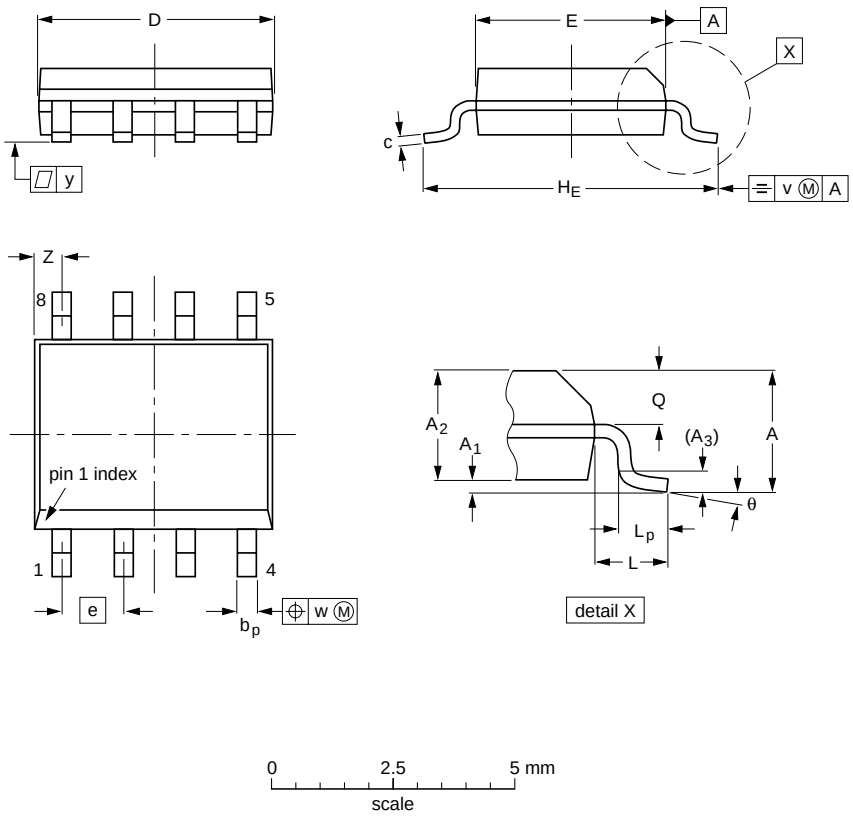


Fig 7. Typical application diagram TEA1742T

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 8. Package outline SOT96-1 (SO8)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1742T_1	20090210	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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