Ordering number : ENA0663A

LV5781

Bi-CMOS IC

3A, Point-of-load, Chopper-type Step-down Converter

ON Semiconductor®
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Overview

The LV5781 is a 1-channel chopper-type (low-side Schottky diode) step-down switching regulator. It incorporates an 80mΩ (typical) power MOSFET to achieve high-efficiency operation for 3A output currents.
The output voltage is set internally to 3.3V. By adding two external resistors, it is possible to set the voltage to any desired setting above 0.85V. Inrush current at startup can be prevented by the soft start function.
Using the ON/OFF pins, the converter can be set to standby mode in which the current consumption is 10μA or less.
Both the load and the IC are protected by means of the overcurrent and thermal protection functions. The converter uses the HSSOP14 miniature package.

Functions

- 3A, 1-channel chopper-type, step-down switching regulator
- Output voltage: 3.3V
- Setting of any output voltage enabled (external resistors required)
- High efficiency: 90% at I_{OUT}=1A, V_O=3.3V
- Miniature package: HSSOP14
- Soft start function
- Standby mode
- Overcurrent protection
- Thermal shutdown
- Fixed frequency: 180kHz

Applications

- LCD TVs
- Game machines

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input voltage	V_{IN} max		6.5	V
Maximum CBOOT pin voltage	VBT max		13	V
Maximum SW pin voltage	VSW max		6.5	V
Maximum voltage between CBOOT and SW pins	VBS max		6.5	V
Maximum voltage at FB, SS, and ENABLE pins	Vfs max		6.5	V
Junction temperature	Tj max		125	°C
Allowable power dissipation	Pd max	Mounted on a circuit board *1	0.85	W
Operating temperature range	Topr		-30 to +80	°C
Storage temperature range	Tstg		-40 to +125	°C

*1: Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy.

*2: To ensure that the maximum voltage is not exceeded even for an instant, check that the coil voltage and other surge voltage levels are factored in.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		4.5 to 6	V
CBOOT pin voltage	VBT		0 to 6	V
SW pin voltage	VSW		6	V
FB, SS, and ENABLE pin voltage	VFSO		6	V

Electrical Characteristics at Ta=25°C, V_{IN}=5V (Unless specifically specified)

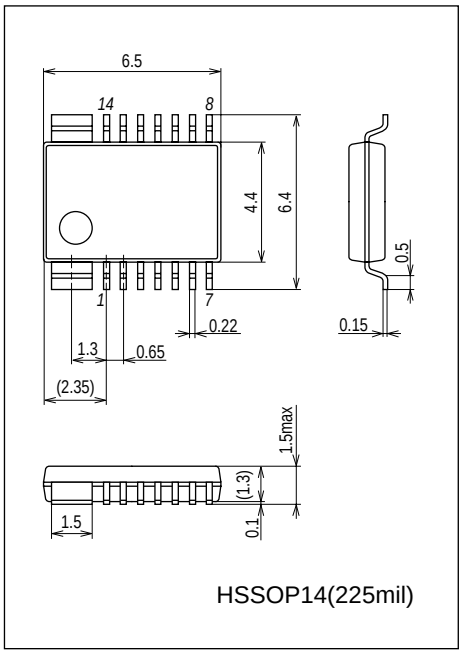
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage 1	$V_{OUT}1$	FB2 pin selected	3.2	3.3	3.4	V
Output voltage 2	$V_{OUT}2$	Dependent on the external voltage divider	0.85			V
Standby mode IC consumption current	$I_{CC}1$	ENABLE=0V		1	10	μA
Operating time IC consumption current	$I_{CC}2$	ENABLE=3V		2	5	mA
ENABLE high level voltage	VENH		3			V
ENABLE low level voltage	VENL				0.7	V
Efficiency	Effcy	I_{OUT}=1A, V_O=3.3V		90		%
Reference voltage	Vref	V_{IN}=4.5V to 6V(±2%)	0.76	0.8	0.84	V
FB pin bias current	Iref			50	200	nA
On resistance	Ron	CBOOT=5V		80		mΩ
Soft start current	ISS		3	6.5	13	μA
Oscillation frequency	Fosc		145	180	225	kHz
Maximum on duty ratio	D max		85			%
Current limiting value	Icl		4.1			A
Under voltage detection	Vl		3.3	3.7	4.2	V
Under voltage detection hysteresis	Vlh		0.15	0.185	0.25	V
Thermal shutdown temperature	Ttsd	Design guarantee value*		180		°C
Thermal shutdown temperature hysteresis	Dtsd	Design guarantee value*		20		°C

*These are design guarantee values and no measurements are made.

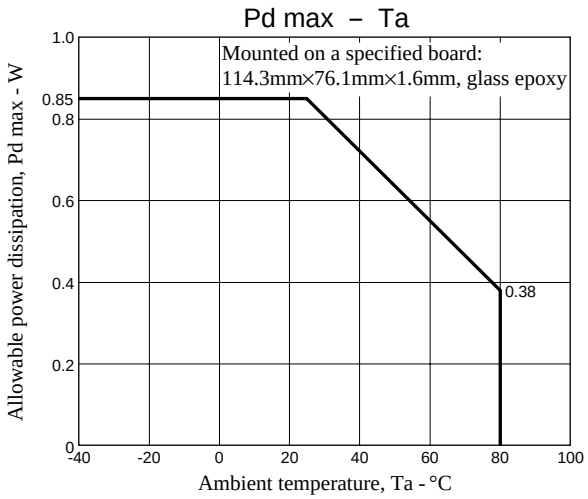
Package Dimensions

unit : mm (typ)

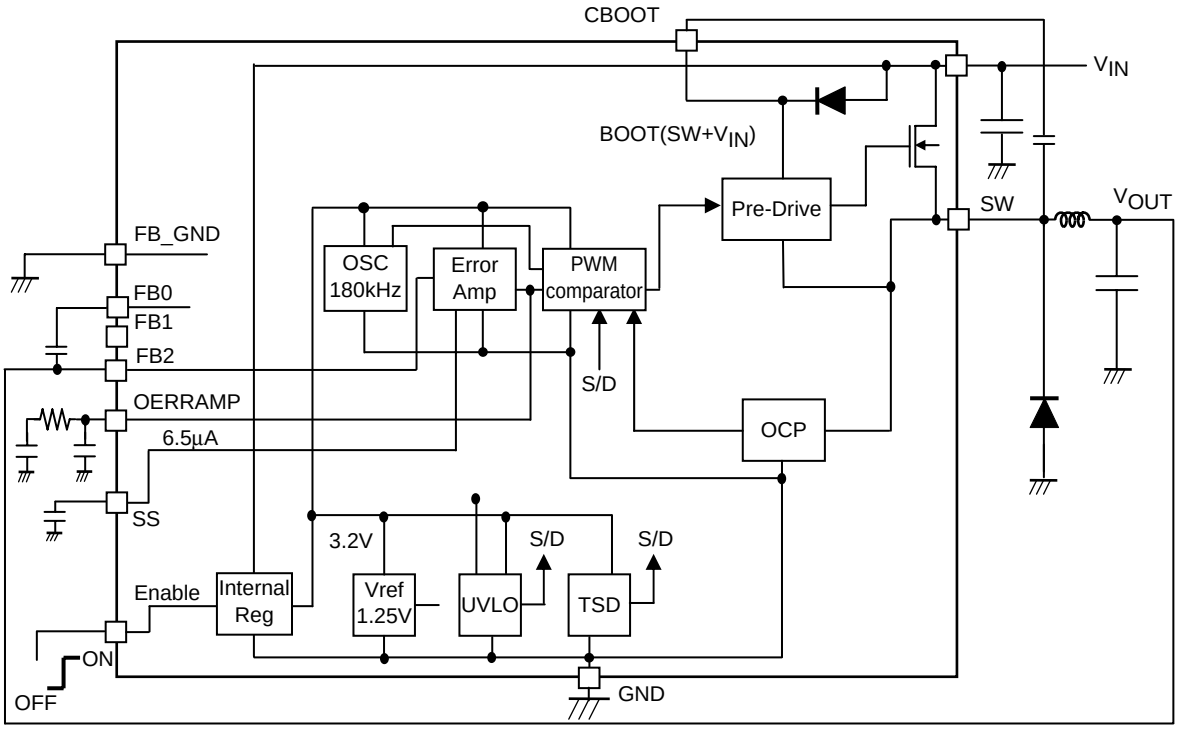
3313



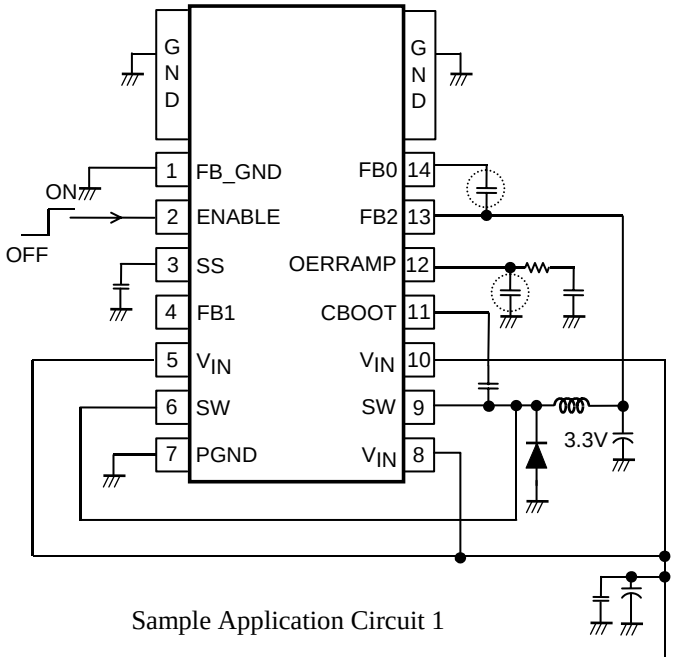
HSSOP14(225mil)



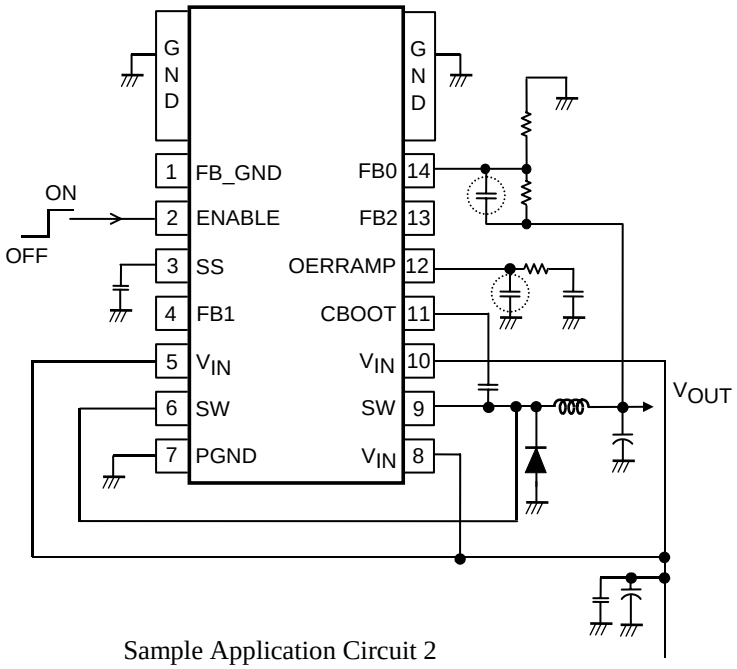
Block Diagram and Sample Application Circuits



Pin Assignment and Sample Application Circuits



Sample Application Circuit 1



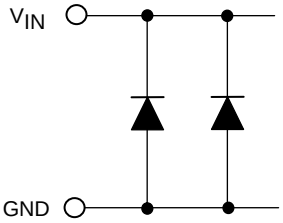
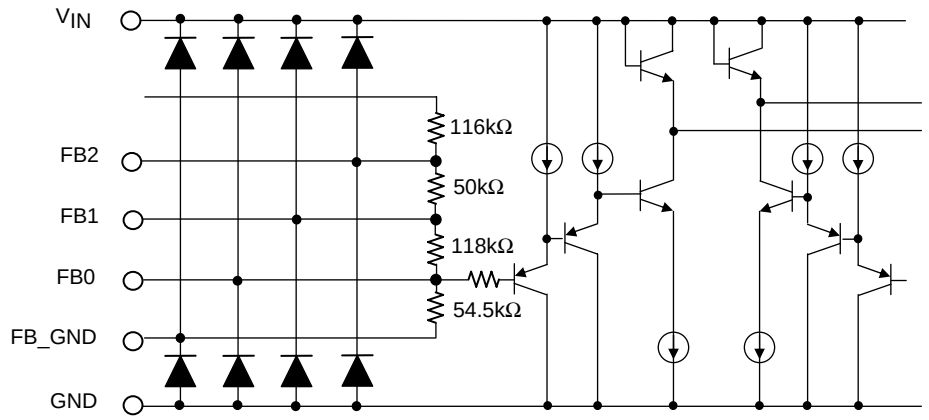
Sample Application Circuit 2

*The capacitor between the FB0 and V_{OUT} pins and capacitor between the OERRAMP pin and GND (the capacitors shown inside the broken lines in the diagram) are used for phase compensation. Their capacitance is intended to stop oscillation when oscillation is caused by the status of the output capacitor. As such, they can be left open under normal circumstances.

Pin Functions

Pin No.	Pin name	Description
1	FB_GND	GND of output voltage setting pins FB0 and FB2. It is connected to GND for use when pin FB2 is used.
2	ENABLE	Output ON/OFF with an active-high polarity. When set to L, the current consumption is reduced to 10μA or less.
3	SS	Soft start time constant setting. The charge current is set to approx. 6.5μA and when a capacitor of 0.1μF is connected between this pin and GND, the output rises in approx. 12ms.
4	FB1	Test pin for verifying the internal reference voltage. It must be set to open for actual use.
5, 8, 10	V_{IN}	Power input. It is used with voltages ranging from 4.5V to 6V.
6, 9	SW	Inductor drive output
7	PGND	Power GND pin. This is the output GND. It is connected so that where at all possible, no impedance is shared with other GND pins (GND, FB_GND).
11	CBOOT	For generating the gate voltage of the internal high-side n-channel MOS transistor. A capacitor with a capacitance of at least 0.1μF (max. 2.2μF) is connected between this pin and the SW pin for use.
12	OERRAMP	Transconductance-type Error_Amp output. An integration constant is provided between this pin and GND to implement phase compensation.
13	FB2	Used to feed back the output voltage to this pin when the output voltage is to be set to 3.3V. In such a case, FB_GND is connected to GND. Refer to application circuit 1.
14	FB0	When the output voltage is to be set to a desired value, connect resistors between FB0 and GND and between FB0 and V_{OUT} to feed back the output voltage to this pin. In such a case, leave FB_GND and FB2 open. Refer to application circuit 2.
Heat sink fin	GND	Analog GND (connected to GND).

Input Equivalent Circuits

Pin No.	Pin Name	Equivalent Circuit
5, 8, 10	GND V_{IN}	
1 4 13 14	FB_GND FB1 FB2 FB0	

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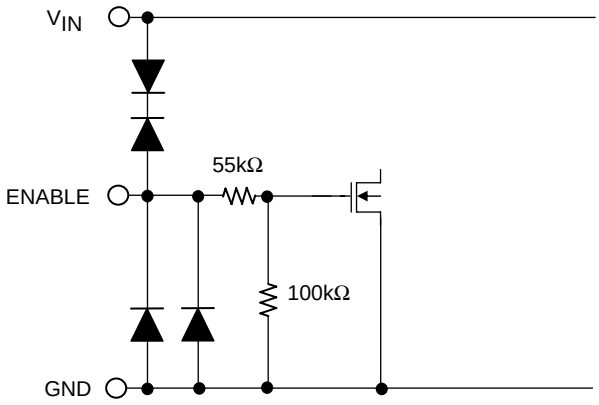
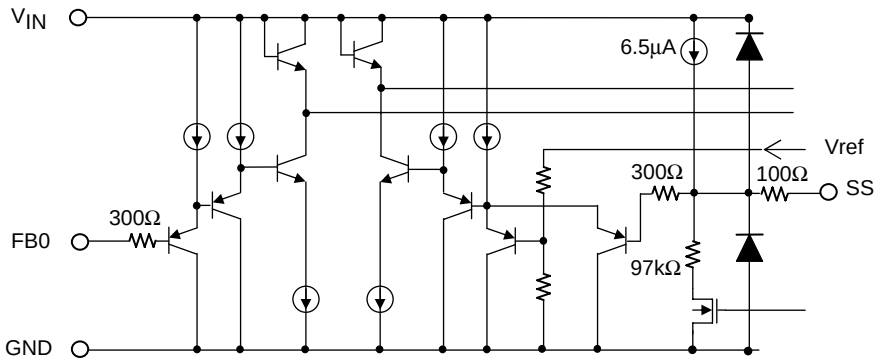
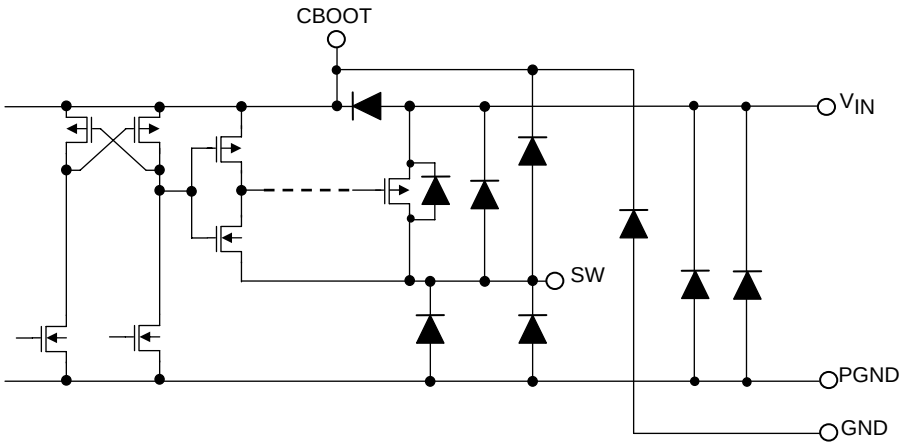
Pin No.	Pin Name	Equivalent Circuit
2	ENABLE	
3	SS	
6, 9 7 11	SW PGND CBOOT	
12	OERRAMP