

## FEATURES

- **Wide Operating Range: 3.5V to 100V**
- **Wide Monitoring Range: 3.5V to 98V**
- **Quiescent Current: 7 $\mu$ A**
- **Adjustable Threshold Range**
- **Internal High Value Resistive Dividers**
- $\pm 1.4\%$  (Max) Threshold Accuracy Over Temperature
- Polarity Selection
- 100V Rated Outputs
- Selectable Built-In Hysteresis
- 16-Lead MS and 8-Lead 3mm  $\times$  3mm DFN Packages

## APPLICATIONS

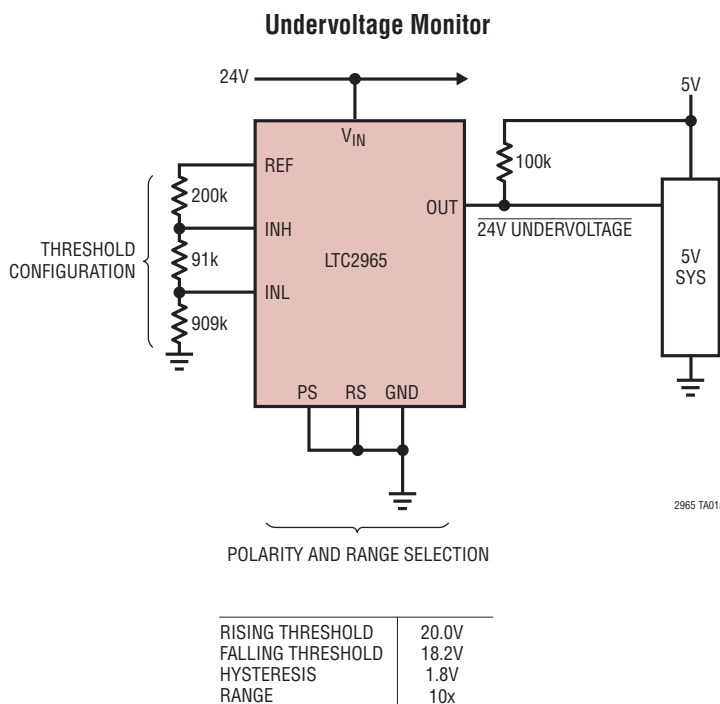
- Portable Equipment
- Battery-Powered Equipment
- Telecom Systems
- Automotive/Industrial Electronics

## DESCRIPTION

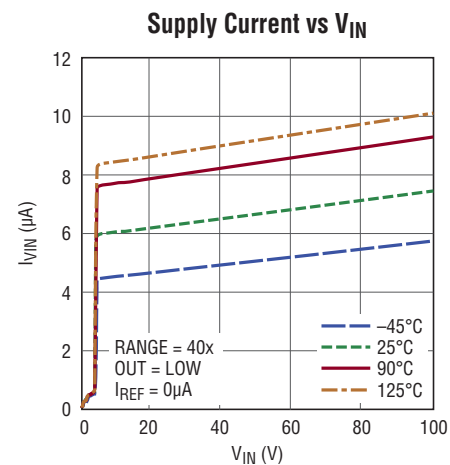
The **LTC<sup>®</sup>2965** is a low current, high voltage single channel voltage monitor. Internal high value resistors sense the input monitor pin providing a compact and low power solution for voltage monitoring. Two comparator reference inputs (INH and INL) are included to allow configuration of a high and low threshold using an external resistive divider biased from the on-chip reference. A range selection pin is provided to set the internal resistive divider for 10x or 40x scaling. The thresholds are scaled according to the range selection settings. Additionally, either INH or INL can be grounded to enable built-in hysteresis. Polarity selection pin allows the output to be inverted. The output is 100V capable and includes a 500k pull-up resistor to an internal supply.

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## TYPICAL APPLICATION



V <sub>IN</sub> MONITOR RANGE	RANGE SELECTION
3.5V to 24.5V	10x
14V to 98V	40x



# LTC2965

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

### Input Voltages

$V_{IN}$ .....	-0.3V to 140V
PS, RS .....	-0.3V to 6V
INH, INL .....	-0.3V to 6V

### Output Voltages

OUT .....	-0.3V to 140V
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### Average Currents

$V_{IN}$ .....	-20mA
OUT .....	±5mA
REF .....	±5mA
INH, INL .....	-1mA

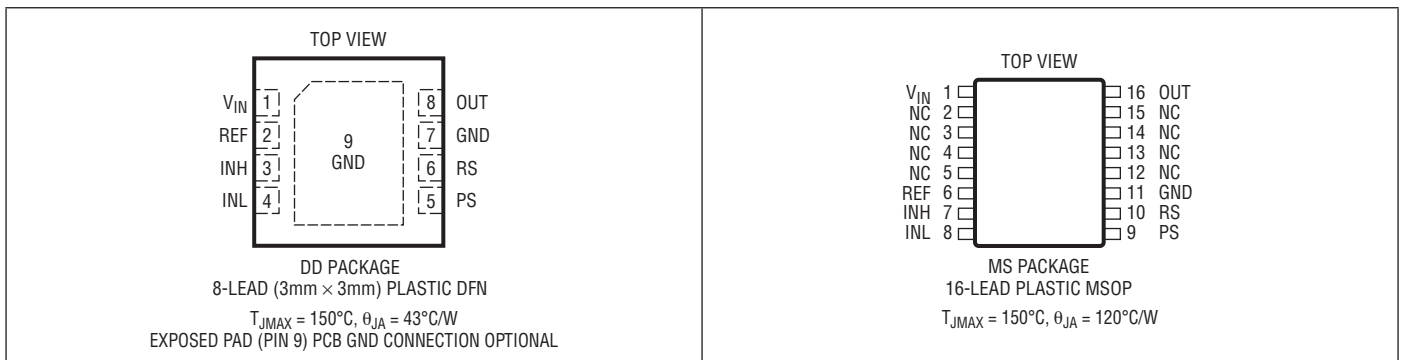
### Operating Ambient Temperature Range

LTC2965C .....	0°C to 70°C
LTC2965I .....	-40°C to 85°C
LTC2965H .....	-40°C to 125°C

### Storage Temperature Range .....

Lead Temperature (Soldering, 10 sec)..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION (<http://www.linear.com/product/LTC2965#orderinfo>)

### Lead Free Finish

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2965CDD#PBF	LTC2965CDD#TRPBF	LGМК	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2965IDD#PBF	LTC2965IDD#TRPBF	LGМК	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2965HDD#PBF	LTC2965HDD#TRPBF	LGМК	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC2965CMS#PBF	LTC2965CMS#TRPBF	2965	16-Lead Plastic MSOP	0°C to 70°C
LTC2965IMS#PBF	LTC2965IMS#TRPBF	2965	16-Lead Plastic MSOP	-40°C to 85°C
LTC2965HMS#PBF	LTC2965HMS#TRPBF	2965	16-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ ,  $R_S = \text{GND}$ ,  $P_S = \text{GND}$ ,  $I_{NH} = 1.2\text{V}$ ,  $I_{NL} = \text{GND}$  (Notes 1, 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input Supply Operating Range	$V_{IN}$	● 3.5		100	V
$V_{MON}$	$V_{IN}$ Monitor Range		3.5		98	V
$I_{VIN}$	$V_{IN}$ Input Supply Current	$V_{IN} = 100\text{V}$ , 40x	● 3	7	15	$\mu\text{A}$
$V_{UVLO}$	Undervoltage Lockout	$V_{IN}$ Rising	●		3	V
	Undervoltage Lockout Hysteresis	$V_{IN}$ Falling		70		mV

### Comparator Reference Input: INH, INL

$V_{CM}$	Comparator Common Mode Voltage		● 0.35		2.45	V	
$V_{ERR}$	$V_{IN}$ Error Voltage at 96V	$I_{NH} = V_{REF}$ , 40x $0.35\text{V} \leq I_{NH} \leq 2.4\text{V}$ , 40x	●	$\pm 250$	$\pm 1360$	mV	
	$V_{IN}$ Error Voltage at 24V	$I_{NH} = V_{REF}$ , 10x $0.35\text{V} \leq I_{NH} \leq 2.4\text{V}$ , 10x	●	$\pm 35$	$\pm 315$	mV	
$V_{OS}$	Comparator Offset Voltage	$I_{NH} = 0.35\text{V}$ , 10x	●	$\pm 1.9$	$\pm 3$	mV	
$AV_{ERR}$	Internal Resistive Divider Range Error	$I_{NH} = 2.4\text{V}$ , Range = 10x, 40x	●		$\pm 0.4$	%	
$V_{HYS}$	Comparator Built-in Hysteresis	$I_{NH} = \text{GND}$ , $I_{NL}$ Rising, $V_{IN} = 24\text{V}$	●	14	22	30	mV
		$I_{NL} = \text{GND}$ , $I_{NH}$ Falling, $V_{IN} = 24\text{V}$	●	-30	-22	-14	mV
$V_{HYTH}$	Built-in Hysteresis Enable Threshold		● 100		175	mV	
$t_{PD}$	$V_{IN}$ to OUT Comparator Propagation Delay	Overdrive = 10%, OUT Falling, 10x $I_{NH} = \text{GND}$ , $I_{NL} = 1.2\text{V}$	●	40	80	$\mu\text{s}$	
$I_{IN(LKG)}$	Input Leakage Current (INH, INL)	$V = 1.2\text{V}$ , I-Grade	●	$\pm 0.1$	$\pm 1$	nA	
		$V = 1.2\text{V}$ , H-Grade	●	$\pm 0.1$	$\pm 10$	nA	

### Reference: REF

$V_{REF}$	Reference Output Voltage	$I_{REF} \leq 100\mu\text{A}$ , $V_{IN} \geq 3.5\text{V}$	● 2.378	2.402	2.426	V
Noise	Reference Output Noise	100Hz to 100kHz		140		$\mu\text{V}_{RMS}$

### Control Inputs: RS, PS

$V_{TH}$	Select Input Threshold		● 0.4		1.4	V
$I_{LKG}$	Input Leakage Current	$V = 2.4\text{V}$	●		$\pm 100$	nA

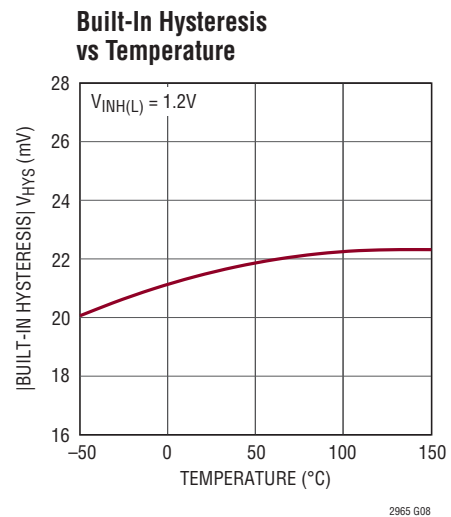
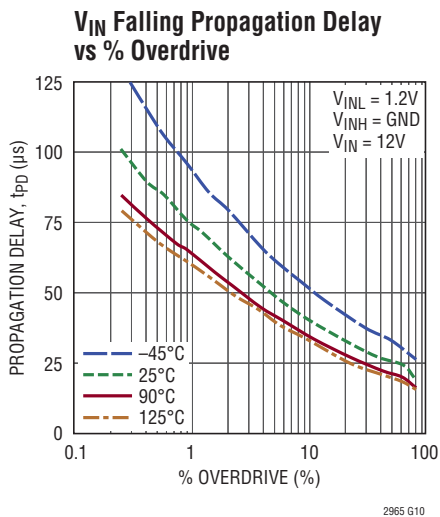
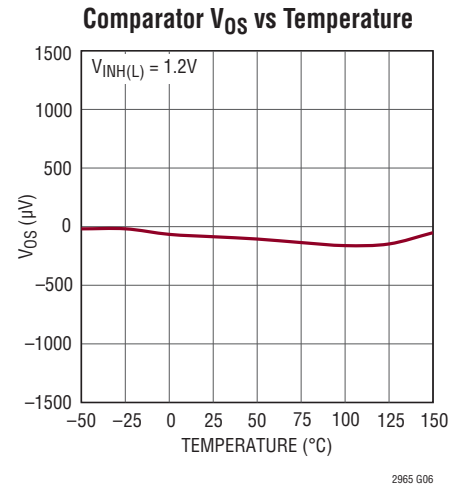
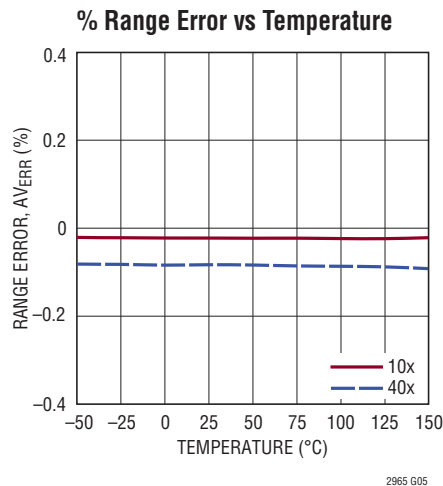
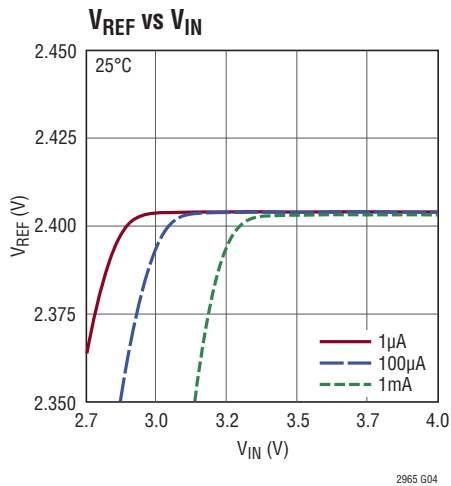
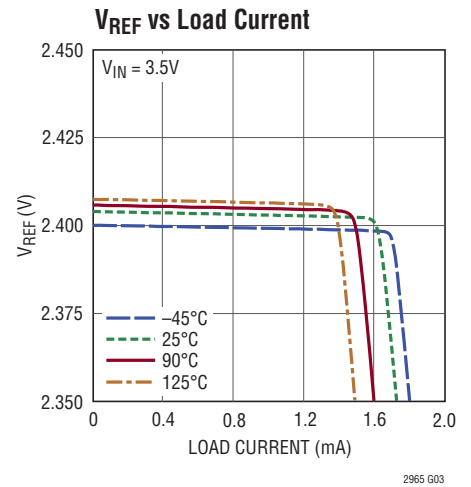
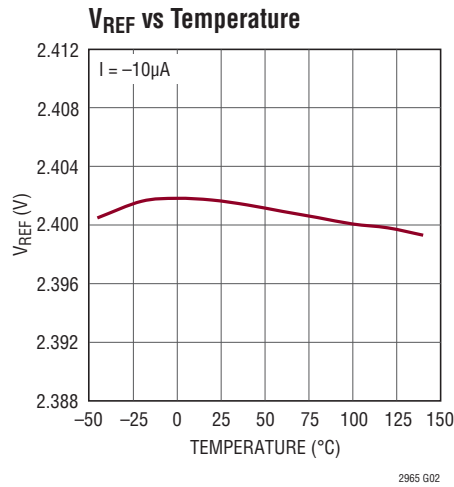
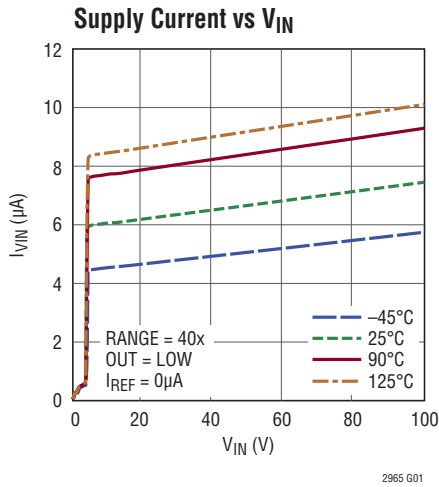
### Status Outputs: OUT

$V_{OL}$	Voltage Output Low	$V_{IN} = 1.25\text{V}$ , $I = 10\mu\text{A}$	●		100	mV	
		$V_{IN} = 3.5\text{V}$ , $I = 500\mu\text{A}$	●		400	mV	
$V_{OH}$	Voltage Output High	$V_{IN} = 3.5\text{V}$ , $I = -1\mu\text{A}$	●	2	2.375	2.75	V
		$V_{IN} \geq 4.5\text{V}$ , $I = -1\mu\text{A}$	●	2.8	3	4	V
$I_{OH}$	Output Current High	$V = \text{GND}$ , $V_{IN} = 3.5\text{V}$	●	-15	-7.5	-5	$\mu\text{A}$
$I_{O(LKG)}$	Leakage Current, Output High	$V = 100\text{V}$ , $V_{IN} = 6\text{V}$	●		$\pm 250$	nA	

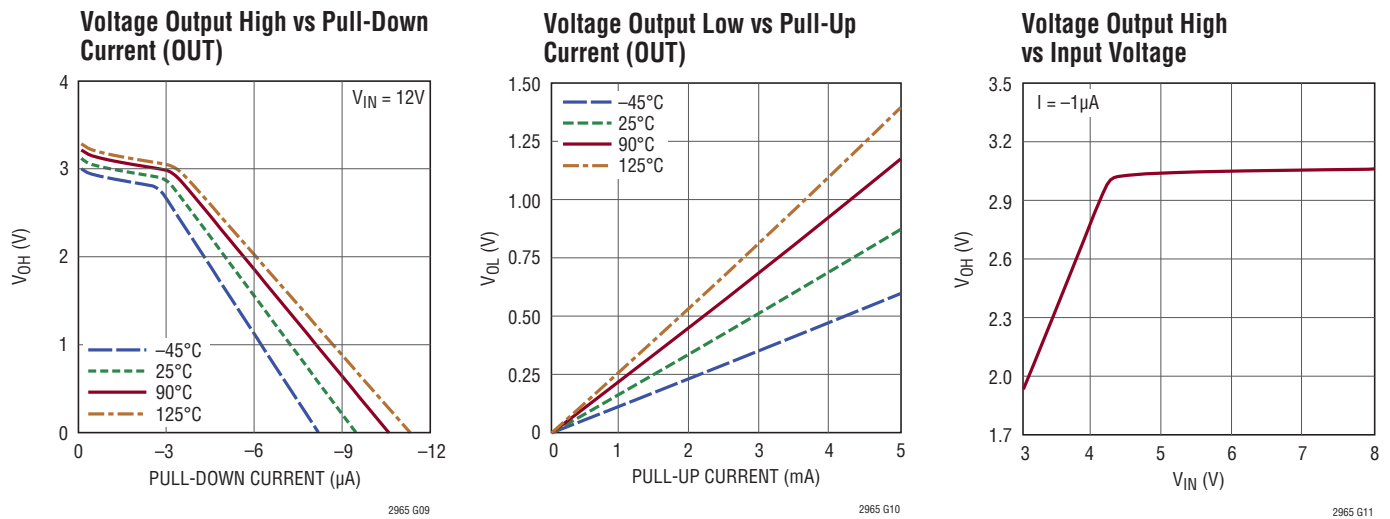
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

## TYPICAL PERFORMANCE CHARACTERISTICS



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**Exposed Pad (DD8 Only):** Exposed pad may be left floating or connected to device ground.

**GND:** Device Ground.

**INH:** High Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{IN}$  high or rising threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where high threshold for  $V_{IN}$  becomes  $INL + V_{HYS}$  scaled according to the RS pin configuration.

**INL:** Low Comparator Reference Input. Voltage on this pin is multiplied by the configured range setting to set the  $V_{IN}$  low or falling threshold. Keep within valid voltage range,  $V_{CM}$ , or tie to GND to configure built-in hysteresis where low threshold becomes  $INH - V_{HYS}$  scaled according to the RS pin configuration. Otherwise, INH-INL sets the hysteresis of the comparator. Oscillation will occur if  $INL > INH$  unless built-in hysteresis is enabled.

**OUT:** Comparator Output. OUT consists of a high voltage active pull-down and a gated, resistive ( $500k\Omega$ ) pull-up

to an internally generated supply between 3.5V and 5V depending on input supply voltage. Blocking circuitry at the pin allows the pin to be resistively pulled up to voltages as high as 100V without back conducting onto the internal supply of the part. Polarity with respect to the  $V_{IN}$  pin is configured using the polarity select pin, PS. OUT pulls low when the part is in UVLO.

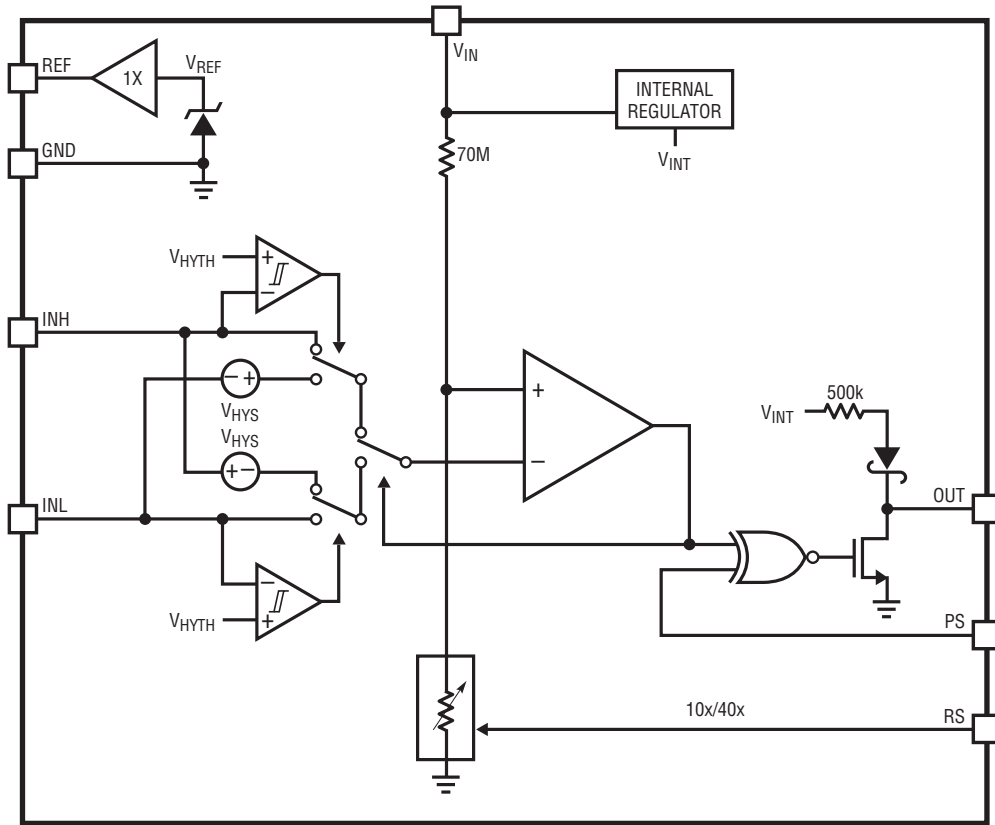
**PS:** Polarity Selection. Connect to REF or a voltage  $>V_{TH}$  to configure comparator output to be inverting with respect to  $V_{IN}$ . Otherwise connect pin to GND to configure comparator output to be noninverting with respect to  $V_{IN}$ .

**REF:** Reference Output.  $V_{REF}$  with respect to GND. Use a maximum of 1nF to bypass unless damping resistor is used.

**RS:** Range Select Input. RS selects 10x or 40x range. Connect to REF or GND to configure pin. (See Table 1)

**$V_{IN}$ :** Voltage Monitor and Supply Input. An internal high value resistive divider is connected to the pin. If  $V_{IN}$  falls below the UVLO threshold minus hysteresis, the output is pulled low. If  $V_{IN} < 1.2V$ , the logic state of the outputs cannot be guaranteed.

**BLOCK DIAGRAMS**



2965 BD

## OPERATION

The LTC2965 is a micropower single channel voltage monitor with a 100V maximum operating voltage. Its channel is comprised of an internal high value resistive divider and a comparator with a high voltage output. A reference voltage is provided to allow the thresholds to be set independently. This configuration has the advantage of being able to monitor very high voltages with very little current draw while threshold programming is done using low value resistors at low voltages. Integration of a resistive divider for high voltage sensing makes the LTC2965 a compact and low power solution for generating voltage status signals to a monitoring system.

A built-in buffered reference gives the monitor flexibility to operate independently from a high voltage supply without the requirement of additional low voltage biasing. The reference provides an accurate voltage from which a resistive divider to ground configures the threshold voltage for the internal comparator. In addition, the REF pin can be used as a logic high voltage for the range and polarity select pins.

The input voltage threshold at  $V_{IN}$  is determined by the voltage on the INH and INL pins which are scaled by the internal resistive divider. The LTC2965 offers two range settings to select from, 10x and 40x, using the RS pin. Use Table 1 to determine the correct configuration for a desired range setting. The polarity select pin, (PS), configures the OUT pin to be inverting or noninverting with respect to  $V_{IN}$  allowing the part to be configured for monitoring overvoltage and undervoltage conditions with either polarity output.

**Table 1.**

$V_{IN}$ MONITOR RANGE	RANGE SELECTION	RS
3.5V to 24.5V	10x	L
14V to 98V	40x	H

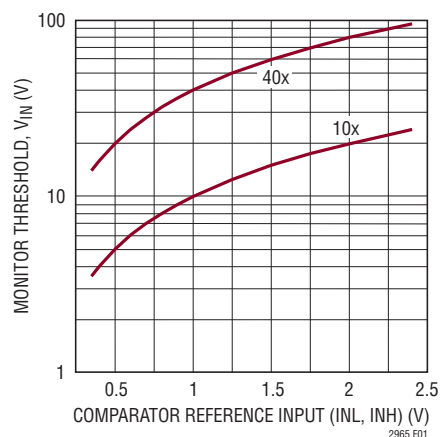
The INH pin determines the high or rising edge threshold for  $V_{IN}$ . If the monitored voltage connected to  $V_{IN}$  rises to the scaled INH voltage then the OUT pin is pulled high assuming PS is ground. Likewise, the INL pin determines the low or falling edge threshold for  $V_{IN}$  in each channel. If  $V_{IN}$  falls to the scaled INL voltage then the OUT pin is

pulled low assuming PS is ground. The amount of hysteresis referred to  $V_{IN}$  is the difference in voltage between INH and INL scaled according to the RS pin configuration. INH and INL have an allowable voltage range,  $V_{CM}$ . Figure 1 shows the allowable monitor voltage at  $V_{IN}$  for each range as a function of comparator reference input voltage (INL/INH).

Typically, an external resistive divider biased from REF is used to generate the INH and INL pin voltages. A built-in hysteresis feature requiring only two resistors can be enabled on either the  $V_{IN}$  rising edge by grounding INH or on the falling edge by grounding INL. For example, it is appropriate to ground INH to activate rising edge hysteresis if an accurate falling voltage threshold is required for undervoltage detection. Conversely, it is appropriate to ground INL for falling edge built-in hysteresis if an accurate overvoltage threshold is required. Do not ground both INH and INL. Oscillation occurs if  $V_{INL} > V_{INH}$  unless INH built-in hysteresis is enabled.

The high voltage OUT pins have the capability to be pulled up to a user defined voltage as high as 100V with an external resistor. The LTC2965 also includes an internal 500k pull-up resistor to an internal voltage between 3.5V and 5V depending on input voltage. (See  $V_{OH}$  in Electrical Characteristics).

If the  $V_{IN}$  pin falls below the UVLO threshold then the OUT pin is pulled low regardless of the PS pin state.



**Figure 1. Monitor Threshold vs Comparator Reference Inputs**

## APPLICATIONS INFORMATION

### Threshold Configuration

The LTC2965 channel monitors the voltage applied to the  $V_{IN}$  input. A comparator senses the  $V_{IN}$  pin on one of its inputs through the internal resistive divider. The other input is connected to INH/INL that is in turn biased with external resistive dividers off of the REF pin as shown in Figure 2a and 2b. The  $V_{IN}$  rising and falling thresholds are determined by:

$$V_{IN(RISE)} = RANGE \cdot V_{INH}$$

$$V_{IN(FALL)} = RANGE \cdot V_{INL}$$

Where RANGE is the configured range of the internal resistive divider. In order to set the threshold for the LTC2965, choose an appropriate range setting for the desired  $V_{IN}$  voltage threshold such that the INH and INL voltages are within the specified common mode range,  $V_{CM}$ . For example, if a falling threshold of 18V is desired for monitoring a 24V power supply then a range greater than 10x is allowed. However, to maximize the accuracy of the  $V_{IN}$  threshold the smallest acceptable range is used, 10x in this case. To implement 2V of hysteresis referred to  $V_{IN}$  this means:

$$V_{INH} = 2V, V_{INL} = 1.8V$$

With 10x range the  $V_{IN}$  thresholds are:

$$V_{IN(RISE)} = 20V, V_{IN(FALL)} = 18V$$

One possible way to configure the thresholds is by using three resistors to set the voltages on INH and INL. See Figure 2a. The solution for R1, R2 and R3 provides three equations and three unknowns. Maximum resistor size is governed by maximum input leakage current. The maximum input leakage current below 85°C is 1nA. For a maximum error of 1% due to both input currents, the resistive divider current should be at least 100 times the sum of the leakage currents, or 0.2µA.

If in this example, a leakage current error of 0.1% is desired then the total divider resistance is 1.2MΩ which results in a current of 2µA through this network. For  $R_{SUM} = 1.2M\Omega$

$$R_{SUM} = R1 + R2 + R3$$

$$R1 = \frac{(V_{INL} \cdot R_{SUM})}{V_{REF}} = \frac{(1.8V \cdot 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined from:

$$R2 = \frac{(V_{INH} \cdot R_{SUM})}{V_{REF}} - R1 \\ = \frac{(2V \cdot 1.2M\Omega)}{2.402V} - 909k\Omega = 90.2k\Omega$$

The closest 1% value is 90.9kΩ. R3 can be determined from  $R_{SUM}$ :

$$R3 = R_{SUM} - R1 - R2 = 1.2M\Omega - 909k\Omega - 90.9k\Omega \\ = 200.1k\Omega$$

The closest 1% value is 200kΩ. Plugging the standard values back into the equations yields the design values for the  $V_{INH}$  and  $V_{INL}$  voltages:

$$V_{INH} = 2.002V, V_{INL} = 1.819V$$

The corresponding threshold voltages are:

$$V_{IN(RISE)} = 20.01V, V_{IN(FALL)} = 18.19V$$

Another possible way to configure the thresholds is with independent dividers using two resistors per threshold to set the voltages on INH and INL. See Figure 2b. Care must be taken such that the thresholds are not set too close to each other, otherwise the mismatch of the resistors may cause the voltage at INL to be greater than the voltage at INH which may cause the comparator to oscillate.

As in the previous example, if  $R_{SUM} = 1.2M\Omega$  is chosen and the target for  $V_{INL}$  is 1.8V:

$$R_{SUM} = R1 + R2$$

$$R1 = \frac{(V_{INL} \cdot R_{SUM})}{V_{REF}} = \frac{(1.8V \cdot 1.2M\Omega)}{2.402V} = 899.5k\Omega$$

The closest 1% value is 909kΩ. R2 can be determined by:

$$R2 = (V_{REF} - V_{INL}) \cdot \frac{R1}{V_{INL}} \\ = (2.402V - 1.8V) \cdot \frac{(909k\Omega)}{1.8V} = 304k\Omega$$



## APPLICATIONS INFORMATION

The closest 1% value is 301kΩ. Plugging the standard values back into the equation for  $V_{INL}$  yields the design voltage for  $V_{INL}$ :

$$V_{INL} = \frac{(R1 \cdot V_{REF})}{(R1 + R2)} = \frac{(909k\Omega \cdot 2.402V)}{(301k\Omega + 909k\Omega)} = 1.804V$$

At this point in the independent divider example only the values required to set the voltage at INL have been found. Repeat the process for the INH input by substituting the above equations with  $V_{INH}$  for  $V_{INL}$ , R3 for R1, R4 for R2 and  $V_{INH} = 2.0V$ .

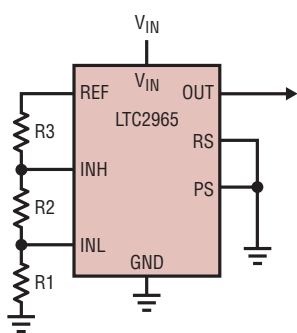


Figure 2a. Three-Resistor Threshold Configuration

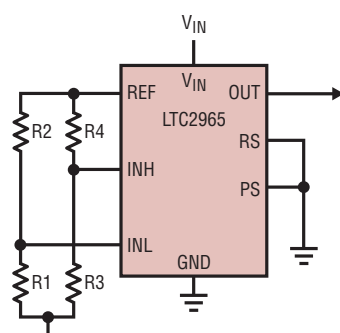


Figure 2b. Two-Resistor Threshold Configuration

### Using Built-In Hysteresis

The LTC2965 has the capability of simplifying the threshold configuration such that only two resistors are required. The device pins can be configured to select a built-in hysteresis voltage,  $V_{HYS}$ , which can be applied to either the rising or falling threshold depending on whether the INH or INL pin is grounded. Note that the hysteresis voltage at each range setting remains at a fixed value. Figure 3 introduces examples of each configuration. For example, if INH is biased from an external divider and the INL pin is grounded, then hysteresis is enabled on the low or falling threshold. The low threshold is then  $-V_{HYS}$  relative to the high threshold determined by INH. Figure 3a introduces built-in hysteresis on the rising edge because INH is pulled to ground. A two-resistor network, R1 and R2, is used to set the voltage on INL using:

$$\frac{R2}{R1} = \frac{V_{REF}}{V_{INL}} - 1$$

Using built-in hysteresis, the  $V_{INA}$  thresholds are:

$$V_{IN(RISE)} = RANGE \cdot (INL + V_{HYS})$$

$$V_{IN(FALL)} = RANGE \cdot INL$$

Figure 3b introduces built-in hysteresis on the falling edge because INL is pulled to ground. Similarly, a two-resistor network, R3 and R4, is used to set the voltage on INH using:

$$\frac{R4}{R3} = \frac{V_{REF}}{V_{INH}} - 1$$

Using built-in hysteresis the  $V_{IN}$  thresholds are:

$$V_{IN(RISE)} = RANGE \cdot INH$$

$$V_{IN(FALL)} = RANGE \cdot (INH - V_{HYS})$$

Consider  $V_{INH} = 2V$  with built-in hysteresis activated on the falling edge. For 10x range, 1.1% falling hysteresis is obtained. If a larger percentage of hysteresis is desired then  $V_{INH}$  is alternatively set to 0.5V and the range is selected to be 40x to obtain the same  $V_{IN}$  threshold but with 4.4% falling hysteresis. The amount of built-in hysteresis is scaled according to Table 2. If more hysteresis is needed then it is implemented in the external resistive divider as described in the Threshold Configuration section.

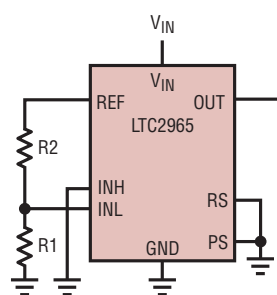


Figure 3a. Rising Edge Built-In Hysteresis

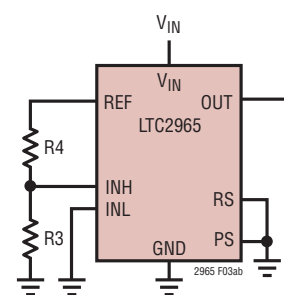


Figure 3b. Falling Edge Built-In Hysteresis

Table 2. Built-In Hysteresis Voltage vs Range

RANGE	$V_{IN}$ REFERRED BUILT-IN HYSTERESIS
10x	220mV
40x	880mV

## APPLICATIONS INFORMATION

### Error Analysis

$V_{IN}$  thresholds are subject to the following errors:

- REF Voltage Variation ( $\Delta V_{REF}$ )
- Comparator Offset ( $V_{OS}$ )
- Internal Divider Range Error ( $A_{VERR}$ )
- External Resistive Divider Error ( $A_{XERR}$ )

The effect these errors have on the  $V_{IN}$  threshold is expressed by:

$$V_{ERR} = \text{RANGE} \cdot \left[ \pm V_{OS} \pm \Delta V_{REF} \cdot \frac{V_{INH(L)}}{V_{REF}} \pm V_{INH(L)} \cdot A_{XERR} \right] \\ \pm \text{RANGE} \cdot A_{VERR} \cdot V_{INH(L)}$$

$$A_{XERR} = 2 \cdot \frac{\text{TOLERANCE}}{100} \cdot \left( 1 - \frac{V_{INH(L)}}{V_{REF}} \right)$$

External divider error is determined by the percentage tolerance values of the resistors. If 1% tolerance resistors are used in the external divider then there is a 2% worst-case voltage error associated with it. The effects of comparator offset and  $V_{REF}$  voltage are uncorrelated with each other. Therefore, a Root-Sum-Square can be applied to the error voltage referred to  $V_{IN}$ . Using the example from Threshold Configuration and assuming 1% resistors implement the external resistive divider, the falling  $V_{IN}$  threshold of approximately 18V has an error tolerance of:

$$V_{ERR(REF)} = (\text{RANGE}) \left( \pm \Delta V_{REF} \cdot \frac{V_{INL}}{V_{REF}} \right) \\ = (10) \cdot \left( \pm 24\text{mV} \cdot \frac{1.8\text{V}}{2.402\text{V}} \right) = \pm 180\text{mV}$$

$$V_{ERR(EXT)} = (\text{RANGE}) \left( \pm V_{INL} \cdot 2 \cdot 0.01 \cdot \left( 1 - \frac{V_{INL}}{V_{REF}} \right) \right) \\ = (10) \cdot (\pm 1.8\text{V} \cdot 0.005) = \pm 90\text{mV}$$

$$V_{ERR(VOS)} = (\text{RANGE}) (\pm \Delta V_{OS}) = (10) \cdot (\pm 16\text{mV}) = \pm 160\text{mV}$$

$$V_{ERR(RS)} = (\text{RANGE}) (\pm A_{VERR}) (\pm V_{INL}) \\ = (10) \cdot (\pm 0.004) \cdot (1.8\text{V}) = \pm 72\text{mV}$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} \\ = \sqrt{(\pm 180\text{mV})^2 + (\pm 90\text{mV})^2 + (\pm 160\text{mV})^2 + (\pm 72\text{mV})^2} \\ = \pm 267\text{mV}$$

The actual  $V_{IN}$  falling threshold has an error tolerance of  $\pm 267\text{mV}$  or  $\pm 1.48\%$ .

### Improving Threshold Accuracy

The biggest threshold error terms are:

- External Resistive Divider Accuracy
- REF Voltage Variation

Even using 1% tolerance resistors, external resistive divider accuracy still accounts for as much as  $\pm 2\%$  threshold error while REF voltage variation accounts for  $\pm 1\%$  threshold error. In order to minimize these threshold error terms, an external reference can be used to set the thresholds for INH/INL as shown in Figure 4. An LT6656-2.048 has an initial accuracy of 0.05% and provides bias via the 0.1% resistive divider network for INH and INL. It is biased off of the LTC2965 REF pin. The threshold error tolerance is calculated using the method described in the Typical Applications section with  $\Delta V_{REF} = \pm 1.024\text{mV}$  given the initial accuracy of the LT6656 2.048V output and using 0.1% tolerance resistors for the external divider.

$$V_{ERR(REF)} = (\text{RANGE}) \left( \pm \Delta V_{REF} \cdot \frac{V_{INL}}{V_{REF}} \right) \\ = (10) \cdot \left( \pm 1.024\text{mV} \cdot \frac{1.8\text{V}}{2.048\text{V}} \right) = \pm 9\text{mV}$$

$$V_{ERR(EXT)} = (\text{RANGE}) \left( \pm V_{INL} \cdot 2 \cdot 0.001 \cdot \left( 1 - \frac{V_{INL}}{V_{REF}} \right) \right) \\ = (10) \cdot (\pm 1.8\text{V} \cdot 0.0005) = \pm 9\text{mV}$$

$$V_{ERR(VOS)} = (\text{RANGE}) (\pm \Delta V_{OS}) = (10) \cdot (\pm 1.6\text{mV}) = \pm 16\text{mV}$$

$$V_{ERR(RS)} = (\text{RANGE}) (\pm A_{VERR}) (\pm V_{INL}) \\ = (10) \cdot (\pm 0.004) \cdot (1.8\text{V}) = \pm 72\text{mV}$$

$$V_{ERR} = \sqrt{V_{ERR(REF)}^2 + V_{ERR(EXT)}^2 + V_{ERR(VOS)}^2 + V_{ERR(RS)}^2} \\ = \sqrt{(\pm 9\text{mV})^2 + (\pm 9\text{mV})^2 + (\pm 16\text{mV})^2 + (\pm 72\text{mV})^2} \\ = \pm 75\text{mV}$$

The resulting  $V_{IN}$  threshold error is reduced to  $\pm 0.42\%$  from  $\pm 1.48\%$  in the previous error analysis example.

## APPLICATIONS INFORMATION

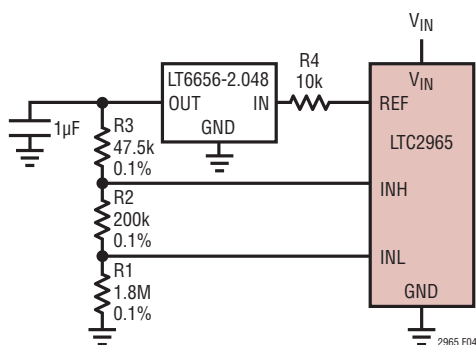


Figure 4. Reducing  $V_{IN}$  Threshold Error

### Output Configuration with Polarity Selection

The OUT pin may be used with a wide range of user-defined voltages up to 100V with an external resistor. Select a resistor compatible with desired output rise time and load current specifications. When the status outputs are low, power is dissipated in the pull-up resistors. An internal pull-up is present if the OUT pins are left floating or if low power consumption is required. The internal pull-up resistor does not draw current if an external resistor pulls OUT up to a voltage greater than  $V_{OH}$ .

If PS is connected to ground, the comparator output is noninverting. This means that OUT pulls low when  $V_{IN}$  falls below the scaled INL voltages. OUT is released after  $V_{IN}$  rises above the scaled INH voltage. Likewise, if PS is connected up to REF or a voltage  $> V_{TH}$ , the comparator output is inverting. This means that OUT pulls low when  $V_{IN}$  rises above the scaled INH voltage and is released when  $V_{IN}$  falls below the scaled INL voltage.

If the  $V_{IN}$  pin falls below the UVLO threshold minus hysteresis, the output is pulled to ground. The output is guaranteed to stay low for  $V_{IN} \geq 1.25V$  regardless of the output logic configuration.

It is recommended that circuit board traces associated with the OUT pin be located on a different layer than those associated with the INH/INL and REF pins where possible to avoid capacitive coupling.

### Hot Swap™ Events

The LTC2965 can withstand high voltage transients up to 140V. However, when a supply voltage is abruptly

connected to the input resonant ringing can occur as a result of series inductance. The peak voltage could rise to 2x the input supply, but in practice can reach 2.5x if a capacitor with a strong voltage coefficient is present. Circuit board trace inductances of as little as 10nH can produce significant ringing. Ringing beyond the absolute maximum specification can be destructive to the part and should be avoided whenever possible. One effective means to eliminate ringing seen at the  $V_{IN}$  pins and to protect the part is to include a 1k $\Omega$  to 5k $\Omega$  resistance between the monitored voltage and the  $V_{IN}$  pin as shown in Figure 5. This provides damping for the resonant circuit. If there is a decoupling capacitor on the  $V_{IN}$  pins the time constant formed by the RC network should be considered.

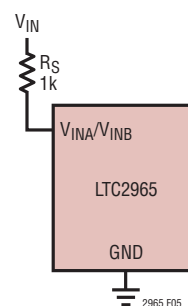


Figure 5. Hot Swap Protection

### High Voltage Pin Creepage/Clearance Options

Appropriate spacing between component lead traces is critical to avoid flashover between conductors. There are multiple industry and safety standards that have different spacing requirements depending on factors such as operating voltage, presence of conformal coat, elevation, etc. The LTC2965 is available in a 16-lead MSOP package which offers landing clearance of at least 0.79mm (0.031in). The package incorporates unconnected pins between all adjacent high voltage and low voltage pins to maximize PC board trace clearance. For voltages  $>30V$  the MSOP should be used, otherwise the smaller or DFN is sufficient when clearance is not an issue. For more information, refer to the printed circuit board design standards described in IPC2221 and UL60950.

## APPLICATIONS INFORMATION

### Voltage Reference

The REF pin is a buffered reference with a voltage of  $V_{REF}$  referenced to GND. A bypass capacitor up to 1000pF in value can be driven by the REF pin directly. Larger capacitances require a series resistance to dampen the transient response as shown in Figure 6A. If a resistive divider is already present then the bypass capacitor can be connected to the INH or INL pin as shown in Figure 6B. Figure 6C shows the resistor value required for different capacitor values to achieve critical damping. Bypassing the reference can help prevent false tripping of the comparators by preventing glitches on the INH/INL pins. Figure 7 shows the reference load transient response. Figure 8 shows the reference line transient response. If there is a decoupling capacitor on the INH/INL pin the time constant formed by the RC network should be considered. Use a capacitor with a compatible voltage rating.

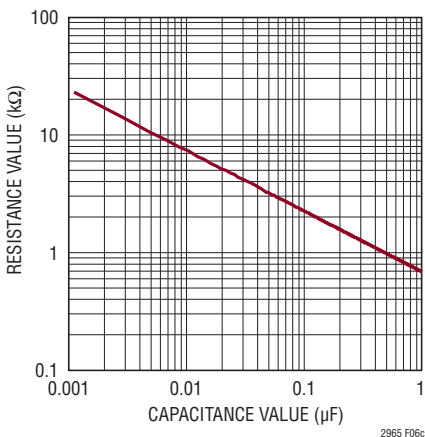
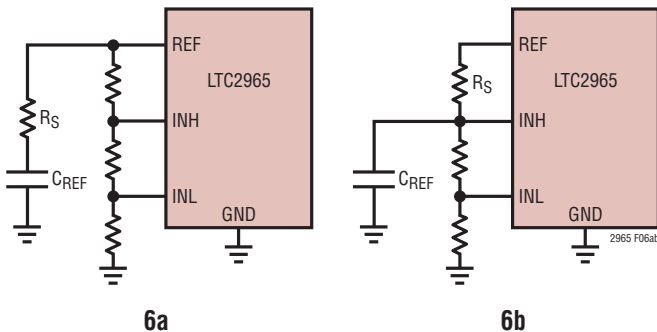


Figure 6. Using Series Resistance to Dampen REF Transient Response

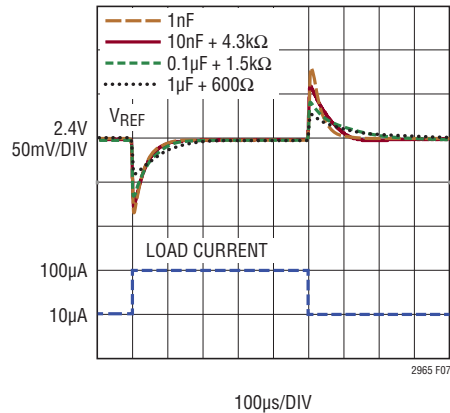


Figure 7.  $V_{REF}$  Load Transient

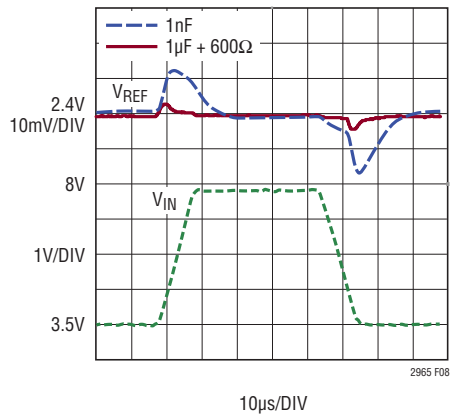


Figure 8.  $V_{REF}$  Line Transient

## TYPICAL APPLICATIONS

### Negative Voltage Monitor with Output Level Shift

Figure 9 illustrates an LTC2965 configured to monitor a -15V supply with a level-shifted output to a 5V supply. Q1 buffers the digital input of the 5V system from the -15V supply and prevents UV from going below GND. The OUT pin drives the base of Q1 through a resistor network comprised of R3 and R4. Keep  $R4/R3 \geq 0.4$  to ensure there is proper base current to pull UV to ground. If an exposed pad is present it should be tied to the LTC2965 GND pin or left open.

### Current Sink/Source

The LTC2965 can be used as a high voltage current source or a current sink as shown in Figure 10. The current is determined by placing a resistive load,  $R_{SET}$ , on the REF pin. The total current is then  $V_{REF}/R_{SET} + I_{VA}$  because the bias current of the part adds a small error term. Part of the bias current is the internal resistive divider which is approximately  $78M\Omega$  with the RS pin configured to 10x.

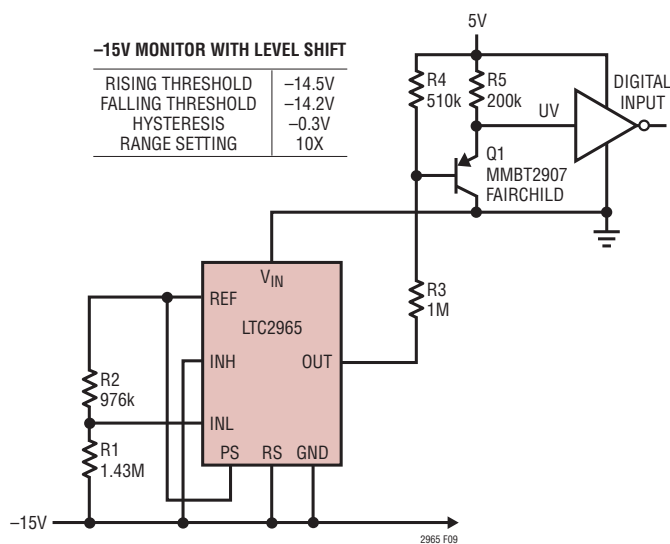


Figure 9. Negative Voltage Monitor with Output Level Shift to a 5V Digital Input

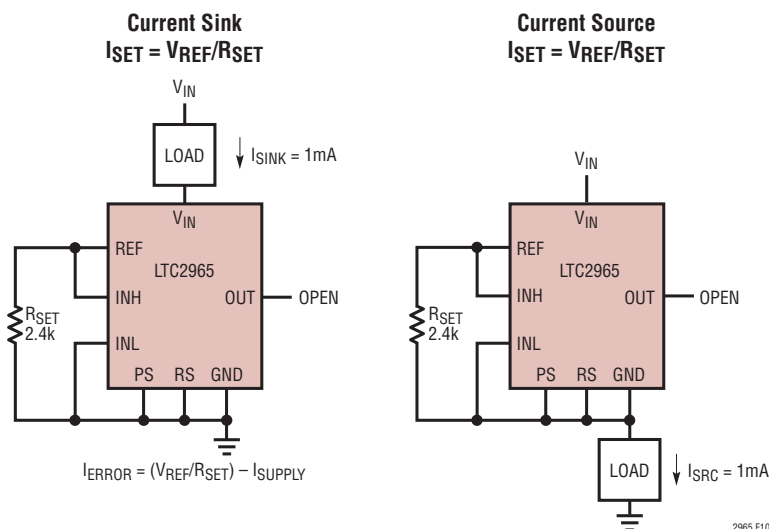


Figure 10. LTC2965 Configured as High Voltage Current Source

## TYPICAL APPLICATIONS

Configure the current to be no greater than 1mA to ensure that the REF voltage stays within  $\pm 1\%$  tolerance. Current values larger than 1mA exceed the REF buffer's load regulation capability and cause the REF voltage to drop out of regulation.

### Shunt Mode Hysteretic Regulator

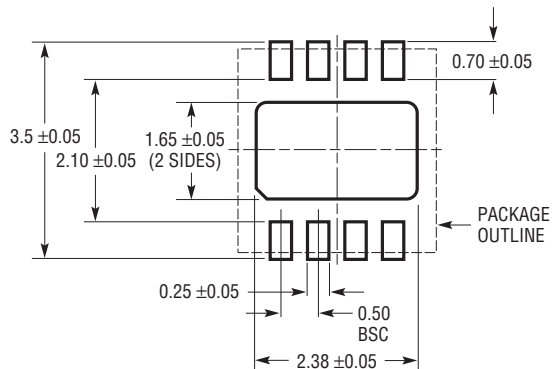
Figure 11 shows the LTC2965 used as the controller for a shunt mode hysteretic regulator to manage a battery-based solar power system. When the battery voltage reaches a

lower float limit of 13.7V Q1 turns off and the solar panel current passes through to the battery and load. Once the battery voltage rises to the upper charging limit of 14.7V, Q1 turns on shorting the solar panel to ground with D1 isolating the battery from the shunt path. The upper and lower thresholds are generated from the on-chip reference as a separate external divider to set INH and INL and scaled by 10x. The charging thresholds are temperature compensated by an NTC thermistor over a 0°C to 50°C range.

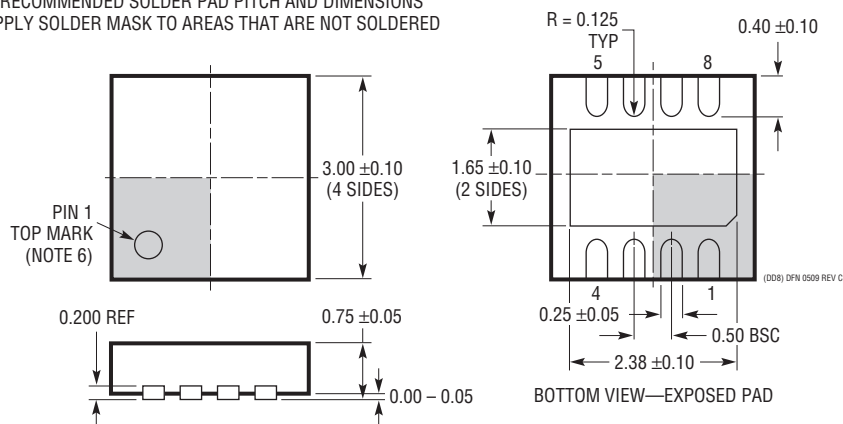
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2965#packaging> for the most recent package drawings.

### DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



#### NOTE:

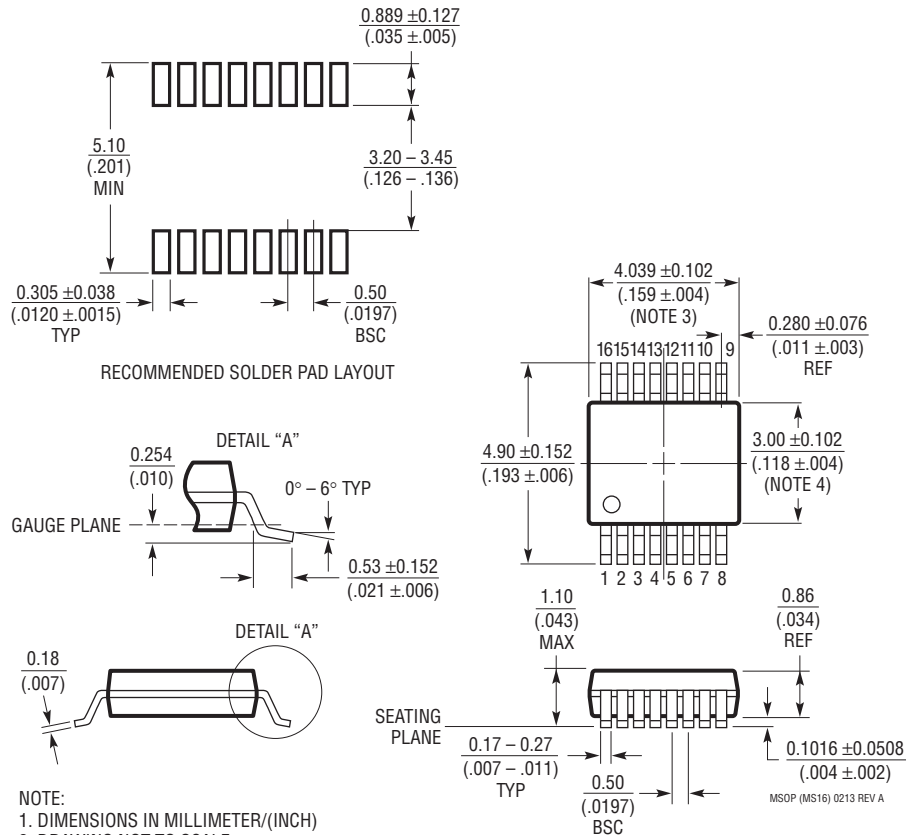
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2965#packaging> for the most recent package drawings.

### MS Package 16-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1669 Rev A)



**NOTE:**

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

MSOP (MS16) 0213 REV A



## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Fixed typos	3, 4, 10 – 12
B	03/16	Added Absolute Maximum Rating for INH and INL Pins	2

## TYPICAL APPLICATION

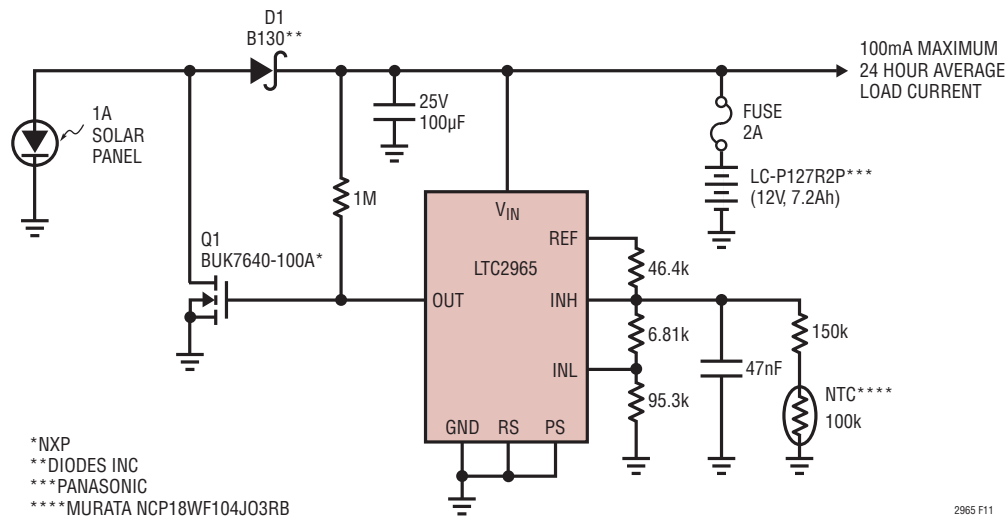


Figure 11. Shunt Mode Hysteretic Regulator

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC1326</a>	Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold ( $\pm 0.75\%$ ) and ADJ
<a href="#">LTC1440/LTC1441/LTC1442</a>	Ultralow Power Single/Dual Comparator with Reference	Adjustable Hysteresis, 3mm $\times$ 3mm $\times$ 0.75mm DFN Package
<a href="#">LTC1726/LTC1727/LTC1728</a>	Micropower Triple Supply Monitor	Adjustable Reset and Watchdog Timeouts
<a href="#">LTC1985</a>	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
<a href="#">LTC2900/LTC2901/LTC2902</a>	Programmable Quad Supply Monitor	Adjustable Reset, Watchdog Timer and Tolerance, 10-Lead MSOP and DFN Packages
<a href="#">LTC2903</a>	Precision Quad Supply Monitor	6-Lead SOT-23 and DFN Packages
<a href="#">LTC2904/LTC2905/LTC2906/LTC2907</a>	Three-State Programmable Precision Dual Supply Monitor	8-Lead SOT-23 and DFN Packages
<a href="#">LTC2908</a>	Precision Six-Supply Monitor (Four Fixed and Two Adjustable)	8-Lead TSOT-23 and DFN Packages
<a href="#">LTC2909/LTC2919</a>	Precision Triple/Dual Input UV, OV and Negative Voltage Monitor	Shunt Regulated $V_{CC}$ Pin, Adjustable Threshold and Reset
<a href="#">LTC2910</a>	Octal Positive/Negative Voltage Monitor	Separate $V_{CC}$ Pin, Eight Inputs, Up to Two Negative Monitors Adjustable Reset Timer, 16-Lead SSOP and DFN Packages
<a href="#">LTC2912/LTC2913/LTC2914</a>	Single/Dual/Quad UV and OV Voltage Monitors	Separate $V_{CC}$ Pin, Adjustable Reset Timer
<a href="#">LTC2915/LTC2916/LTC2917/LTC2918</a>	Single Voltage Supervisors with 27 Pin-Selectable Thresholds	Manual Reset and Watchdog Functions, 8- and 10-Lead TSOT-23, MSOP and DFN Packages
<a href="#">LTC2966</a>	100V Micropower Dual Voltage Monitor	1.75V to 98V Monitoring Range, 3.5V to 100V Operating Range, 7 $\mu$ A Quiescent Current
<a href="#">LTC2960</a>	36V Nano-Current Two Input Voltage Monitor	36V, 850nA Quiescent Current, 2mm $\times$ 2mm 8-Lead DFN and TSOT-23 Packages
<a href="#">LT6700</a>	Micropower Dual Comparator with 400mV Reference	SOT-23, 2mm $\times$ 3mm DFN Package