Document Number: MM912F634ER
Rev. 8.0, 6/2015

MM912F634, Silicon Analog Mask (M91W) / Digital Mask (M33G) Errata

Introduction

This mask set errata applies to the Analog mask M91W for these products:

Package	Part Number	Analog Mask ID	Analog Pass	MCU Mask ID
48 LQFP-EP	MM912F634BV1AE	DA04M91W	2.3	DW33634M33G01
	MM912F634CV1AE	DA05M91W	2.4	DW33634M33G01
	MM912F634DV1AE	DA06M91W	2.5	DW33634M33G01
	MM912F634CV2AE	DA05M91W	2.4	DW33634M33G01
	MM912F634DV2AE	DA06M91W	2.5	DW33634M33G01
48 LQFP	MM912F634CV2AP	DA05M91W	2.4	DW33634M33G01
	MM912F634DV2AP	DA06M91W	2.5	DW33634M33G01

1 Device Revision Identification

The device revision is indicated by a 1-character code after the device code. For instance the “C” in the “MM912F634CV2AE” indicates revision 2.4. All standard devices are marked with a device identification and build information code.

2 Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1125”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1125” indicates the 25th week of the year 2011.

3 Device Part Number Prefixes

Some device samples are marked with a PM prefix. A PM prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MM prefix.

4 Analog Mask (M91W) Errata

Silicon Revision Register - SRR

The analog die contains a silicon revision register to read the actual revision information.

- Mask M91W-E corresponds to silicon revision 2.3;
- Mask M91W-F corresponds to silicon revision 2.4;
- Mask M91W-G corresponds to silicon revision 2.5;

The actual revision of the analog die is available in the SRR (Silicon Revision Register), accessible through the Die-to-Die interface.

Register Details

Offset [(1)] 0xF4 Access: Read only

		7	6	5	4	3	2	1	0
	R	0	0	0	0	FMREV		MMREV	
	W								
Default Values	M91W-E	0	0	0	0	0	1	1	1
	M91W-F	0	0	0	0	0	1	1	0
	M91W-G	0	0	0	0	1	1	0	0

Notes

1. Offset related to 0x0200 for blocking access and 0x300 for non blocking access, within the global address space

Field	Description
3-2 FMREV	MM912F634 analog die Silicon Revision Register - These bits represent the revision of Silicon of the analog die. They are incremented for every full mask or metal mask issued of the device. One number is set for one revision of the silicon of the analog die.
1-0 MMREV	

NOTE

All the following errata items are valid for all silicon revisions unless explicitly noted.

Multiple Readings of the ADC Bandgap Channel

General Description

Multiple (>4) consecutive conversions of Channel 14 cause the Low-side drivers to turn off.

Failure Mechanism

The Channel 14 conversion samples the independent internal bandgap reference (bg1p25sleep). Charging the sample capacitor leads to unintended decrease of the reference voltage. As the reference is used as source for the VREG high voltage detection threshold, the decreased reference leads to a decreased high voltage threshold while the actual voltage regulator output is within its operating range. This will cause the VREG-HV mechanism for Low-side shutdown to be activated (documented in the data sheet, LS - section).

Workaround / Solution

No continuous conversion must be performed on channel 14.
The maximum of 4 consecutive channel14 readings within a 400 μs cycle must not be exceeded.

Low-side Control Enable (LSCEN) Register not resetting on VREG Overvoltage Condition

General Description

The Low-side Control Enable (LSCEN) register is reset only after LVR, LVRX and POR. It is also supposed to reset in case of an VREG Over-voltage event. See Figure 1.

Failure Mechanism

A digital implementation issue prevents the LSCEN register from resetting in case of a VREG high voltage condition. This register was implemented to create a secondary deactivation stage for the Low-side drives, verifying the VDD-Digital and the Sleep2p5 Digital circuitry is functional after a VREG high voltage.
The Shutdown of the LS drivers is still established via the VREG OVERVOLTAGE FLAG and has to be acknowledged by the Software (IRQ optional).
The basic intention of the feature is still present as a functional VDD-Digital and the Sleep2p5 Digital circuitry is still required for the LS to be active. Other than specified, the register will not reset in case of a high-voltage condition and therefore would not need to be written to reactivate the Low-side drivers.

Workaround / Solution

This feature is listed for correction in case of future mask corrections. It is recommended to maintain the register write LSCEN=0x5 to re-enable the Low-side drivers to assure software compatibility with the potential silicon fix.
Other than that, the intended security function of the feature is still in place.

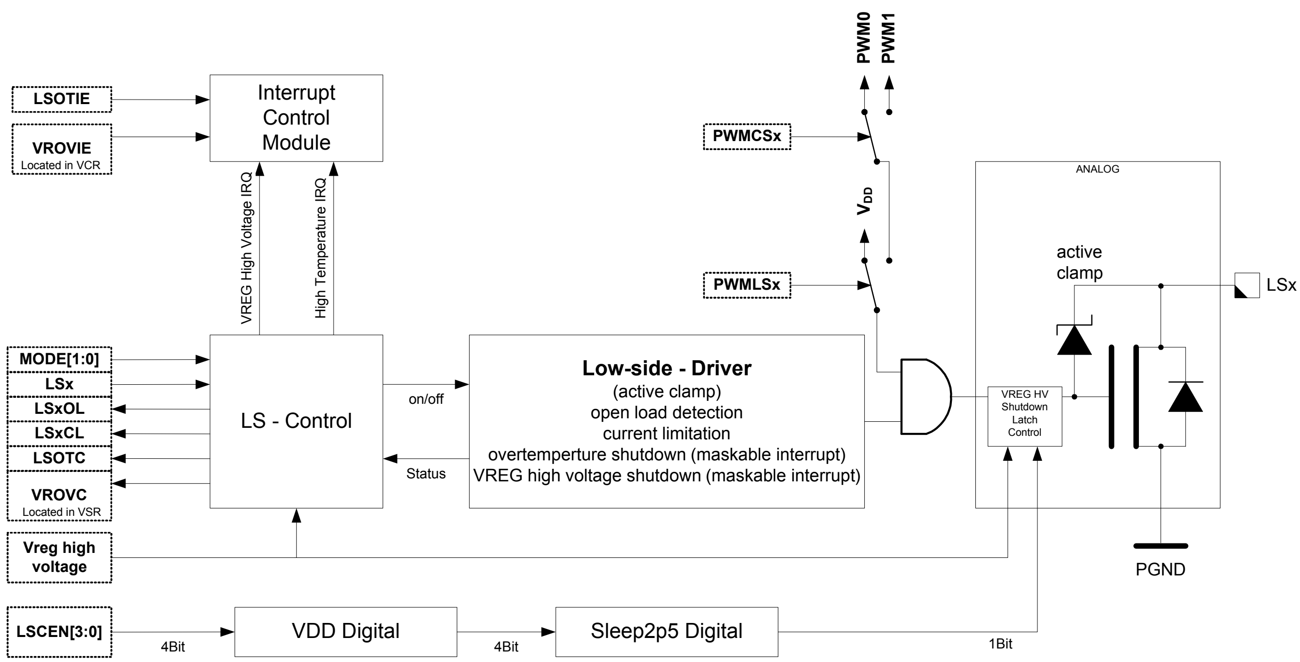

Figure 1. Low-side Block Diagram

AD Converter Not Functional with ADC Clock Equal to D2D Clock

General Description

Due to the current ADC state machine implementation, the ADC will not operate correctly with the ADCCLK = D2DCLK (Prescaler = 1).

Failure Mechanism

Due to a digital implementation issue, the ADC requires the D2DCLK frequency to be higher than the ADCCLK frequency to perform to specification. As the ADCCLK frequency is required to be in the range specified as f_{ADC} (typ. 2.0 MHz), it only applies to D2DCLK frequencies in the same range.

Workaround / Solution

The setting of the ADC Clock Prescaler = 1 (PS[2:0]=101, 110 or 111) must not be used when performing ADC measurements.

Multiple Resets On Power-Down With Large V_{SUP} Capacitor Values

General Description

With a large value of V_{SUP} (>100 μF) during power down, the RST/RESET_A line may toggle multiple times, causing the microcontroller to execute power-on resets.

Failure Mechanism

The MM912F634 has several regulators used for internal functions that are not mentioned in the data sheet. One of the 2.5 V regulators, “sleep2p5”, is used to power the sleep mode features of the device during sleep mode when the normal mode V_{DD} regulator is shut down. This regulator has an associated low voltage reset signal (LVR) that is activated at 1.8 V (power down) and released at 2.2 V (power up).
The sequence of events at power down is as follows:

1. V_{SUP} begins to decay. When V_{SUP} goes below (2.5 V + sleep2p5 headroom), the sleep2p5 output voltage begins to decay.
2. When sleep2p5 voltage reaches 1.8 V, its LVR goes low.
3. When the LVR goes low, a number of internal modules normally powered by 2sleep5 are disabled, reducing the load on the sleep2p5 regulator.
4. This reduced load reduces the value of sleep2p5 headroom, causing its output voltage to increase.
5. If the sleep2p5 output voltage increases above 2.2 V, the LVR is released, causing the internal modules to reactivate and the microcontroller to execute a power on reset (POR).
6. With a sufficiently large V_{SUP} capacitor, the slow decay of V_{SUP} can cause multiple PORs as described above.

Workaround/Solution

If possible in the application, the value of the VSUP capacitor should be decreased to increase the decay rate of V_{SUP} during power down. A value of 47 μF or less is recommended. If this is not possible, a software delay of at least 1.0 ms should be included before any code is executed following a power-on reset.

Stop Mode Wake-up generating Reset and rising WUR bit into RSR register

General Description

After a transition from Stop mode to Normal mode due to a wake up event, the device may generate a Reset.
If this occur, WUR bit into RSR register is set until a reading of RSR register occurs.
This behavior will affect parts with VDD in stop mode below LVR in normal mode.

Products

Only valid on “B” or “C” silicon:
MM912F634BV1AE
MM912F634CV1AE
MM912F634CV2AE
MM912F634CV2AP

Corrected on: “D” silicon:

MM912F634DV1AE
MM912F634DV1AP
MM912F634DV2AE
MM912F634DV2AP

Root Cause

When a wake-up event occurs, the transition from stop mode to normal mode is started. The VDD stop regulator is switched to VDD normal regulator. The LVR normal mode is activated. In case the actual VDD regulator output voltage is below LVR normal, the device will generate a reset on RESETA pin.
When an LVR condition on VDD occurs during a transition from Low Power to Normal, a RESET is performed and WUR bit is set into RSR register. This is the standard behavior during wake-up from sleep mode.

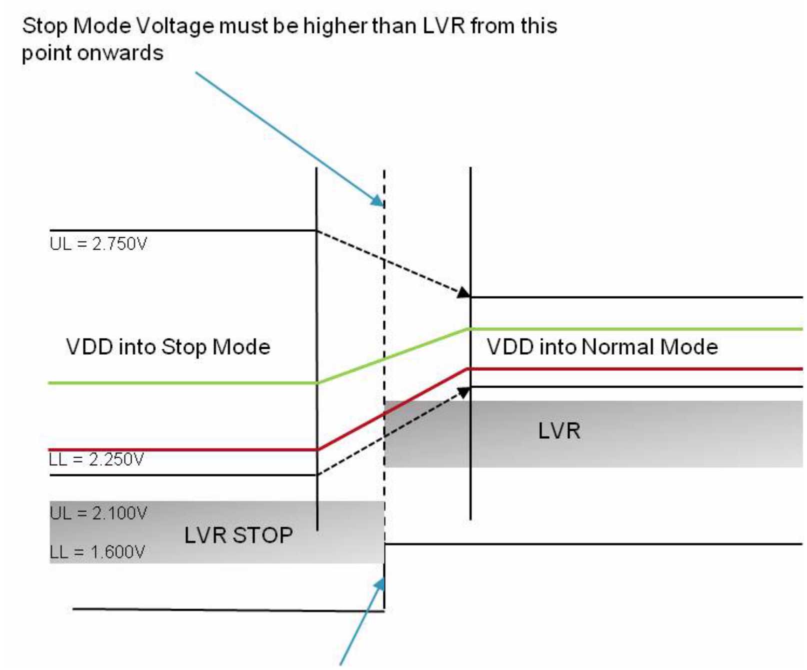

Figure 2. Stop mode to Normal mode Transition

NOTE: The green line denotes a part that does not show this behavior. The red lines denotes a part that does show this behavior.
The VDD parameter in Stop mode is distributed between 2.25 V and 2.75 V, while the LVR Normal is max 2.40 V. Only devices that have an actual VDD stop between 2.25 V and 2.40 V will exhibit this behavior.

Containment Solution

There is no workaround possible to prevent the occurrence of this behavior.
The software recommendation to help minimize impact of the behavior consists in verification of the reset source after a wake-up.
This check might be performed after return from reset sequence. In case a reset has occurred, the following flag will be as described below:

1. WUR bit is set to 1 into RSR register, indicating a Wake-up reset.
2. PORF bit is set to 0 into CRGFLG register indicating:

a.) EVDD, MCU supply, did not cross the Power-On-Reset threshold (PORF will be set to 1 in the case at wake-up from Sleep mode).
b.) EVDD and VDD stayed and are still inside their operating conditions.
The wake-up source can be identified from the Wake-up Source Register (WSR). The RAM content will not be altered by this behavior as EVDD remains in operating conditions during this transition. The program will start from its beginning following the reset sequence.
NOTE: The RAM cannot be accessed between MCU wake-up and reset generation. The delay for the MCU to start executing its code is longer than the delay for the analog to generate the reset.
NOTE: It is recommended to use VDD output to supply exclusively EVDD input and avoid any additional current load.

Unexpected setting of VROVC Bit and disabling of Low-side Driver(s) at V_{SUP} Power On

Severity Level – Medium

Description of the Problem:

During certain dynamic voltage start-up conditions (V_{BATT} cranking condition, slow V_{BATT} ramp up, etc.), and depending on the V_{SUP} capacitor used, multiple assertions of the VDD and VDDX regulators could cause multiple resets. This causes the desired Sleep Band Gap trim value CTR2 (set by the user) to be replaced with the default value (-12%). This causes the trimmed Sleep Band Gap (SLPBGP) voltage to be set too low. Consequently, a voltage regulator overvoltage condition (VROVC) fault is triggered and the bit set to 1 in the Voltage Status register (VSR). Subsequently, the Low-side drivers are disabled (see Voltage Regulator Overvoltage Protection in the Low-side Drivers section of the data sheet).
Due to a clock synchronization management issue in a case of a multiple reset, the proper CTR2 trim loaded by a user can be replaced by the intentionally low default CTR2 trim value. This default trim value can become locked during this event, meaning it can only be cleared by a full device power-down.
As the default value is loaded and locked in the analog trim circuitry, no other trim of the parameter is possible without a power-down. If after the last reset event, software is loading the trim word again, this reflects on the CTR2 register, but not on the analog trim circuitry.

4.25.1.2.3 Trimming Register 2 (CTR2)

Table 208. Trimming Register 2 (CTR2)

Offset[149] 0xF2 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	SLPBGTRE	SLPBG_LOCK	SLPBGTR2	SLPBGTR1	SLPBGTR0
W								
Reset	0	0	0	0	0	0	0	0

Note:
149. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Figure 3. Trimming Register 2 Description

Customer Impact or Symptoms:

Following an unexpected POR or voltage transient on V_{SUP}, the VROVC bit is set to 1 and the low-side drivers are disabled. The VROVC bit can subsequently be cleared **only** with a full power-down of the device.

Workaround: Disable use of the SLPBGTRE_Lock Bit

By factory default, the SLPBGTR lock bit is set to 1 in the MCU IFR. The customer can disable use of the lock bit by masking this bit when loading the contents from the IFR into the analog die CTR2 register. Since this trim data is no longer locked, it does mean the contents of CTR2 digital register must be re-loaded by the user after each RESET event.
Of all the TRIM registers used in the device, only the CTR2 trim register has this locking feature. Therefore, disabling the use of this lock feature does not represent an unusual condition in which to operate the device.

5 Revision History

Revision	Date	Description of Changes
7.0	5/2015	• Added Revision History • Unexpected setting of VROVC Bit and disabling of Low-side Driver(s) at V_{SUP} Power On • Re-formatted document to conform to new Errata template
8.0	6/2015	• Changed part number in Introduction table from MM912F634CV1AE to MM912F634CV2AE • Changed part number in Introduction table from MM912F634DV1AE to MM912F634DV2AE

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