

## General Description

The MAX20307 is a configurable driver IC for enhancement mode Gallium Nitride (eGaN) FETs, optimized for high-frequency operation. The device is designed to drive both the high-side and low-side FETs in a half-bridge topology. The floating high-side driver is capable of driving a high-side eGaN FET operating up to 60V. A synchronous bootstrap technique provides the high-side bias voltage and is internally clamped at 5.2V. This clamping prevents the gate voltage from exceeding the maximum rated gate-source voltage of eGaN FETs.

The gate driver input signal is 3.3V TTL logic compatible, and can withstand input voltages up to 6V regardless of the  $V_{CC}$  voltage. Additionally, the MAX20307 features adaptive dead time control.

High-frequency H-bridge drive capability and adaptive dead time control make the MAX20307 ideal for high-efficiency buck applications. TTL logic compatibility allows the INH drive input to operate directly from the outputs of most PWM controllers allowing for flexible design.

The device covers wireless power (transmitting) levels from a few Watts to over 20 Watts making it well suited for wireless charging of various portable devices. High frequency optimization enables the use of wireless charging standards such as A4WP (6.78MHz) and ISM band (13.56MHz) wireless charging.

The MAX20307 is available in a space-saving, 15-bump, 1.2 x 2.0mm wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

## Applications

- Switching Power Supply Topology Support
  - Half and Full-Bridge converters
  - Current Fed Push-Pull converters
  - Synchronous Buck converters
- A4WP Wireless Charging
- Medical Device Wireless Charging in ISM Band
- WPC and PMAT

## Benefits and Features

- Flexible/Configurable Gate Drive
  - Single Control Input
  - 1A/5A Gate Source/Sink Current
- High-Efficiency SMPS Design
  - Low Loss Gate Drive: Optimized Bootstrap Circuit
  - Automatic Dead Time Control Optimized for Half-Bridge Converters
  - Programmable Maximum Dead Time
    - 0ns–9ns GPIO Controlled
  - Fast Propagation Delay (22ns)
- Safe Gate Drive
  - High-Side Floating Node Voltage up to 60V
  - Gate Supply Voltage UVLO
- Space-Saving Design
  - 0.4mm pitch 1.2mm x 2.0mm WLP

[Ordering Information](#) appears at end of data sheet.

### Absolute Maximum Ratings

(Voltages reference to GND unless otherwise noted)

V <sub>CC</sub> .....	-0.3V to +6V
V <sub>IN</sub> .....	-0.3V to +66V
LO.....	-0.3V to V <sub>CC</sub> + 0.3V
HO.....	V <sub>HS</sub> - 0.3V to V <sub>HB</sub> + 0.3V
HB.....	-0.3V to +66V
HB to V <sub>CC</sub> .....	-0.3V to +60V
HS.....	-0.3V to +60V

INL, INH, LDTY0, LDTY1, DTP0, DTP1 .....	-0.3V to +6V
Continuous Power Dissipation (T <sub>A</sub> = +70°C):	
WLP (derate 16.4mW/°C above +70°C.).....	1312mW
Operating Temperature Range.....	-40°C to +85°C
Junction Temperature.....	-40°C to +150°C
Storage Temperature Range.....	-40°C to +150°C
Soldering Temperature (reflow).....	+260°C

### Package Thermal Characteristics (Note 1)

WLP

Junction-to-Ambient Thermal Resistance (θ<sub>JA</sub>) .....52°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Electrical Characteristics

(V<sub>CC</sub> = 4.5 to 5.5V, T<sub>A</sub> = -40°C to +85°C unless otherwise noted. Typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>V<sub>CC</sub></b>						
Supply Voltage Range	V <sub>CC</sub>		4.5		5.5	V
V <sub>CC</sub> Quiescent Current	I <sub>Q</sub>	INH = 0V		6	13	mA
V <sub>CC</sub> Operating Current	I <sub>CC</sub>	f = 13.56MHz, C <sub>L</sub> = 47pF		35		mA
V <sub>CC</sub> Undervoltage Lockout (UVLO)	V <sub>CC_UVLO</sub>	V <sub>CC</sub> Rising	3.1	3.6	3.8	V
V <sub>CC</sub> UVLO Hysteresis	V <sub>CC_UVLOHYS</sub>	V <sub>CC</sub> Falling		0.1		V
<b>eGaN GATE DRIVER</b>						
LO Output Low	LO <sub>OUT_LOW</sub>	I <sub>LO</sub> = 100mA		<0.1		V
LO Output High	LO <sub>OUT_HIGH</sub>	I <sub>LO</sub> = 100mA		V <sub>CC</sub> - 0.5V		V
HO Output Low	HO <sub>OUT_LOW</sub>	I <sub>HO</sub> = 100mA		<0.1		V
HO Output High	HO <sub>OUT_HIGH</sub>	I <sub>HO</sub> = 100mA, V <sub>BS</sub> = V <sub>HB</sub> - V <sub>HS</sub>		V <sub>BS</sub> - 0.5V		V
Peak Source Current ON				1		A
Peak Sink Current OFF				5		A

## DC Electrical Characteristics (continued)

(V<sub>CC</sub> = 4.5 to 5.5V, T<sub>A</sub> = -40°C to +85°C unless otherwise noted. Typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL CONTROL INPUT SIGNALS (INL, INH)</b>						
Input High Threshold	V <sub>IH</sub>	Rising Edge		52		%V <sub>CC</sub>
Input Hysteresis				3		%V <sub>CC</sub>
Input Pull Down	PD <sub>INH</sub>		80	200	370	kΩ
<b>DIGITAL IO SIGNALS (DTP0, DTP1, LDTY0, LDTY1)</b>						
Input High Threshold	V <sub>IH</sub>		1.6			V
Input Low Threshold	V <sub>IL</sub>				0.4	V
Input Leakage Current	I <sub>LEAK</sub>		-1		1	μA
Output High Leakage Current	I <sub>LEAKOUT</sub>	V <sub>IO</sub> = 5.5V	-1		1	μA
Output Low	V <sub>OL</sub>	I <sub>LDTY_</sub> = 10mA			0.4	V
<b>TIMING CHARACTERISTICS (FIGURE 1)</b>						
L Turn-On Propagation Delay	t <sub>PLOn</sub>	INH rising to LO rising (Note 3), DTP0 = DTP1 = 0		22		ns
L Turn-Off Propagation Delay	t <sub>PLOff</sub>	INH falling to LO falling, DTP0 = DTP1 = 0		22		ns
H Turn-On Propagation Delay	t <sub>PHOn</sub>	INH rising to HO rising (Note 3), DTP0 = DTP1 = 0		22		ns
H Turn-Off Propagation Delay	t <sub>PHOff</sub>	INH falling to HO falling, DTP0 = DTP1 = 0		22		ns
LO HO Delay Matching	t <sub>DMHOn</sub>	L off to H on		2		ns
HO LO Delay Matching	t <sub>DMLOn</sub>	H off and L on		2		ns
Minimum Input Signal Length		INH input deglitching duty cycle mismatch 4%		2		ns
LO Rise Time		C <sub>L</sub> = 1000pF		5		ns
LO Fall Time		C <sub>L</sub> = 1000pF		1		ns
HO Rise Time		C <sub>L</sub> = 1000pF		5		ns
HO Fall Time		C <sub>L</sub> = 1000pF		1		ns
Minimum Output Dead Time		(Note 4)		0		ns
Maximum Output Dead Time		(Note 4)		9		ns
<b>THERMAL PROTECTION</b>						
Thermal Shutdown	T <sub>SHDN</sub>			150		°C
Thermal Hysteresis	T <sub>HYST</sub>			20		°C

**Note 2:** All devices are 100% production tested at T<sub>A</sub> = +25°C. Limits over the operating temperature range are guaranteed by design.

**Note 3:** The specified propagation delay of a rising edge includes dead time.

**Note 4:** See Table 1 for details on configuring the dead time on MAX20307. The minimum and maximum dead time will vary with supply voltage.

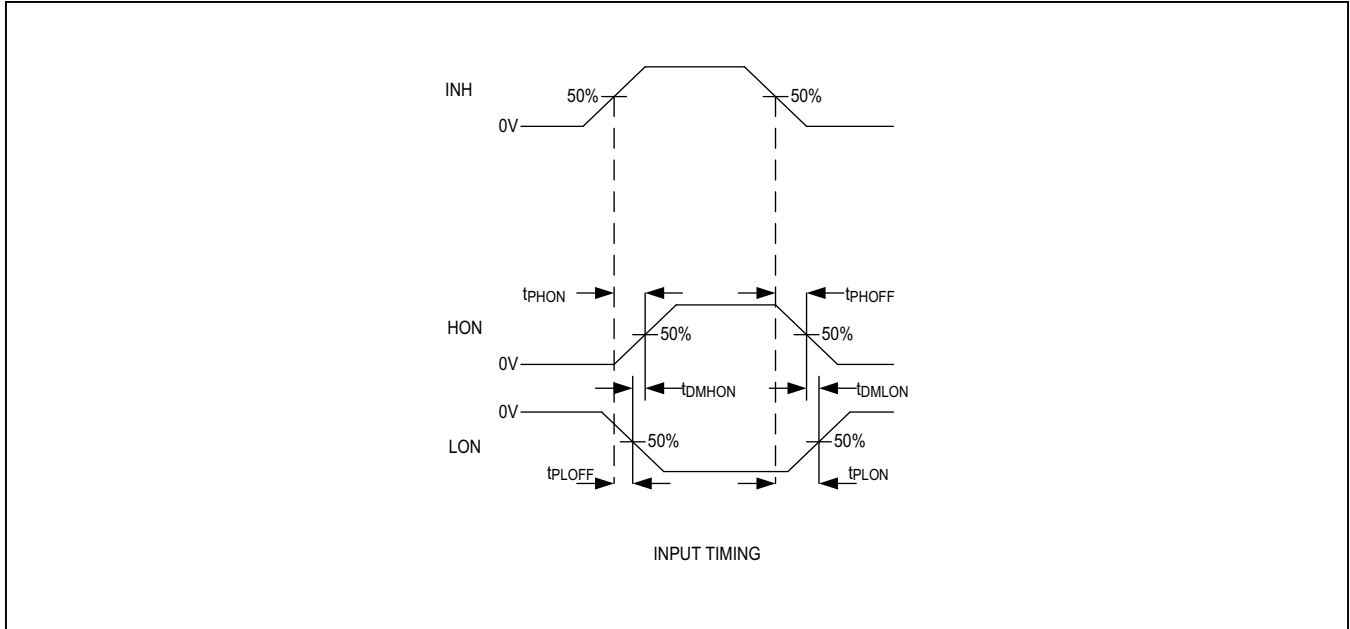
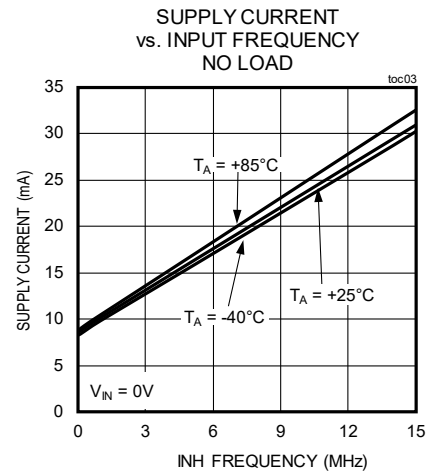
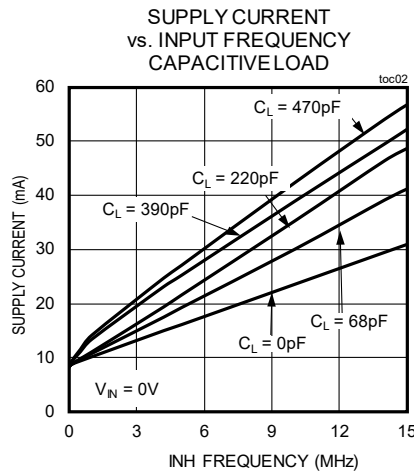
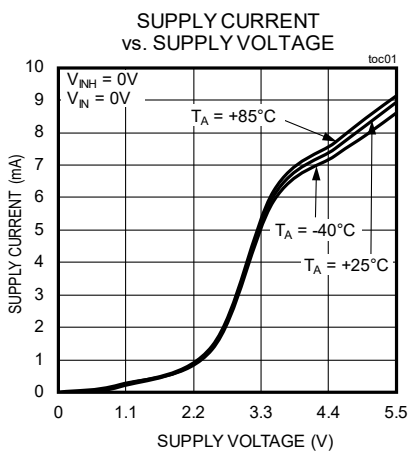


Figure 1. Timing Diagram

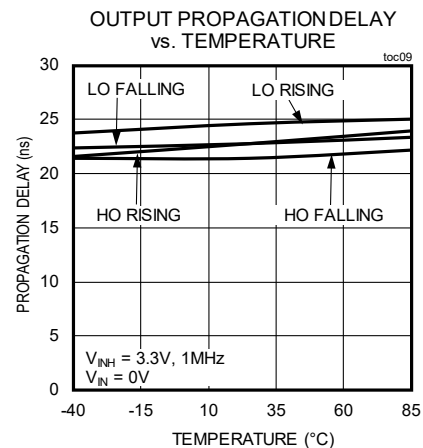
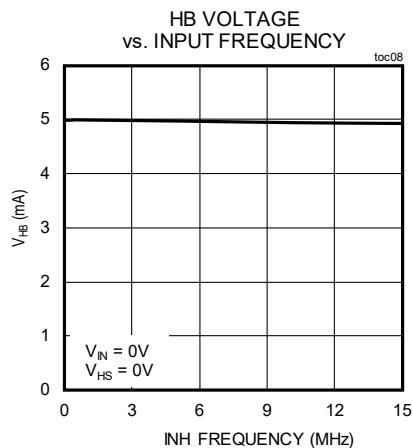
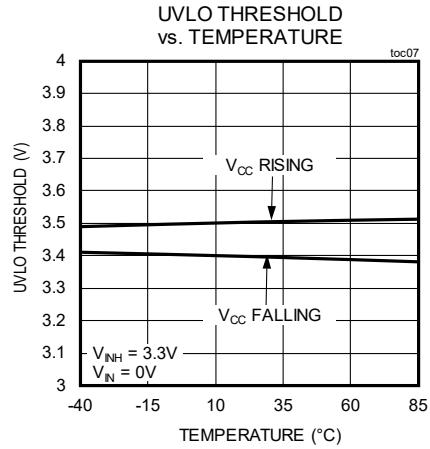
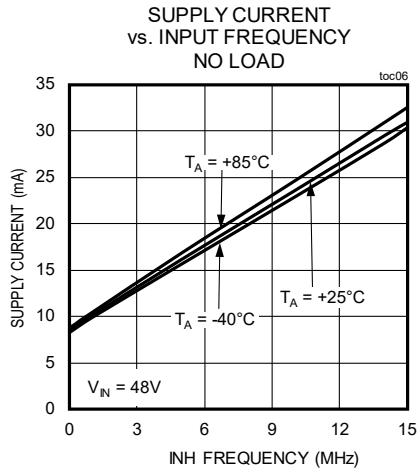
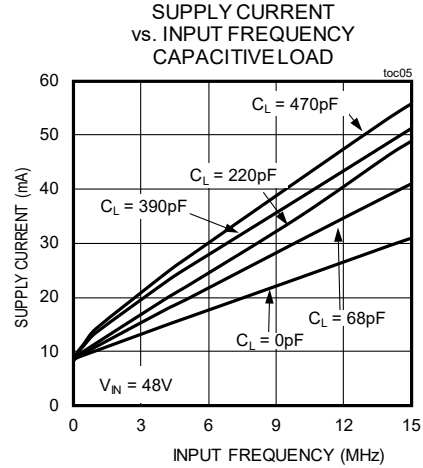
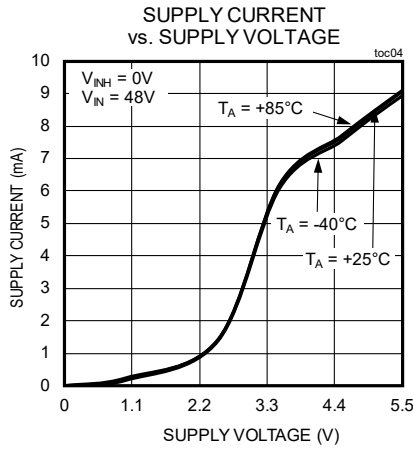
**Typical Operating Characteristics**

(V<sub>CC</sub> = 5V, V<sub>IN</sub> = 48V, T<sub>A</sub> = +25°C unless otherwise noted.)



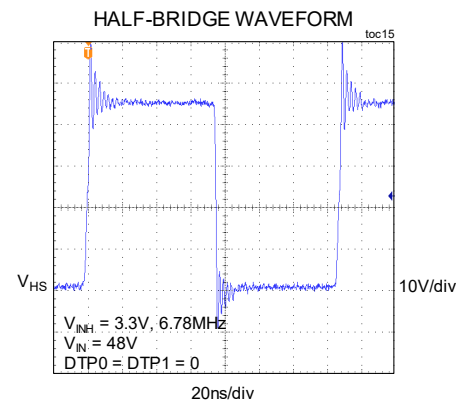
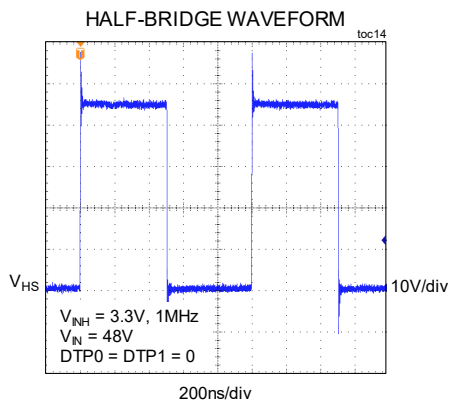
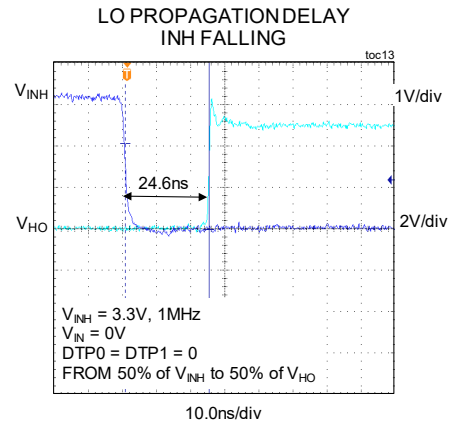
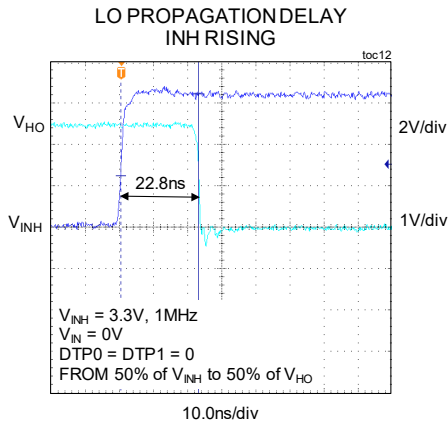
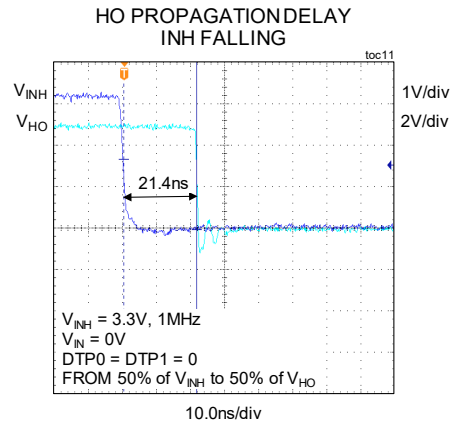
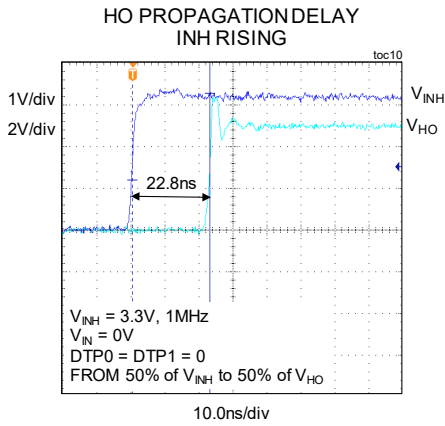
Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{IN} = 48V$ ,  $T_A = +25^\circ C$  unless otherwise noted.)

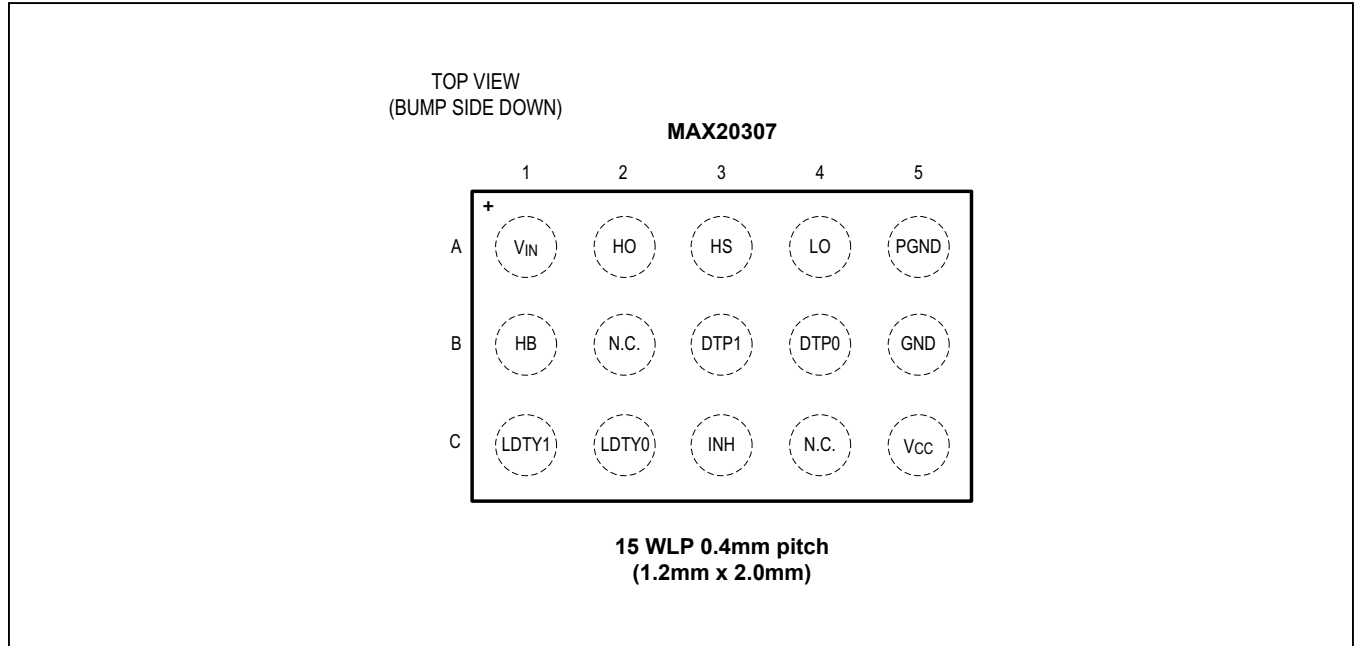


Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{IN} = 48V$ ,  $T_A = +25^\circ C$  unless otherwise noted.)



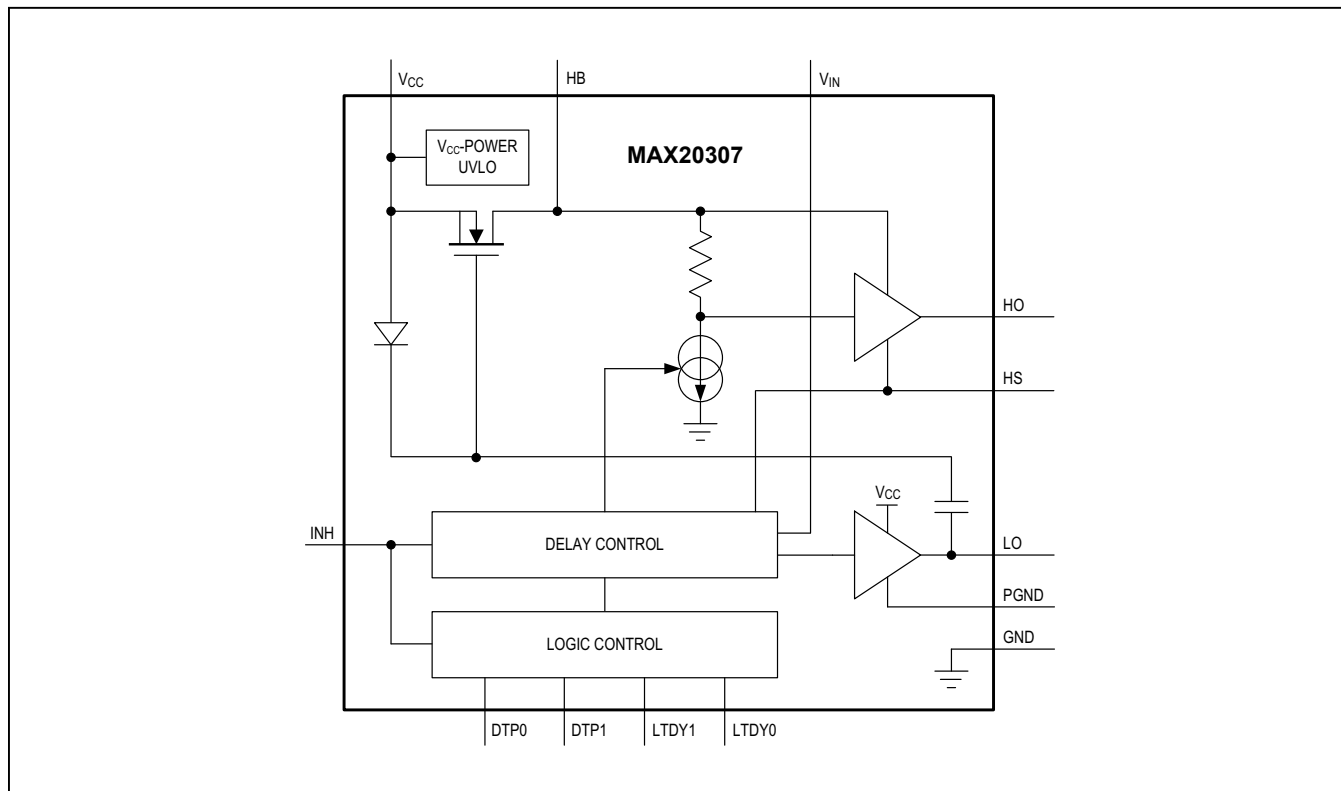
Pin Configurations



Bump Descriptions

BUMP	NAME	FUNCTION
A1	V <sub>IN</sub>	High-Side Rail. Connect to drain of the high-side eGaN FET.
A2	HO	High-Side eGaN FET Gate Driver Output
A3	HS	High-Side eGaN FET Source Connection
A4	LO	Low-Side eGaN FET Gate Driver Output
A5	PGND	Low-Side eGaN FET Source Connection. Power ground. Connect to GND.
B1	HB	High-Side eGaN FET Gate Driver Bootstrap
B2, C4	N.C.	No Connect. Leave pin floating.
B3	DTP1	Maximum Dead Time Programming Bit 1 Input.
B4	DTP0	Maximum Dead Time Programming Bit 0 Input.
B4	GND	Ground
C1	LDTY1	Load Type Indicator for Capacitive Load. Open drain output.
C2	LDTY0	Load Type Indicator for Inductive Load. Open drain output.
C3	INH	Drive Input
C5	V <sub>CC</sub>	Power

Block Diagram





## Detailed Description

The MAX20307 is designed to drive the high-side and low-side eGaN FETs of a half-bridge configuration or two low-side eGaN FETs with a single-drive input. The device features adaptive dead time control to maximize switching efficiency, making the MAX20307 well suited for high-frequency switching converters.

The device features TTL logic compatible inputs and can withstand input voltages of up to +6V regardless of the  $V_{CC}$  voltage. This wide operating range enables most PWM controllers to directly drive the input of the MAX20307.

The asymmetrical sink/source gate drive outputs of the device are optimized for high-frequency applications. A low impedance path in the gate driver prevents accidental turn-on by the high dv/dt characteristic of HS switching transitions.

## Power Consumption

The total power consumption of the device is critical as it ultimately determines the maximum operating frequency of the gate driver. Power losses in the MAX20307 are defined by the  $V_{CC}$  supply current.  $V_{CC}$  supplies the low-side gate drive circuit directly, but also powers the high-side circuit through the synch-FET circuit. Gate driver losses are proportional to the gate charge of the eGaN FET as it charges and discharges. The synch-FET reduces losses through the bootstrap clamping diode caused by the diode's reverse recovery charge ( $Q_{RR}$ ).

## Dead Time Control

An adaptive dead time control feature maximizes efficiency when the MAX20307 drives a half-bridge. The MAX20307 automatically increases or decreases the dead time between 0ns and the maximum dead time set by DTP0 and DTP1. This allows the device to minimize the losses caused by body diode conduction and reverse recovery while also avoiding shoot-through. [Table 1](#) details the maximum dead time setting for a DTP\_ configuration. Setting DTP0 and DTP1 to 0 gives the device full control of the dead time without delay.

**Table 1. Maximum Dead Time Programming**

DTP1	DTP0	DEAD TIME (ns)
0	0	0
0	1	3
1	0	6
1	1	9

## Load Type Indicator

The MAX20307 features the ability to distinguish between inductive and capacitive loads. Two open-drain outputs, LDTY0 and LDTY1, indicate if the load connected to HS is capacitive or inductive. By connecting pullup resistors from LDTY0 and LDTY1 to the  $V_{CC}$  supply, the pins can signal the type of load attached. LDTY0 will output high if the load is inductive and LDTY1 will output high if the load is capacitive.

## Applications Information

### $V_{CC}$ Bypass Capacitor

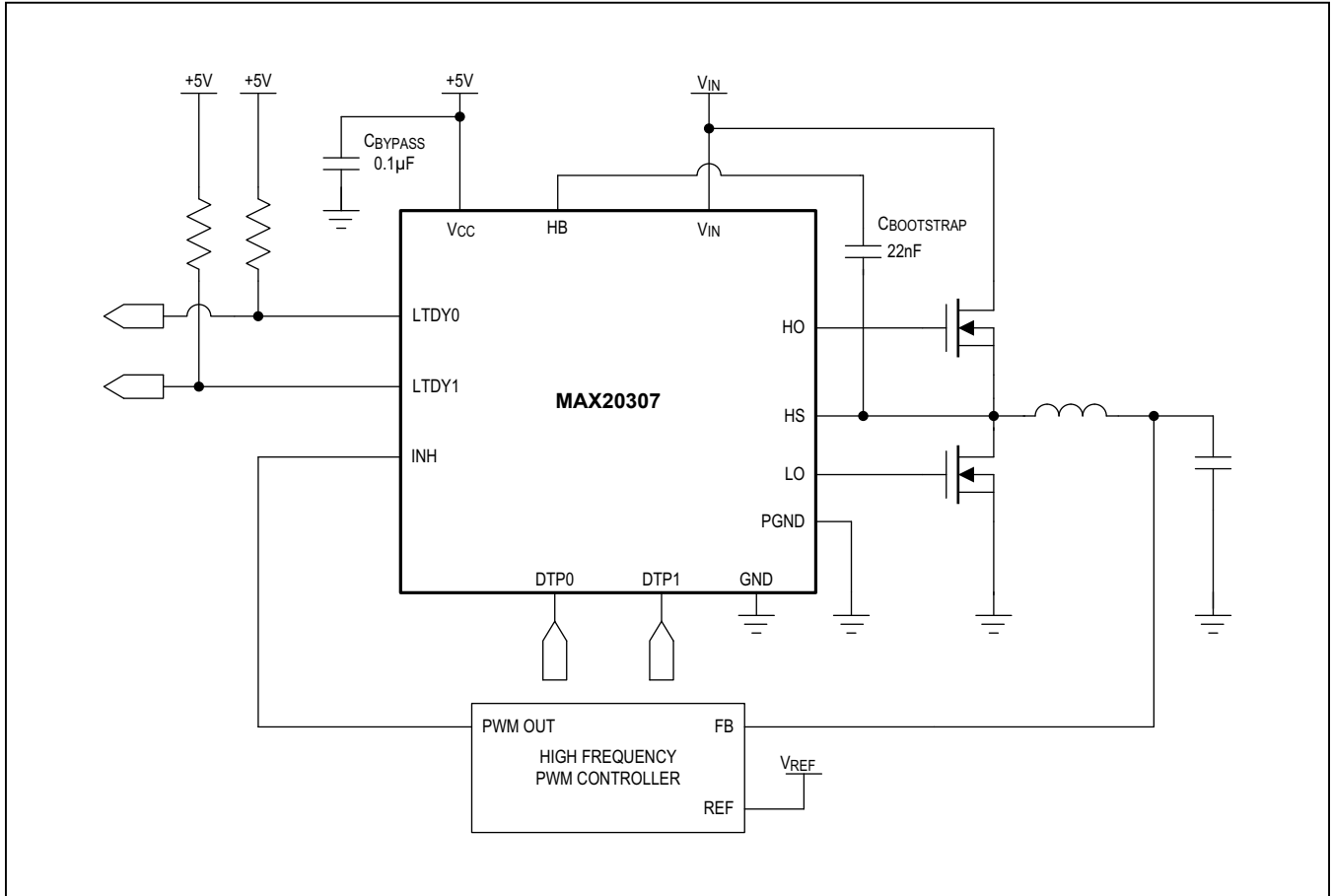
An external  $V_{CC}$  bypass capacitor provides the gate charge for the low- and high-side transistors and absorbs the reverse recovery charge of the bootstrap diode. A 0.1 $\mu$ F or larger ceramic capacitor with low ESR and low temperature coefficient is recommended. The bypass capacitor should be placed close to the  $V_{CC}$  pin of the devices to minimize parasitic inductance.

### Bootstrap Capacitor

When driving a half-bridge configuration, the MAX20307 needs an external bootstrap capacitor to drive the high-side eGaN FET. The bootstrap capacitor is charged by the synch-FET whenever the HS is pulled to ground. Since the source to drain voltage drop of an eGaN FET is much higher than that of a typical PN junction diode, the MAX20307 features an internal clamping circuit with synch-FET control to prevent the gate drive voltage from exceeding the maximum gate-source voltage of the eGaN FET and damaging the high-side eGaN FET.

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB UVLO circuit, and the clamping circuit. A 0.1 $\mu$ F for 1MHz applications or 22nF for 6.78MHz applications or larger ceramic capacitor with low ESR and low temperature coefficient are recommended. The bypass capacitor should be placed close to the HB pin of the devices to minimize parasitic inductance.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20307EWL+	-40°C to +85°C	15 WLP
MAX20307EWL+T	-40°C to +85°C	15 WLP

+Denotes a lead (Pb)-free package/RoHS-compliant package  
T = Tape and reel

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
15 WLP	W151E2+1	<a href="#">21-1031</a>	Refer to <a href="#">Application Note 1891</a>

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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