RoHS Compliant

N-CHANNEL MOSFET

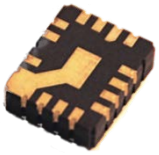
Qualified per MIL-PRF-19500/555

Qualified Levels: JAN, JANTX, and JANTXV

DESCRIPTION

These 2N6788U and 2N6790U devices are military qualified up to a JANTXV level for high-reliability applications. Microsemi also offers numerous other products to meet higher and lower power voltage regulation applications.

Important: For the latest information, visit our website http://www.microsemi.com.



U-18 LCC Package

FEATURES

- Surface mount equivalent of JEDEC registered 2N6788 and 2N6790 numbers.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/555.
- RoHS compliant by design.

APPLICATIONS / BENEFITS

- High frequency operation.
- Lightweight, low-profile package.
- ESD rated to class 1A.

Also available in:

TO-205AF Package
(leaded)
2N6788 & 2N6790

MAXIMUM RATINGS @ T_C = +25 °C unless otherwise noted

Parameters / Test Conditions		Symbol	Value	Unit
Junction & Storage Temperature		T_J, T_{stg}	-55 to +150	°C
Thermal Resistance Junction-to-Case (see Figure 1)		$R_{\Theta JC}$	8.93	ºC/W
Total Power Dissipation (1)		P_T	0.8	W
Drain to Gate Voltage	2N6788U 2N6790U	V_{DG}	100 200	V
Drain – Source Voltage	2N6788U 2N6790U	V_{DS}	100 200	V
Gate – Source Voltage		V_{GS}	± 20	V
Drain Current, dc @ T_C = +25 °C (2) (see Figure ?)	2N6788U 2N6790U	I_{D1}	4.5 2.8	A
Drain Current, dc @ T_C = +100 °C	2N6788U 2N6790U	I_{D2}	2.8 1.8	A
Off-State Current (3)	2N6788U 2N6790U	I_{DM}	18 11	A (pk)
Source Current	2N6788U 2N6790U	I_S	4.5 2.8	A

Notes:
1. Derated linearly by 0.11 W/°C for T_C > +25 °C.
2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(max)}}$$

3. I_{DM} = 4 x I_{D1}; I_{D1} as calculated in note 2.

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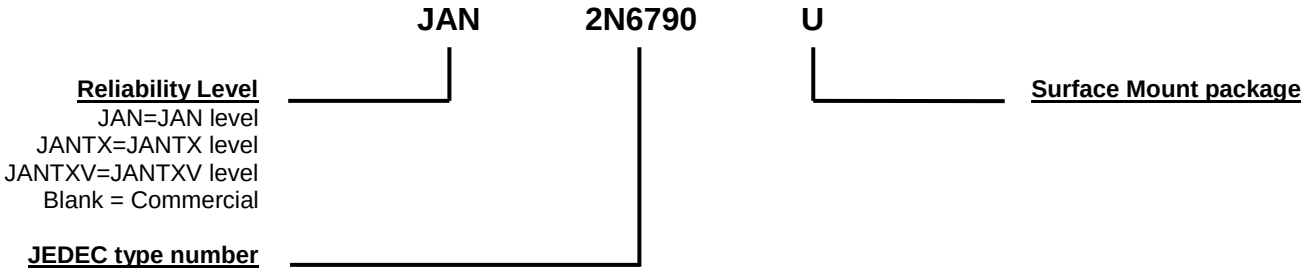
MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
I_D	Drain current.
I_F	Forward current.
T_C	Case temperature.
V_{DD}	Drain supply voltage.
V_{DS}	Drain to source voltage.
V_{GS}	Gate to source voltage.

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERTICS					
Drain-Source Breakdown Voltage V_{GS} = 0 V, I_D = 1 mA	2N6788U 2N6790U	$V_{(BR)DSS}$	100 200		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}$, I_D = 0.25 mA $V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_j = +125 °C $V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_j = -55 °C		$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±20 V, V_{DS} = 0 V, T_j = +125 °C		I_{GSS1} I_{GSS2}		±100 ±200	nA

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
ON CHARACTERISTICS					
Drain Current V_{GS} = 0V, V_{DS} = 80 V V_{GS} = 0V, V_{DS} = 160 V	 2N6788U 2N6790U	I_{DSS1}		25	µA
Drain Current V_{GS} = 0V, V_{DS} = 80 V, T_j = +125 °C V_{GS} = 0V, V_{DS} = 160 V, T_j = +125 °C	 2N6788U 2N6790U	I_{DSS2}		0.25	mA
Static Drain-Source On-State Resistance V_{GS} = 10 V, I_D = 3.5 A pulsed V_{GS} = 10 V, I_D = 2.25 A pulsed	 2N6788U 2N6790U	$r_{DS(on)1}$		0.30 0.80	Ω
Static Drain-Source On-State Resistance V_{GS} = 10 V, I_D = 6.0 A pulsed V_{GS} = 10 V, I_D = 3.5 A pulsed	 2N6788U 2N6790U	$r_{DS(on)2}$		0.35 0.85	Ω
Static Drain-Source On-State Resistance T_j = +125 °C: V_{GS} = 10 V, I_D = 3.5 A pulsed V_{GS} = 10 V, I_D = 2.25 A pulsed	 2N6788U 2N6790U	$r_{DS(on)3}$		0.54 1.50	Ω
Diode Forward Voltage V_{GS} = 0 V, I_D = 6.0 A pulsed V_{GS} = 0 V, I_D = 3.5 A pulsed	 2N6788U 2N6790U	V_{SD}		1.8 1.5	V

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Gate Charge:					
On-State Gate Charge V_{GS} = 10 V, I_D = 6.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.5 A, V_{DS} = 100 V	2N6788U 2N6790U	$Q_{g(on)}$		18.0 14.3	nC
Gate to Source Charge V_{GS} = 10 V, I_D = 6.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.5 A, V_{DS} = 100 V	2N6788U 2N6790U	Q_{gs}		4.0 3.0	nC
Gate to Drain Charge V_{GS} = 10 V, I_D = 6.0 A, V_{DS} = 50 V V_{GS} = 10 V, I_D = 3.5 A, V_{DS} = 100 V	2N6788U 2N6790U	Q_{gd}		9.0 9.0	nC

SWITCHING CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Turn-on delay time I_D = 6.0 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 35 V I_D = 3.5 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 74 V	2N6788U 2N6790U	$t_{d(on)}$		40	ns
Rinse time I_D = 6.0 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 35 V I_D = 3.5 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 74 V	2N6788U 2N6790U	t_r		70 50	ns
Turn-off delay time I_D = 6.0 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 35 V I_D = 3.5 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 74 V	2N6788U 2N6790U	$t_{d(off)}$		40 50	ns
Fall time I_D = 6.0 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 35 V I_D = 3.5 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 74 V	2N6788U 2N6790U	t_f		70 50	ns
Diode Reverse Recovery Time di/dt = 100 A/µs, V_{DD} ≤ 50 V, I_F = 6.0 A di/dt = 100 A/µs, V_{DD} ≤ 50 V, I_F = 3.5 A	2N6788U 2N6790U	t_{rr}		240 400	ns

GRAPHS

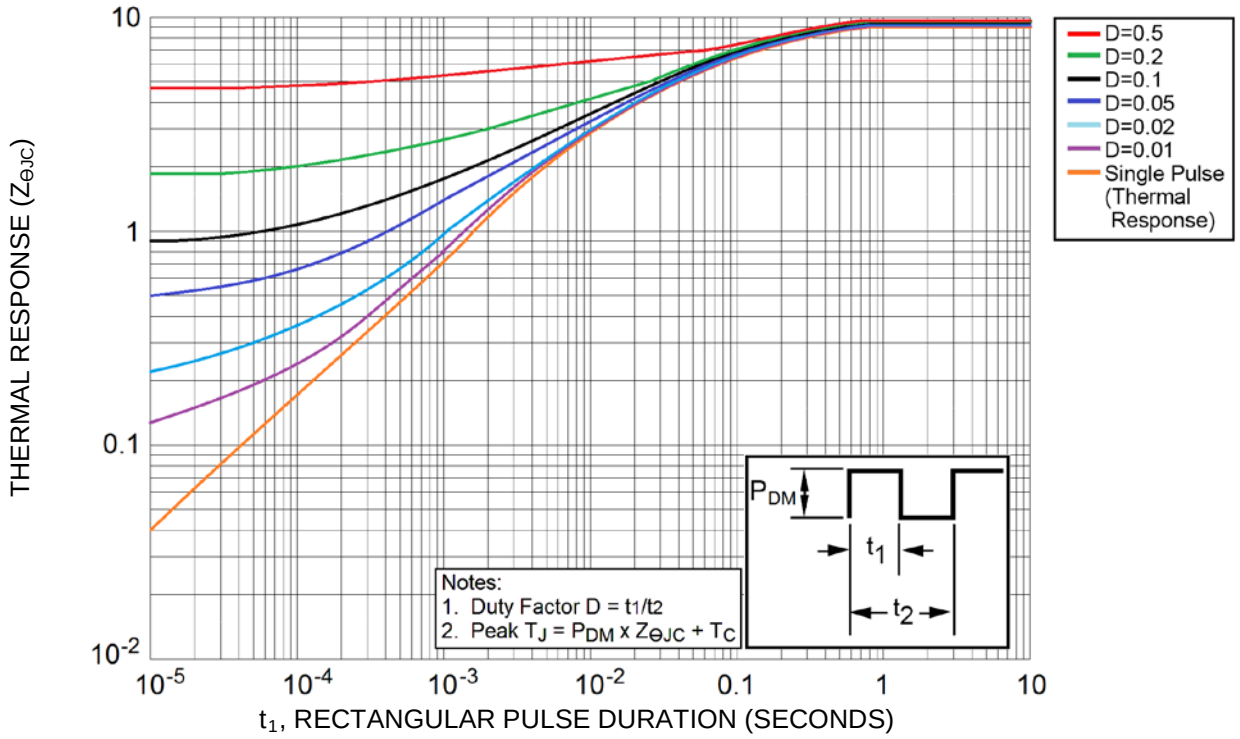


Figure 1
Thermal Impedance Curves

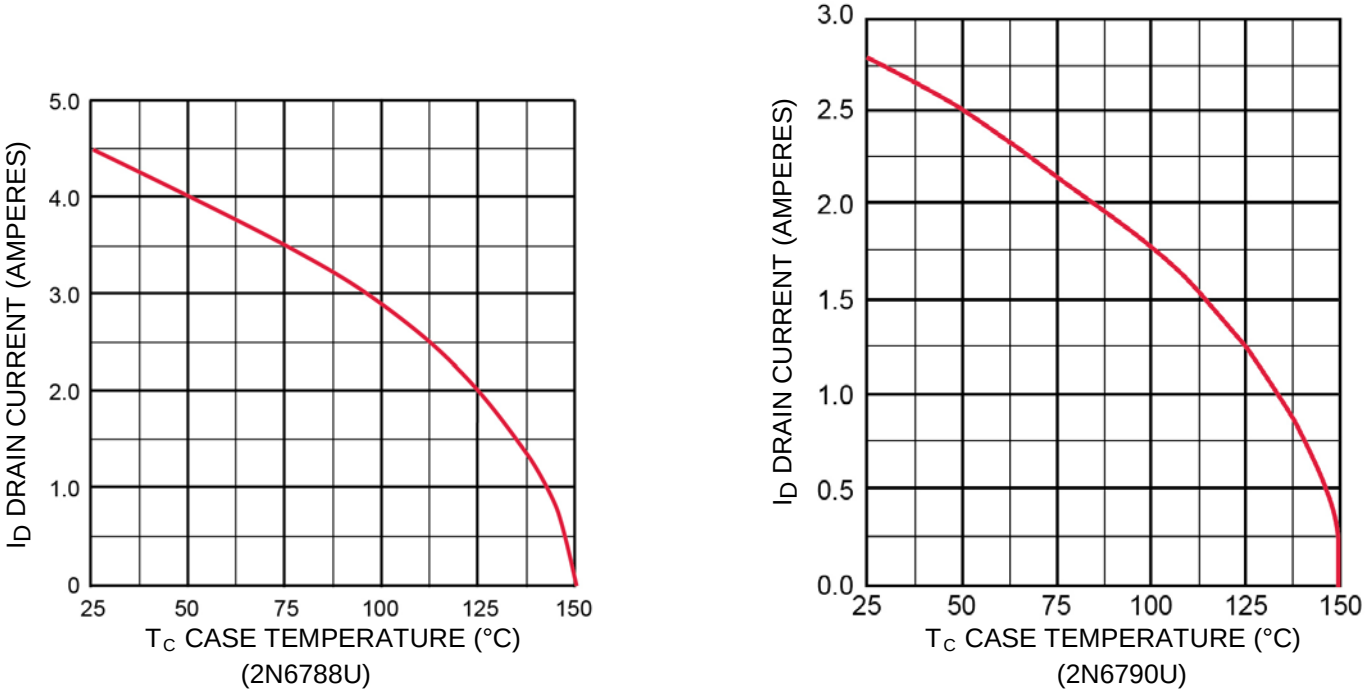
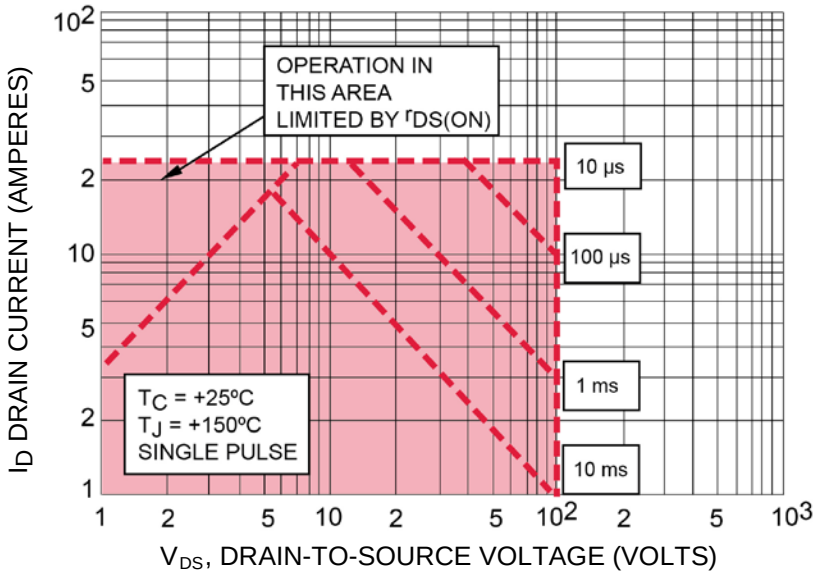
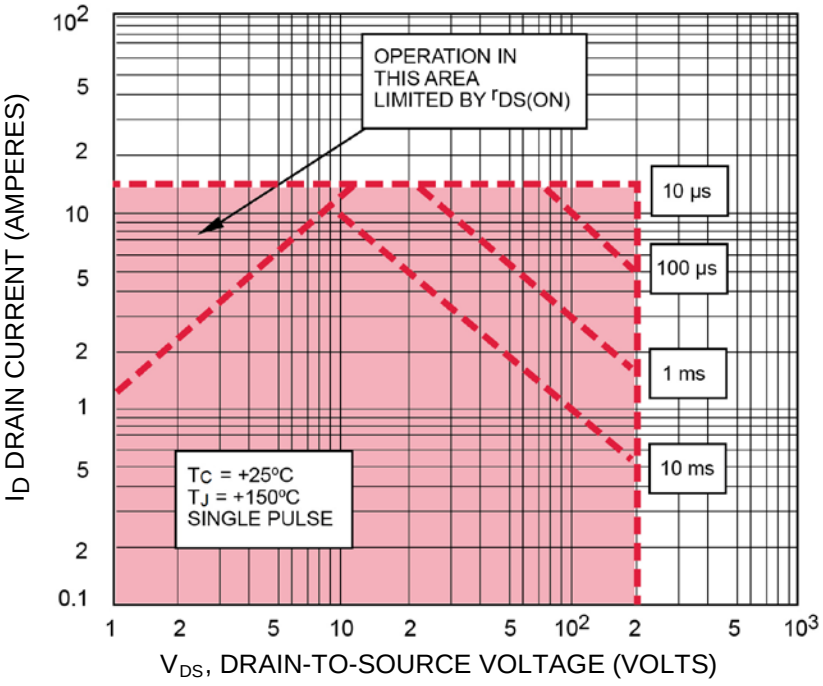


Figure 2
Maximum Drain Current vs. Case Temperature Graph

GRAPHS (continued)

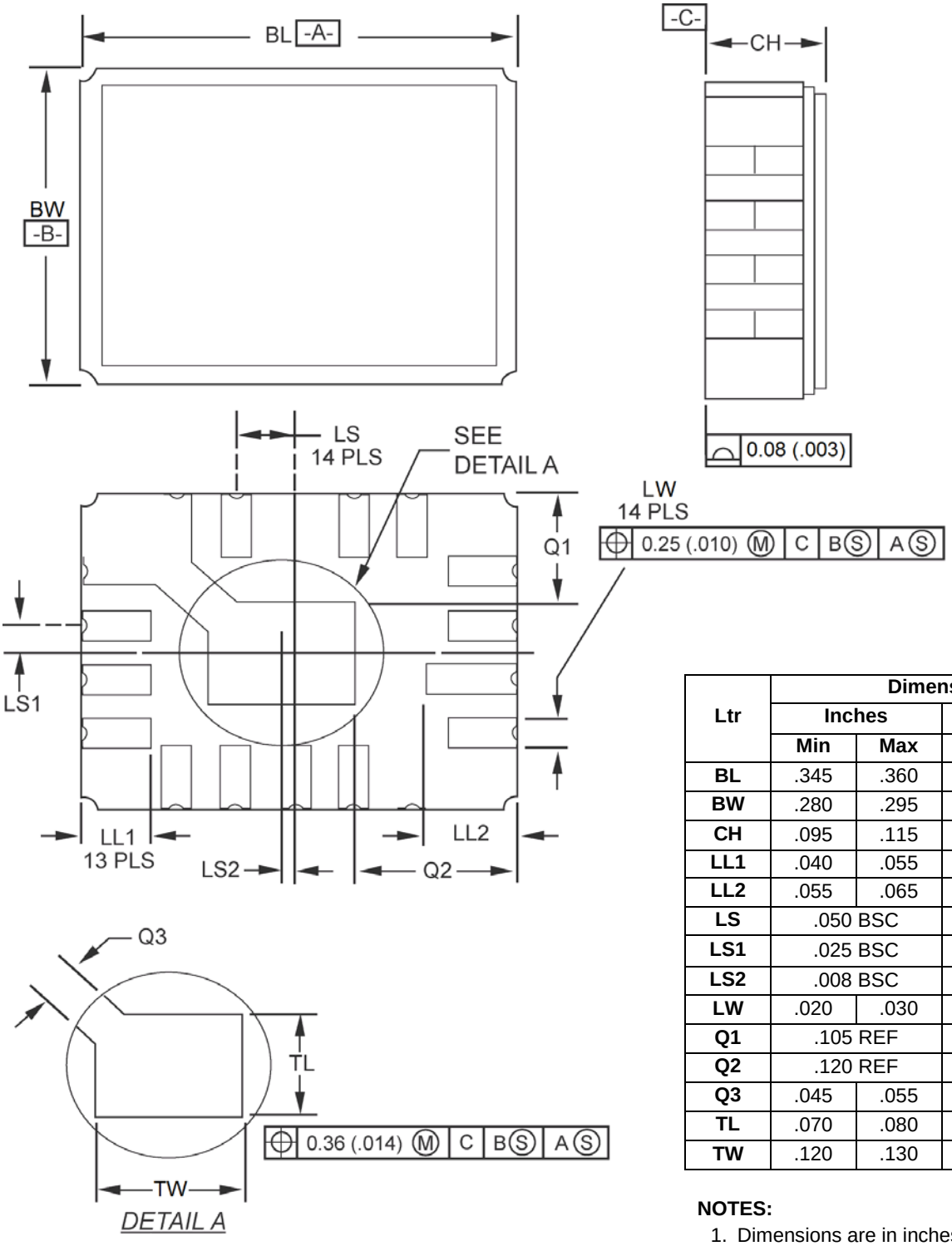


Maximum Safe Operating Area (2N6788U)



Maximum Safe Operating Area (2N6790U)

PACKAGE DIMENSIONS

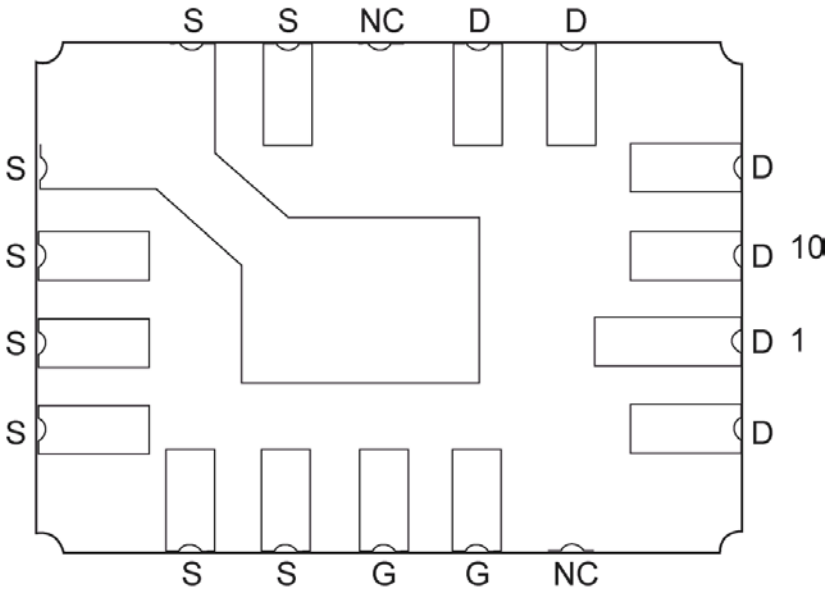


Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.12	7.49
CH	.095	.115	2.42	2.92
LL1	.040	.055	1.02	1.39
LL2	.055	.065	1.40	1.65
LS	.050 BSC		1.27 BSC	
LS1	.025 BSC		0.635 BSC	
LS2	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q1	.105 REF		2.67 REF	
Q2	.120 REF		3.05 REF	
Q3	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

PAD LAYOUT



PAD ASSIGNMENTS