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Kind regards,

Team Nexperia

74LVC139

Dual 2-to-4 line decoder/demultiplexer

Rev. 5 — 19 October 2011

Product data sheet

1. General description

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. It has two independent decoders, each accepting two binary weighted inputs ($nA0$ and $nA1$) and providing four mutually exclusive outputs ($nY0$ to $nY3$) that are LOW when selected. Each decoder has an active LOW input ($n\bar{E}$). When $n\bar{E}$ is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC139D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC139DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC139PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC139BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

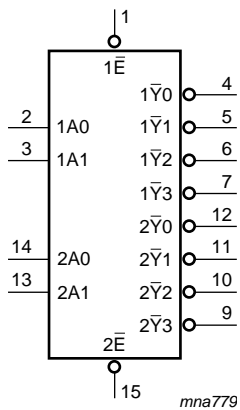


Fig 1. Logic symbol

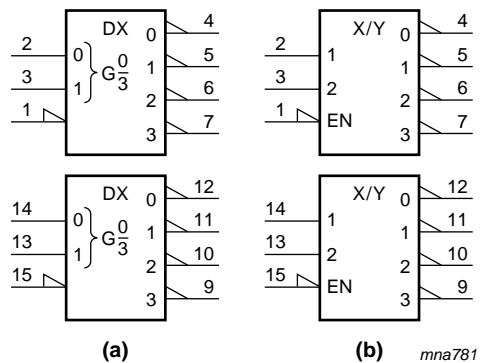


Fig 2. IEC logic symbol

- a) demultiplexer
- b) decoder

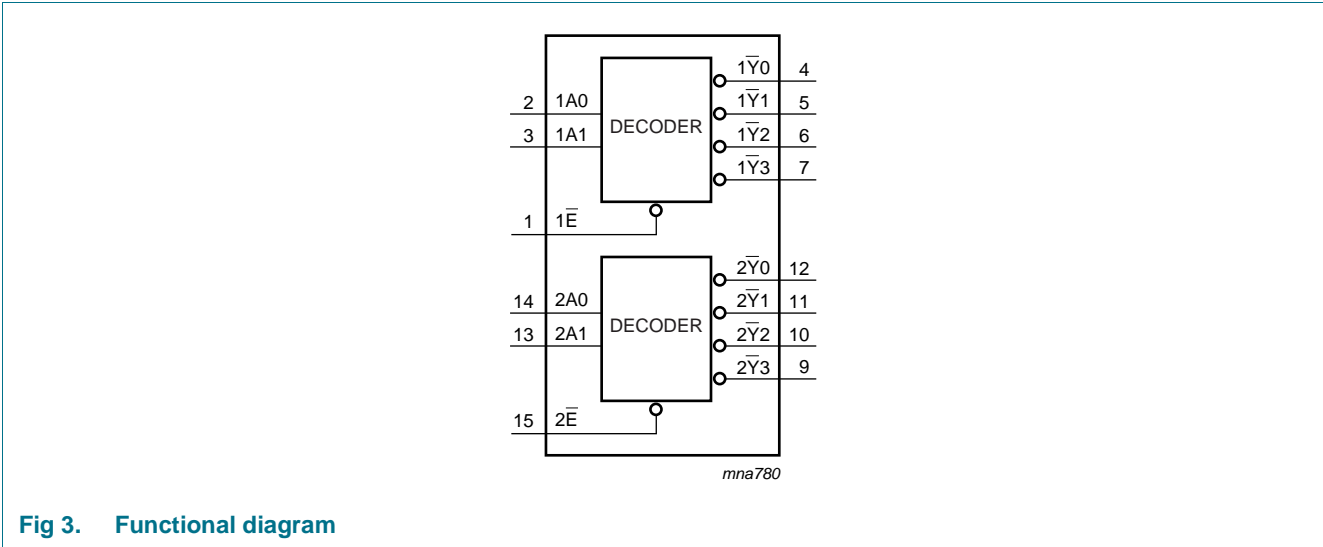


Fig 3. Functional diagram

5. Pinning information

5.1 Pinning

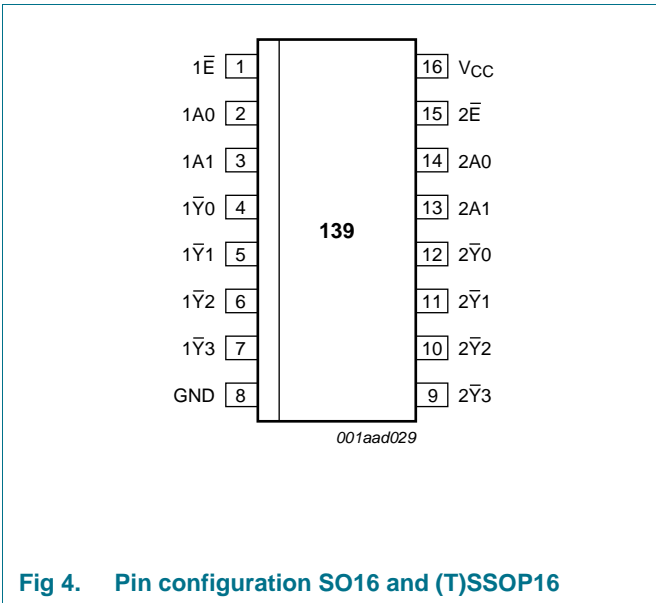


Fig 4. Pin configuration SO16 and (T)SSOP16

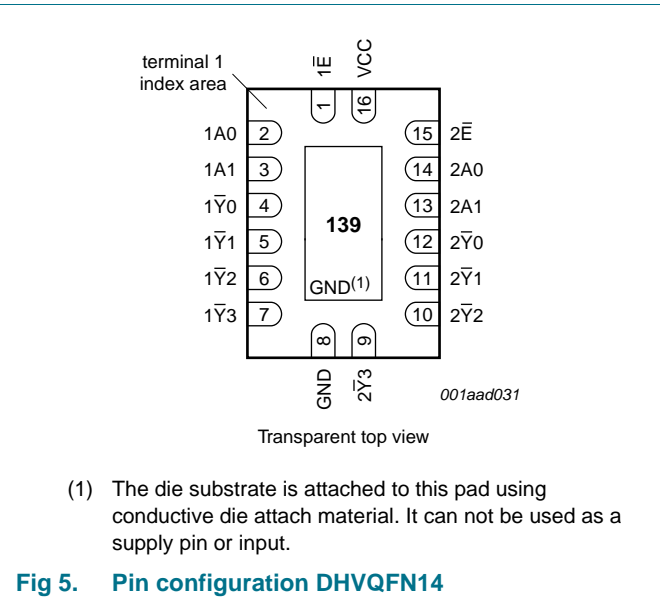


Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Name	Pin	Description
1E	1	enable input (active LOW)
2E	15	enable input (active LOW)
1A[0:1]	2, 3	address input
2A[0:1]	14, 13	address input
1Y[0:3]	4, 5, 6, 7	output

Table 2. Pin description ...continued

Name	Pin	Description
$2\bar{Y}[0:3]$	12, 11, 10, 9	output
GND	8	ground (0 V)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table^[1]

Input			Output			
nE	nA0	nA1	nY0	nY1	nY2	nY3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage		^[2] -0.5	$V_{CC} + 0.5$	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40		+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = -100\ \mu\text{A}; V_{CC} = 1.65\text{ V to }3.6\text{ V}$	$V_{CC} - 0.2$	-	-	$V_{CC} - 0.3$	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18\text{ mA}; V_{CC} = 3.0\text{ V}$	2.4	-	-	2.25	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = 100\ \mu\text{A}; V_{CC} = 1.65\text{ V to }3.6\text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_{CC} = 3.6\text{ V}; V_I = 5.5\text{ V or GND}$	-	± 0.1	± 5	-	± 20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin ; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to $\bar{Y}n$; see Figure 6 ^[2]						
		V _{CC} = 1.2 V	-	14	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	0.5	4.7	10.4	0.5	11.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.8	5.9	1.0	6.5	ns
		V _{CC} = 2.7 V	1.0	3.0	6.3	1.0	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	5.3	1.0	7.0	ns
		n \bar{E} to $\bar{Y}n$; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	14	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	4.5	9.8	1.5	10.7	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	2.7	5.6	2.1	6.1	ns
V _{CC} = 2.7 V	1.0	2.8	5.4	1.0	7.0	ns		
V _{CC} = 3.0 V to 3.6 V	1.0	2.4	5.0	1.0	6.5	ns		
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ^[4]						
		V _{CC} = 1.65 V to 1.95 V	-	5.6	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	11.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	16.4	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:

f_i = input frequency in MHz; f_o = output frequency in MHz

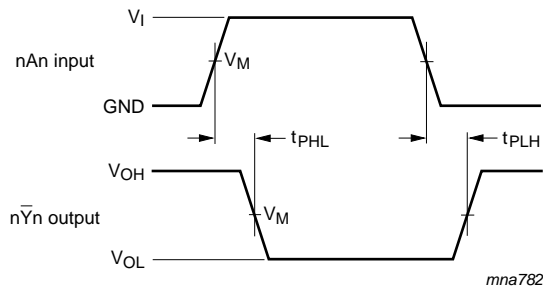
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching,

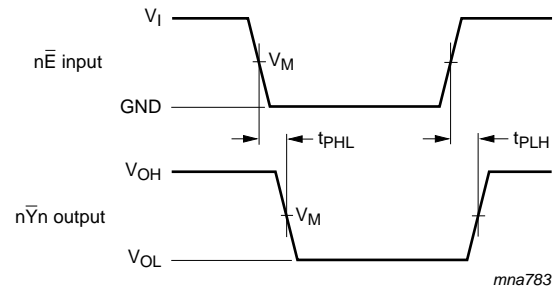
$$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

11. Waveforms



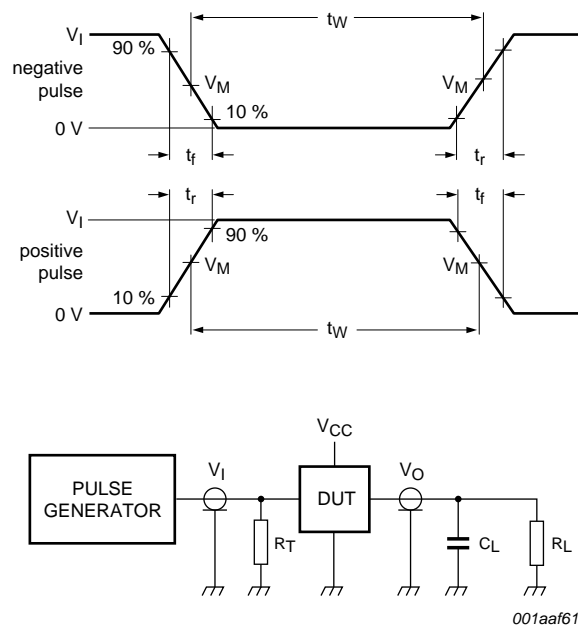
$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$.
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.
 V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 6. Input (nAn) to output (nYn) propagation delays



$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$.
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.
 V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 7. Enable input (nE) to output (nYn) propagation delays



Test data is given in [Table 8](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

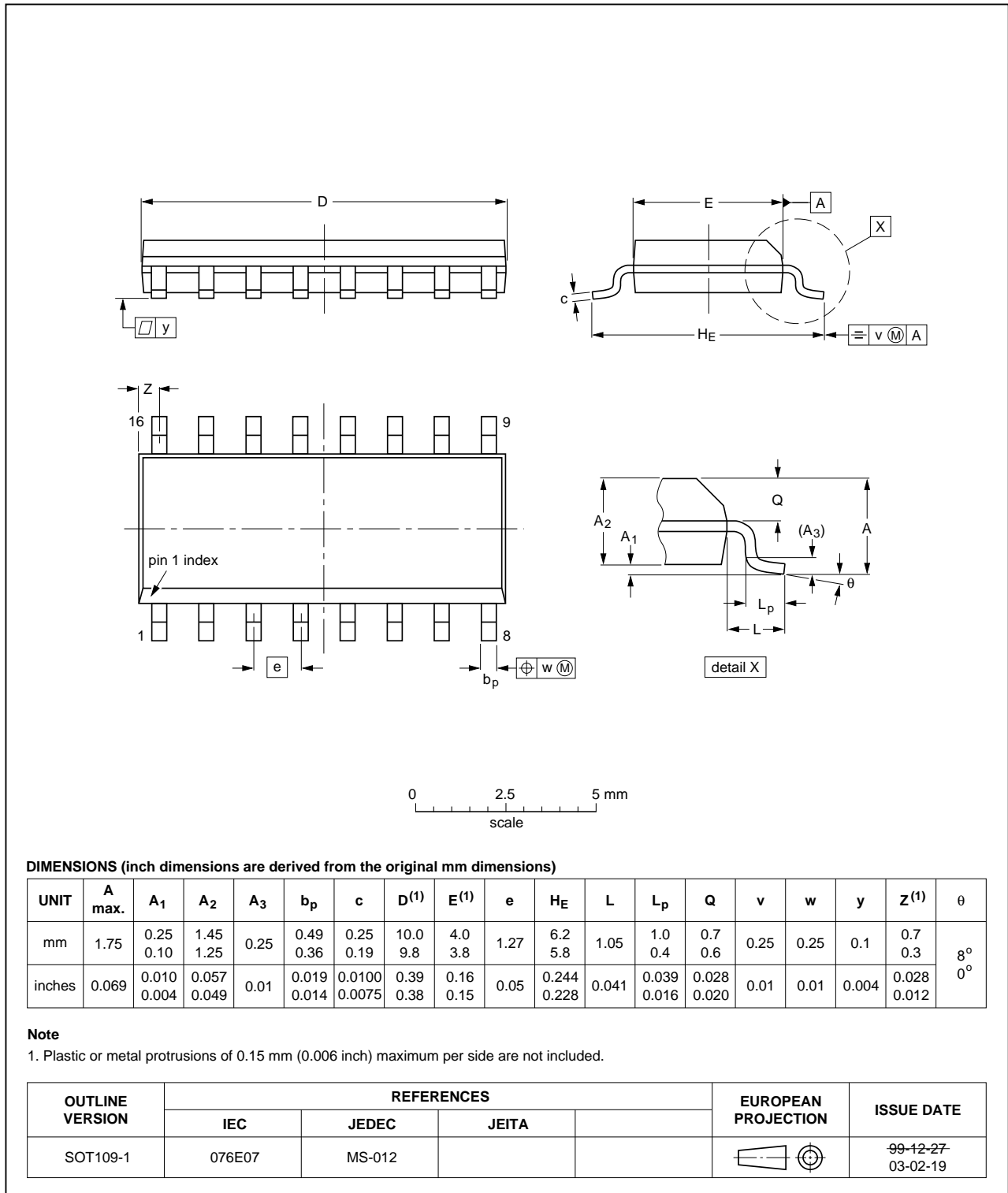


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

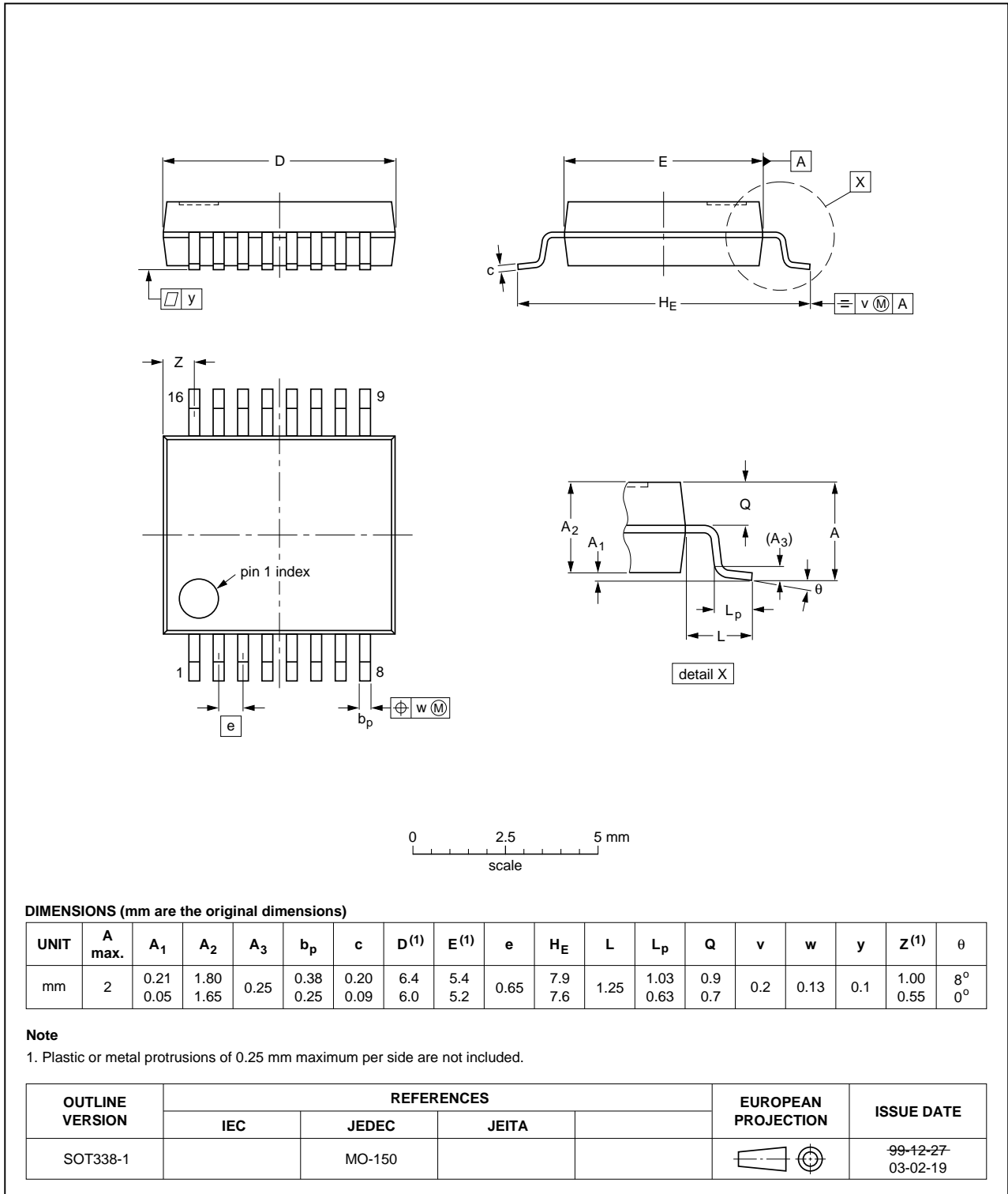


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

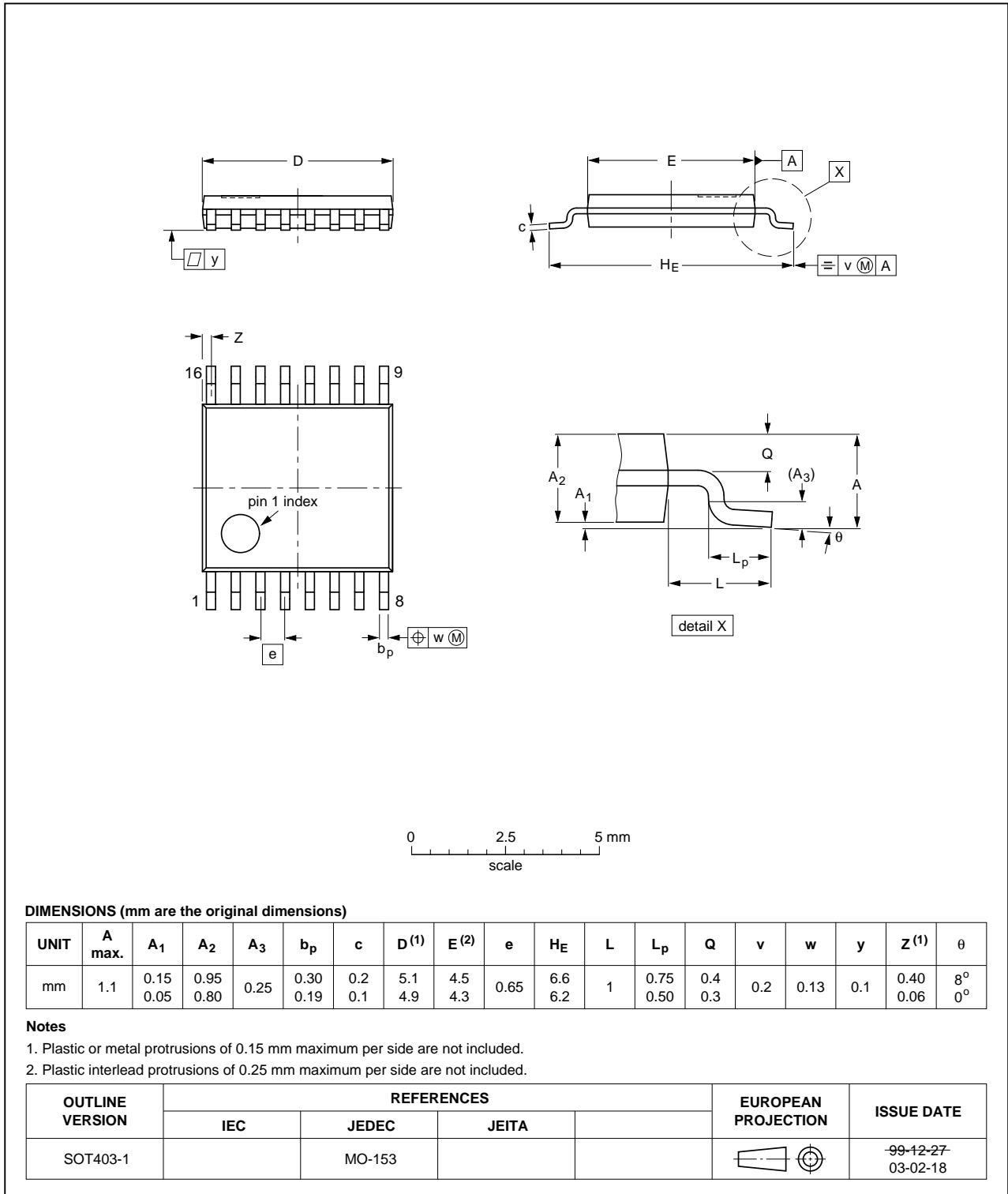


Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

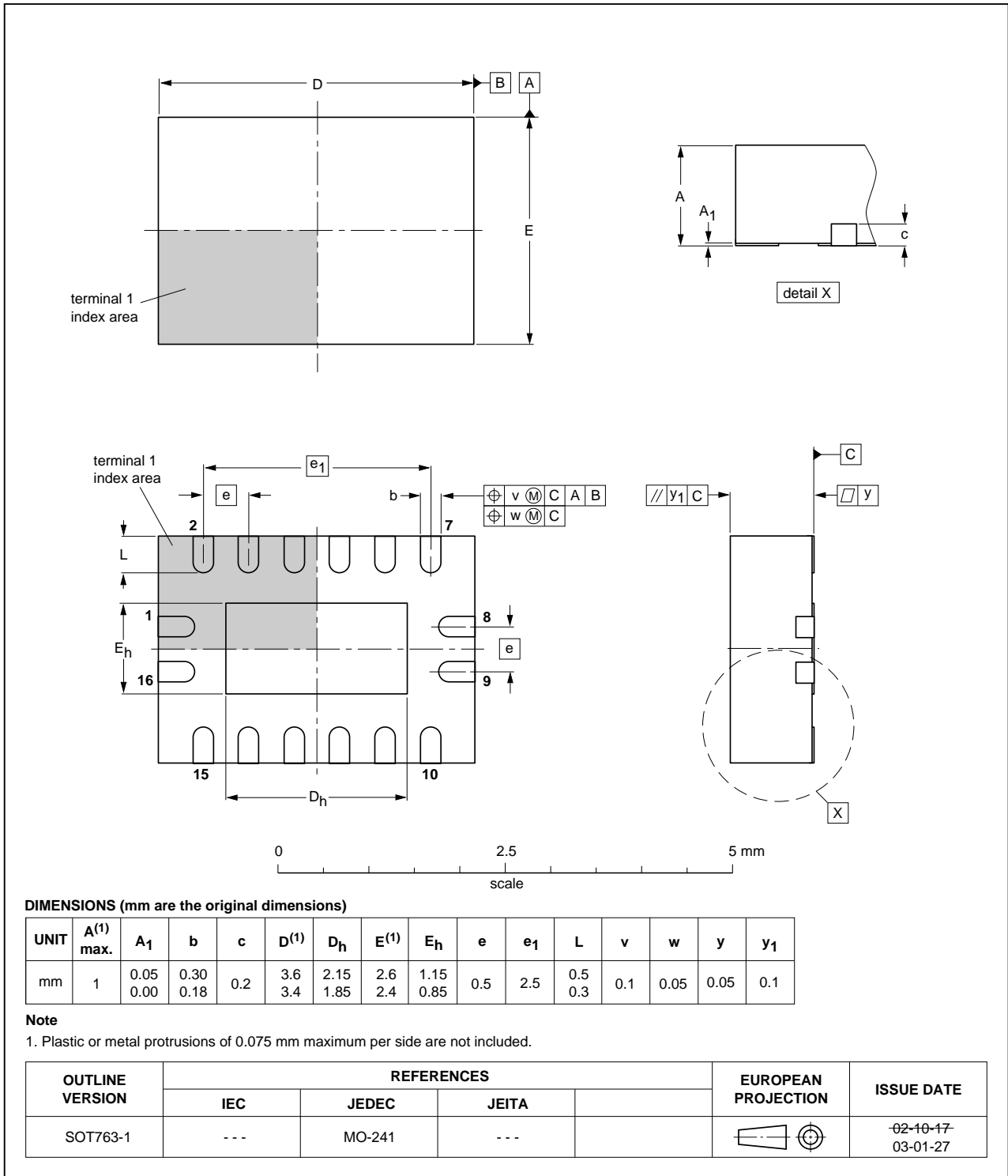


Fig 12. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC139 v.5	20111019	Product data sheet	-	74LVC139 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 			
74LVC139 v.4	040315	Product specification	-	74LVC139 v.3
74LVC139 v.3	030519	Product specification	-	74LVC139 v.2
74LVC139 v.2	980428	Product specification	-	74LVC139 v.1
74LVC139 v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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