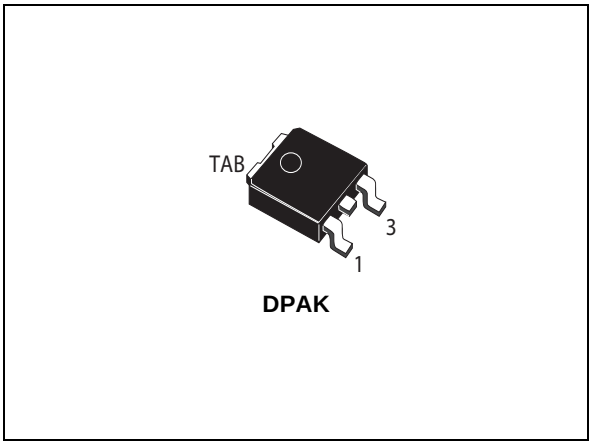
STD60N3LH5

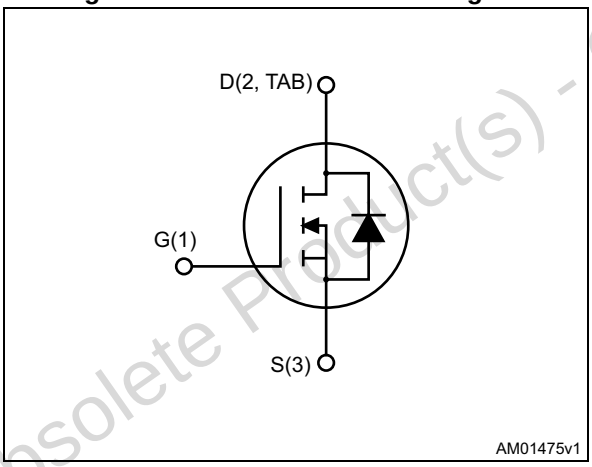
N-channel 30 V, 0.0072 Ω typ., 48 A STripFET™ V Power MOSFET in a DPAK package

Datasheet - not recommended for new design



DPAK

Figure 1. Internal schematic diagram



Features

Order code	$V_{DS\ @\ Tjmax}$	$R_{DS(on)}$ max	I_D
STD60N3LH5	35 V	0.008 Ω	48 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to a FOM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STD60N3LH5	60N3LH5	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{DS}	Drain-source voltage @ T_{jmax}	35	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	48	A
I_D	Drain current (continuous) at T_C = 100 °C	42.8	A
I_{DM} (2)	Drain current (pulsed)	192	A
P_{TOT}	Total dissipation at T_C = 25 °C	60	W
	Derating factor	0.4	W/°C
E_{AS} (3)	Single pulse avalanche energy	160	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Limited by wire bonding.
2. Pulse width limited by safe operating area.
3. Starting T_j = 25 °C, I_D = 24 A, V_{DD} = 12 V.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max.	50	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30 V V_{DS} = 30 V, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.8	3	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 24 A		0.0072	0.008	Ω
		V_{GS}= 5 V, I_D= 24 A		0.0088	0.011	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1350	1620	pF
C_{oss}	Output capacitance		-	265	318	pF
C_{rss}	Reverse transfer capacitance		-	32	38	pF
Q_g	Total gate charge	V_{DD}=15 V, I_D = 48 A V_{GS} =5 V (*Figure 14*)	-	8.8	12.3	nC
Q_{gs}	Gate-source charge		-	4.7	6.6	nC
Q_{gd}	Gate-drain charge		-	2.2	3.1	nC
Q_{gs1}	Pre V_{th} gate-to-source charge	V_{DD}=15 V, I_D = 48 A V_{GS} =5 V (*Figure 19*)	-	2.2	3.1	nC
Q_{gs2}	Post V_{th} gate-to-source charge		-	2.5	3.5	nC
R_G	Gate input resistance	f = 1 MHz, gate DC Bias = 0, test signal level = 20 mV, I_D = 0	-	1.1	1.3	Ω

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=10 V, I_D= 24 A, R_G=4.7 Ω, V_{GS}= 10 V (*Figure 13 and Figure 18*)	-	6	-	ns
t_r	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
t_f	Fall time		-	4.2	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		48	A
I_{SDM}	Source-drain current (pulsed)(1)		-		192	A
V_{SD}	Forward on voltage	I_{SD}=24 A, V_{GS}=0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD}=48 A, di/dt =100 A/µs, V_{DD}=20 V, (*Figure 15*)	-	25		ns
Q_{rr}	Reverse recovery charge		-	18.5		nC
I_{RRM}	Reverse recovery current		-	1.5		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

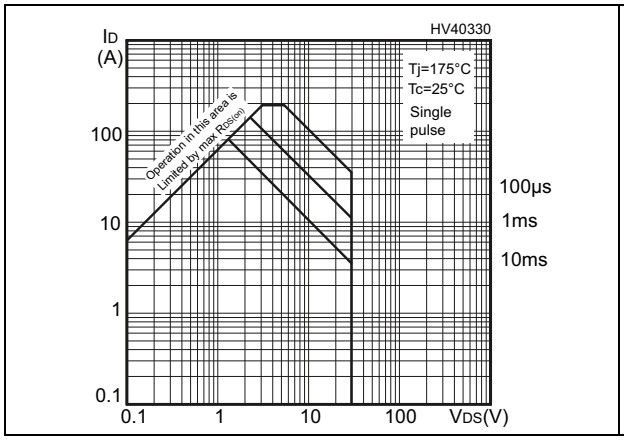


Figure 3. Thermal impedance

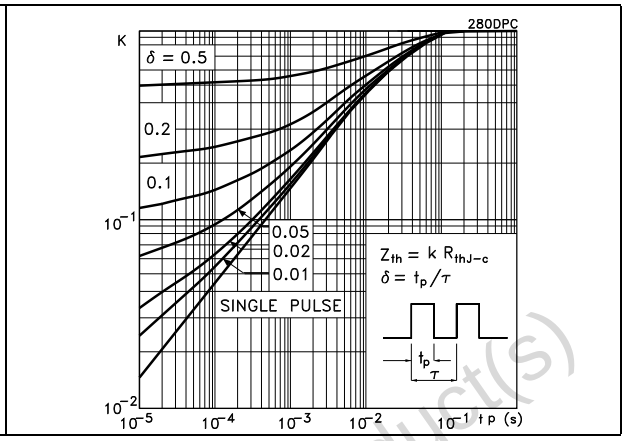


Figure 4. Output characteristics

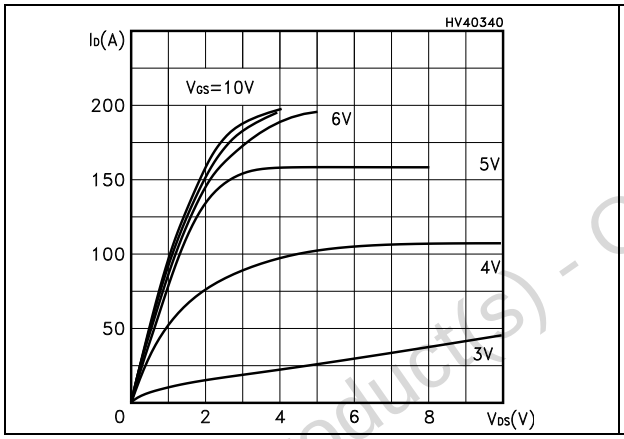


Figure 5. Transfer characteristics

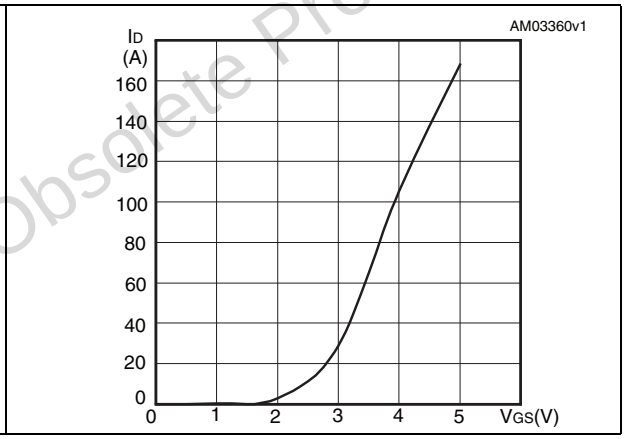


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

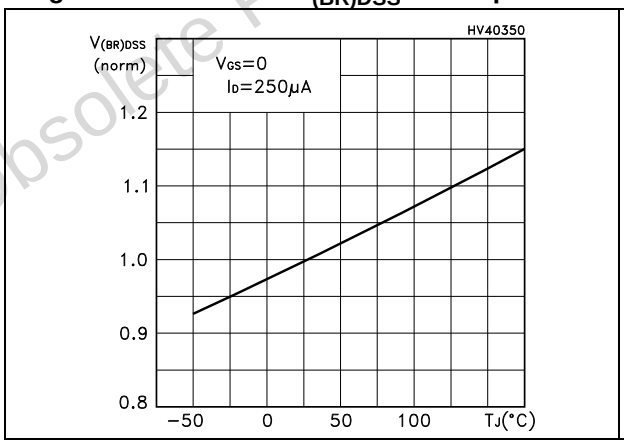


Figure 7. Static drain-source on-resistance

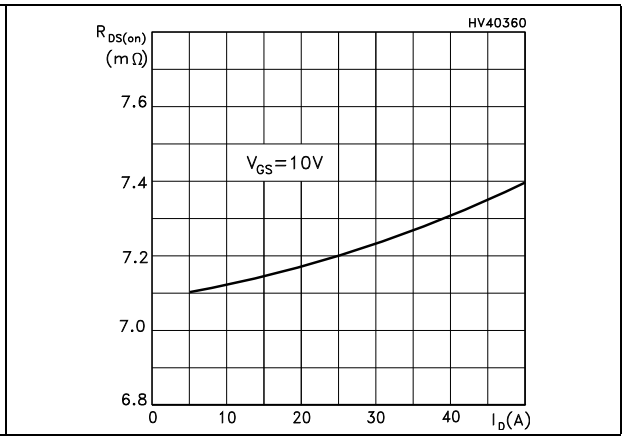


Figure 8. Gate charge vs gate-source voltage

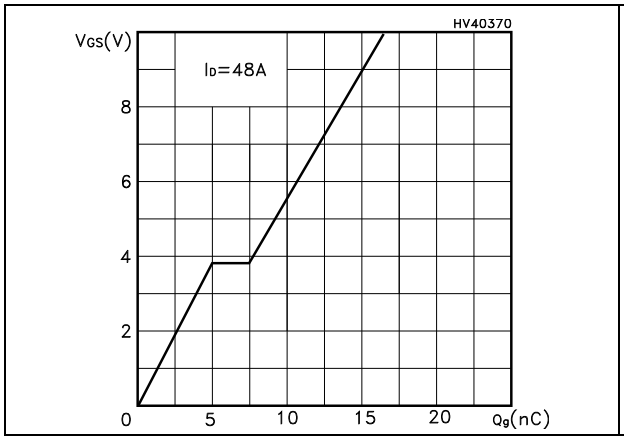


Figure 9. Capacitance variations

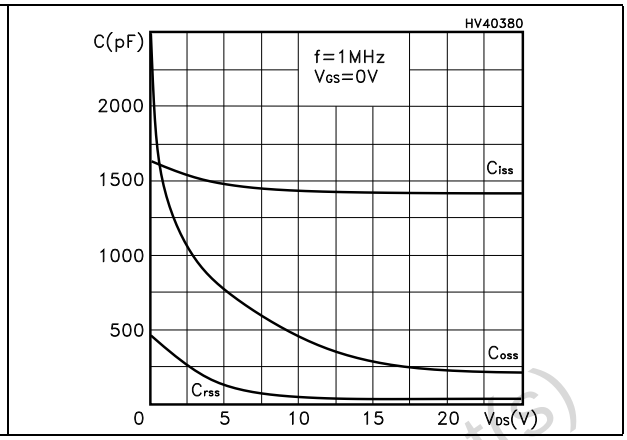


Figure 10. Normalized gate threshold voltage vs temperature

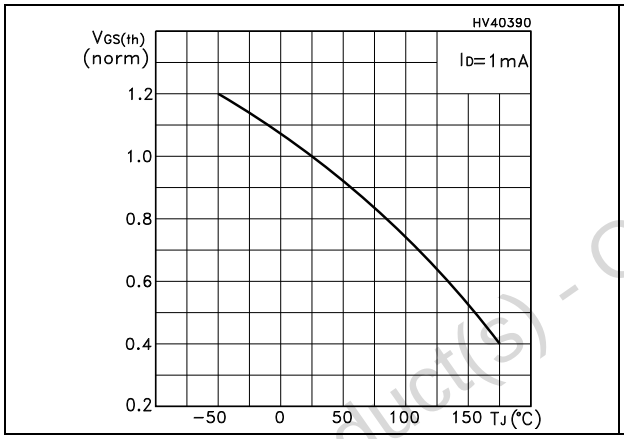


Figure 11. Normalized on-resistance vs temperature

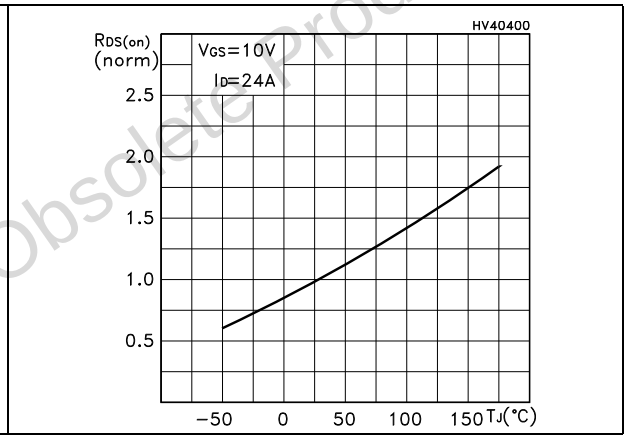
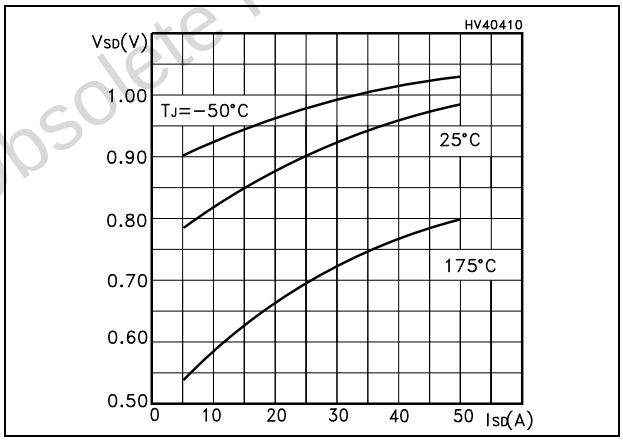


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

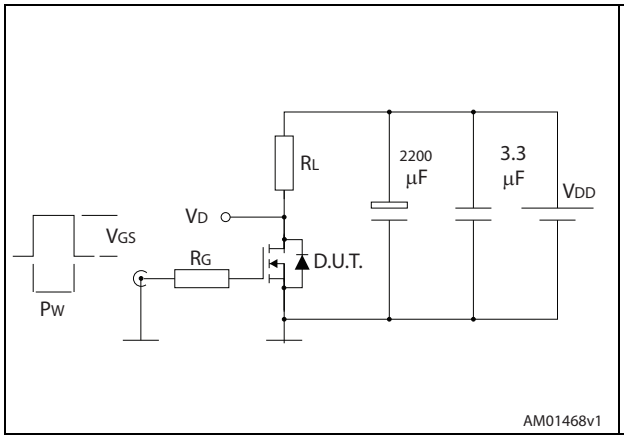


Figure 14. Gate charge test circuit

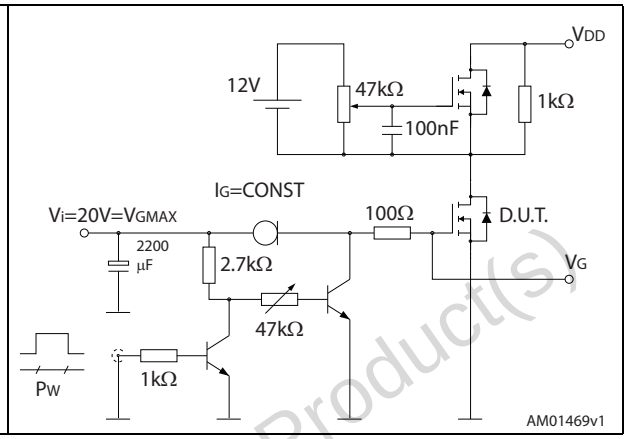


Figure 15. Test circuit for inductive load switching and diode recovery times

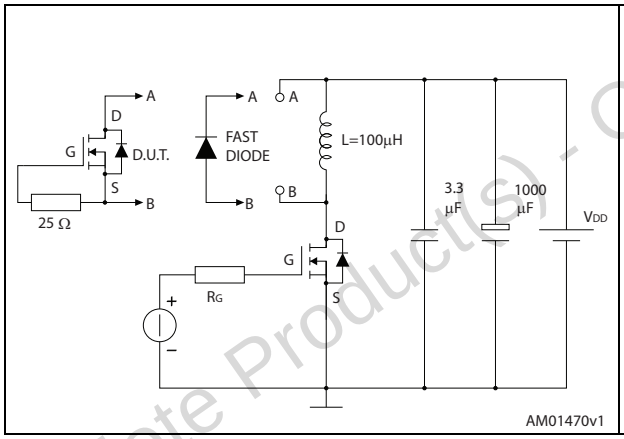


Figure 16. Unclamped inductive load test circuit

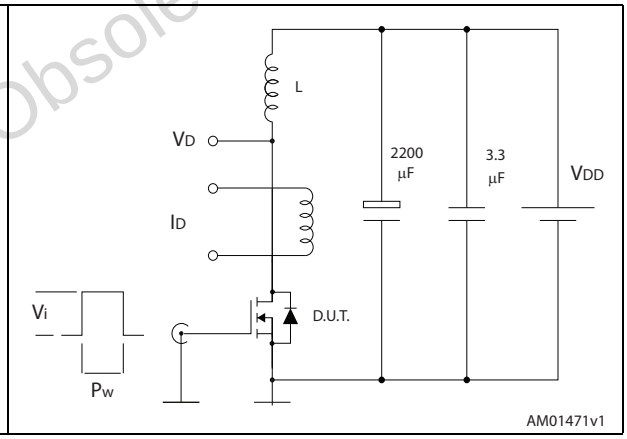


Figure 17. Unclamped inductive waveform

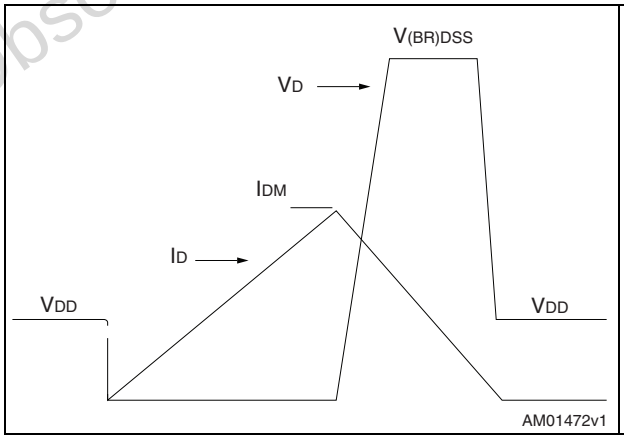


Figure 18. Switching time waveform

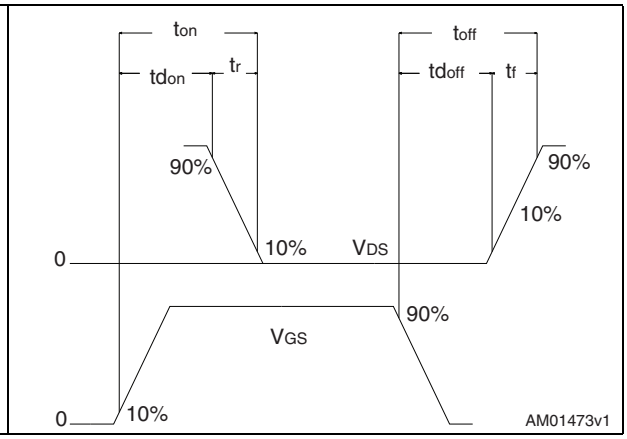
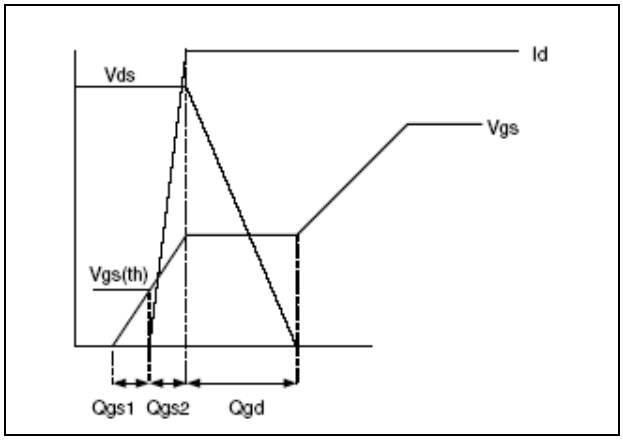


Figure 19. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) type A drawing

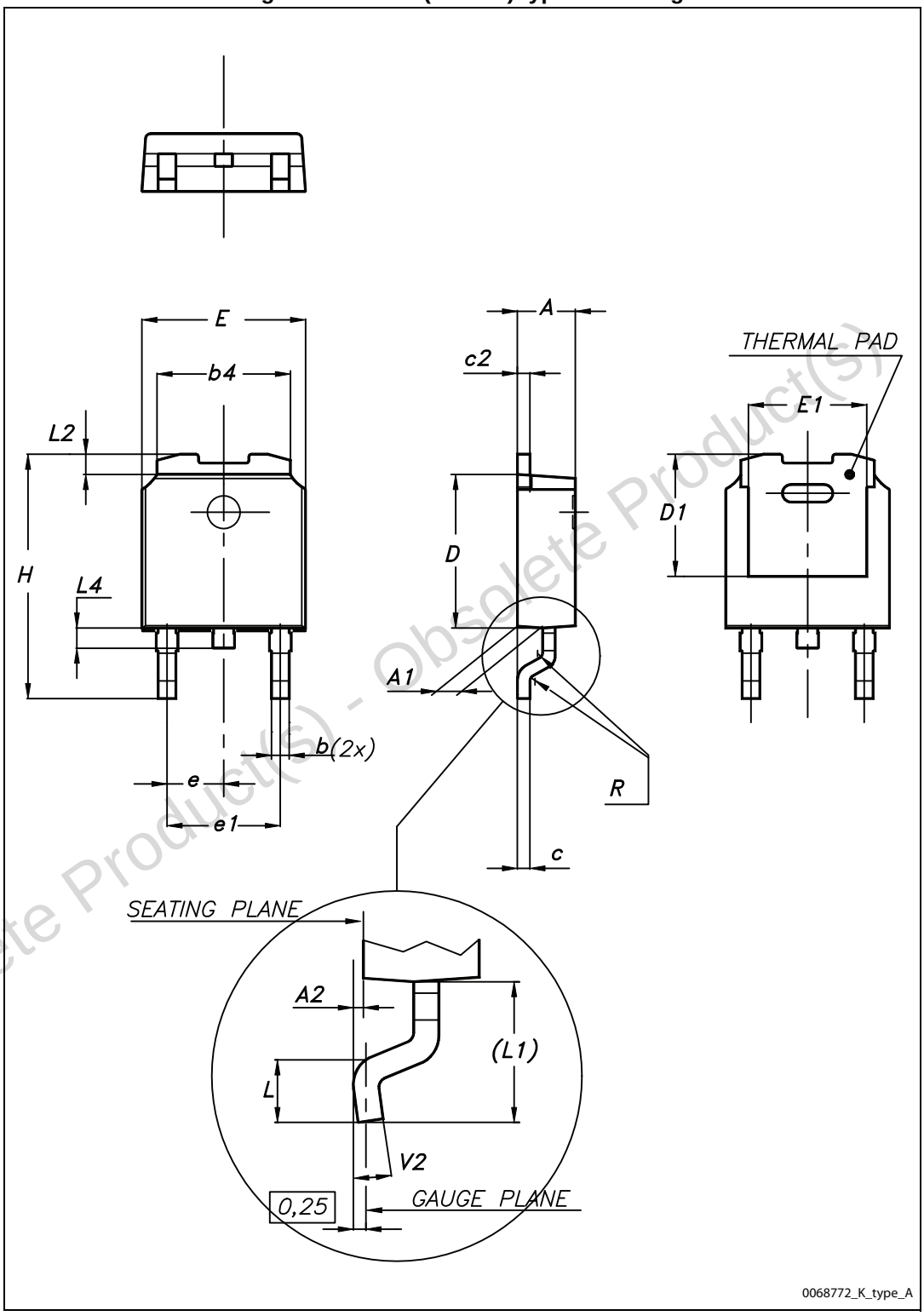


Table 9. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 21. DPAK (TO-252) type E drawing

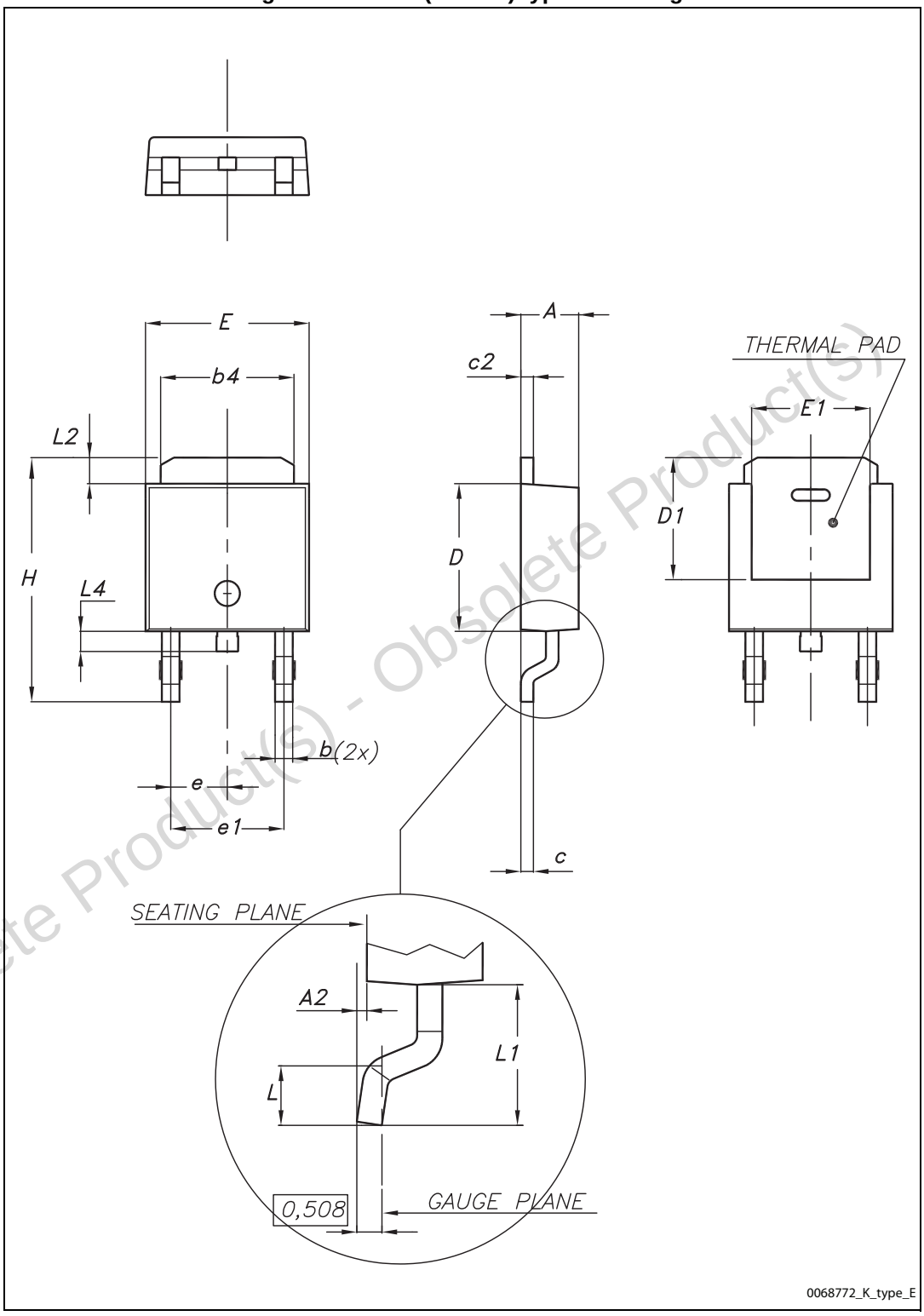
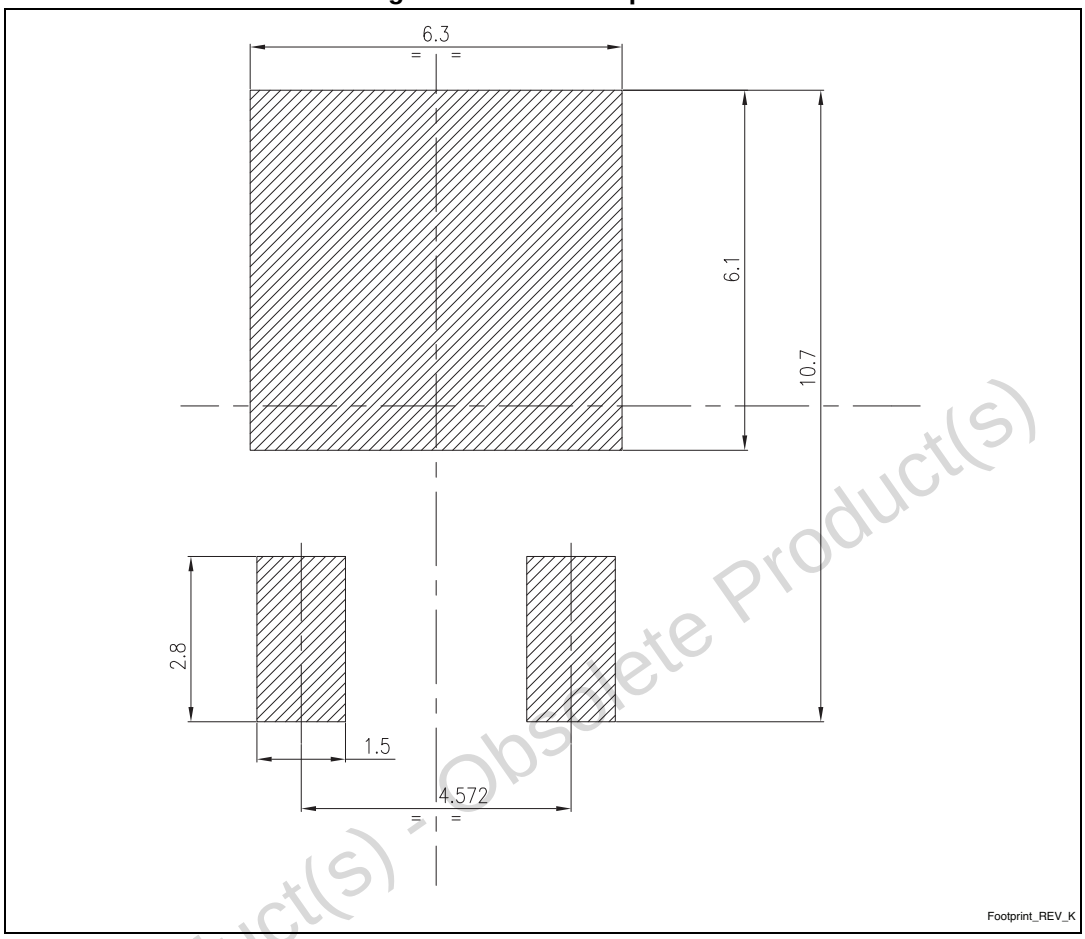


Figure 22. DPAK footprint [(a)]



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 23. Tape for DPAK (TO-252)

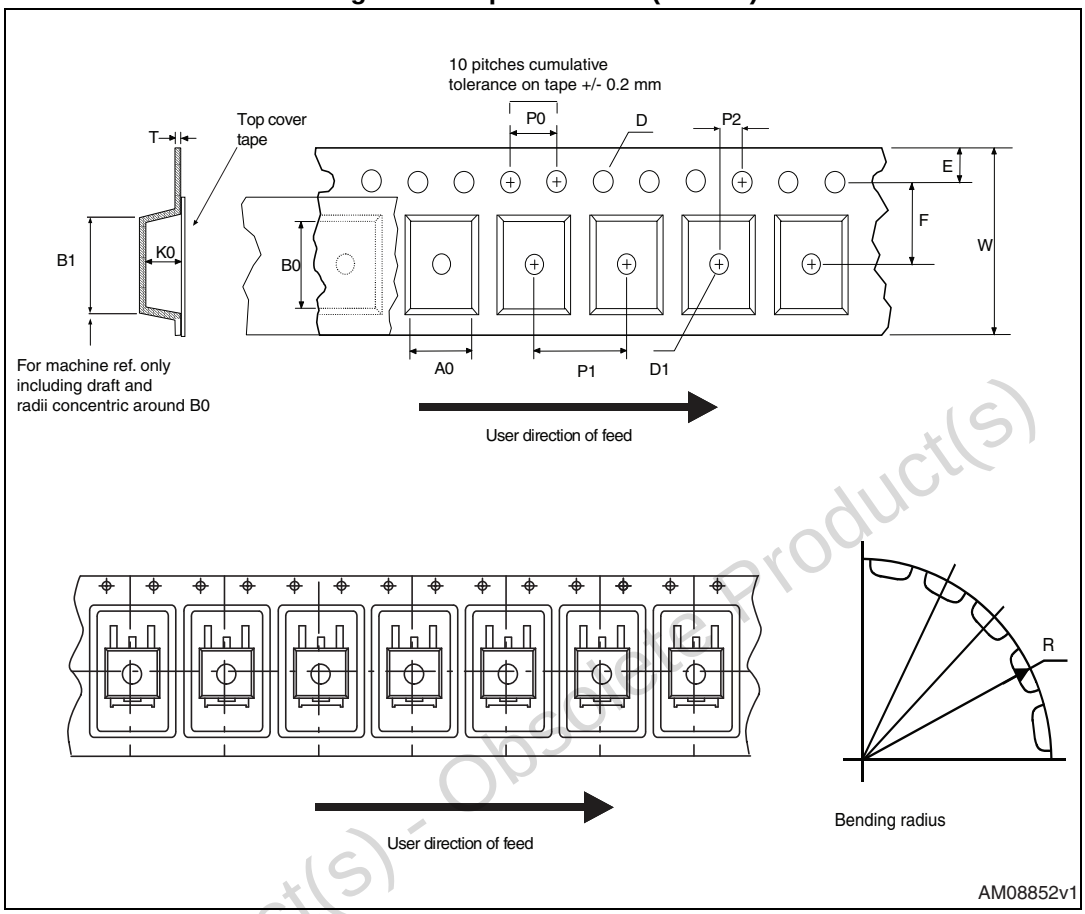
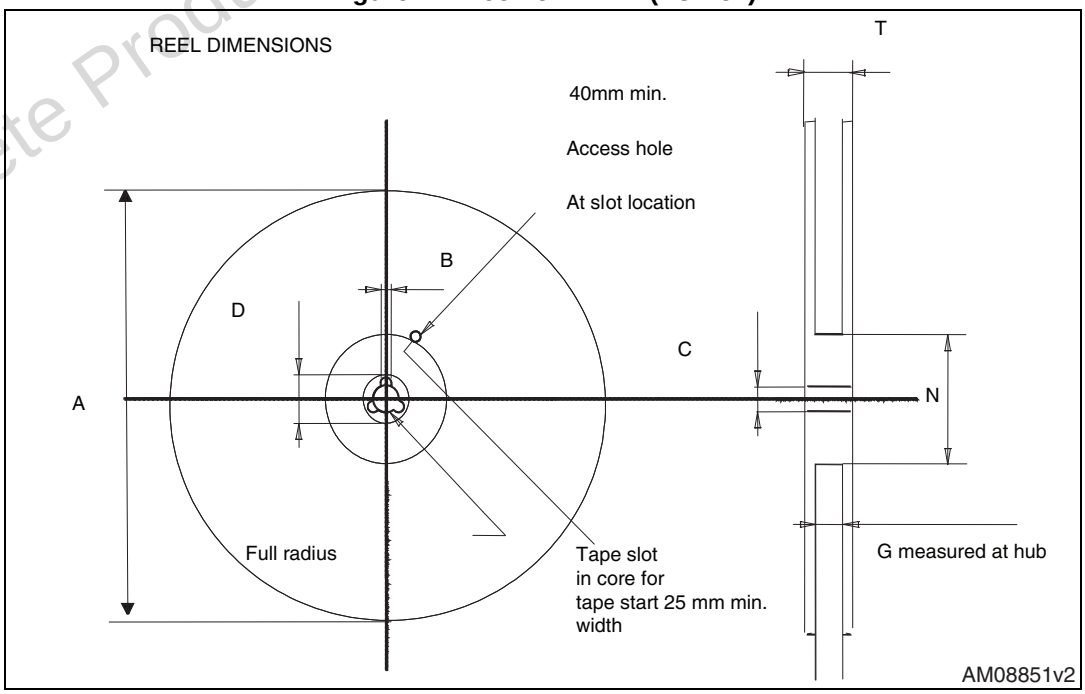


Figure 24. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Oct-2007	1	First release
23-Sep-2008	2	V_{GS} value has been changed on *Table 2* and *Table 5*
20-Apr-2009	3	– Inserted typical maximum value in $V_{GS(th)}$ parameter – *Figure 5: Transfer characteristics* has been updated – Added device in TO-220
05-Apr-2011	4	– Added device in Short IPAK – Added max values in *Table 5: Dynamic* – V_{GS} value has been changed in *Table 2* and *Table 4*
09-Aug-2013	5	The part numbers STP60N3LH5, STU60N3LH5 and STU60N3LH5-S have been moved to a separate datasheet

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