NCP2830

1W Constant Filterless Class-D Audio Amplifier

NCP2830 is a cost effective mono audio power amplifier designed for portable communication device applications such as mobile phones. Due to its integrated charge pump structure, this part is capable of delivering 1 W of continuous average power to an 8.0 Ω Bridge Tied Load no matter the voltage provided by a lithium/Ion battery.

NCP2830 is a preferred solution for long playback audio with minimum space required.

Added to a fast start−up time of 200 μs and a −88dB PSRR, the NCP2830 audio power amplifier is specifically designed to provide high quality and level output power from low supply voltage, requiring very few external components.

Features

- 1 W to 8 Ω load for V_{DD} from 2.7 V up to 5.5 V
- High quality audio (THD+N = 0.04%)
- Low noise: SNR up to 100 dB
- Very Fast Turn On Time: 200 μs
- Overall system efficiency optimization: up to 89%
- Superior PSRR (−88 dB): Direct Connection to Battery
- Very Low Quiescent Current 7 mA
- Optimized PWM Output Stage: Filterless Capability
- Selectable gain of 2 V/V or 4 V/V
- Fully Differential Capability:
- Thin QFN 3x3 mm, 20 pins
- This Device uses Halogen−Free Molding Compound
- This is a Pb−Free Device

Typical Applications

- Cellular Phones and Digital Cameras
- Personal Digital Assistant and Portable Media Player
- Audio Accessories
- GPS

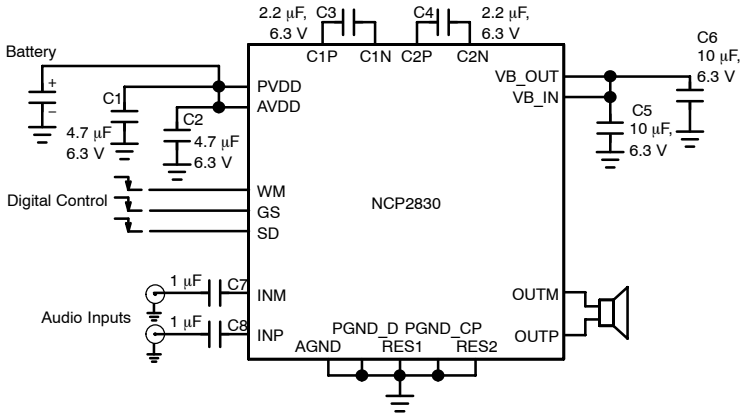


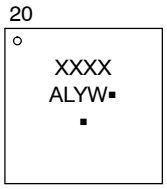
Figure 1. Typical Application Circuit

ON Semiconductor®

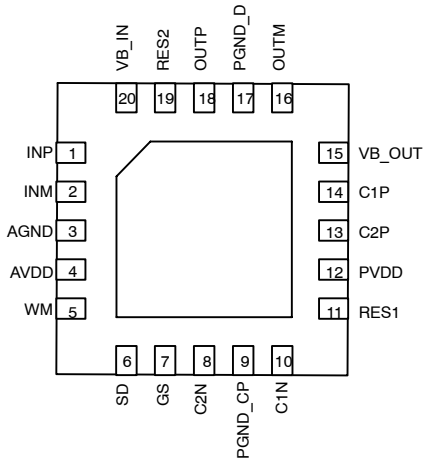
http://onsemi.com

MARKING DIAGRAM

UQFN20
MU SUFFIX
CASE 523AL



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package



(TOP VIEW)
20−Pin 3 x 3 x 0.50 mm QFN
Exposed pad must be soldered to PCB Ground Plane

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

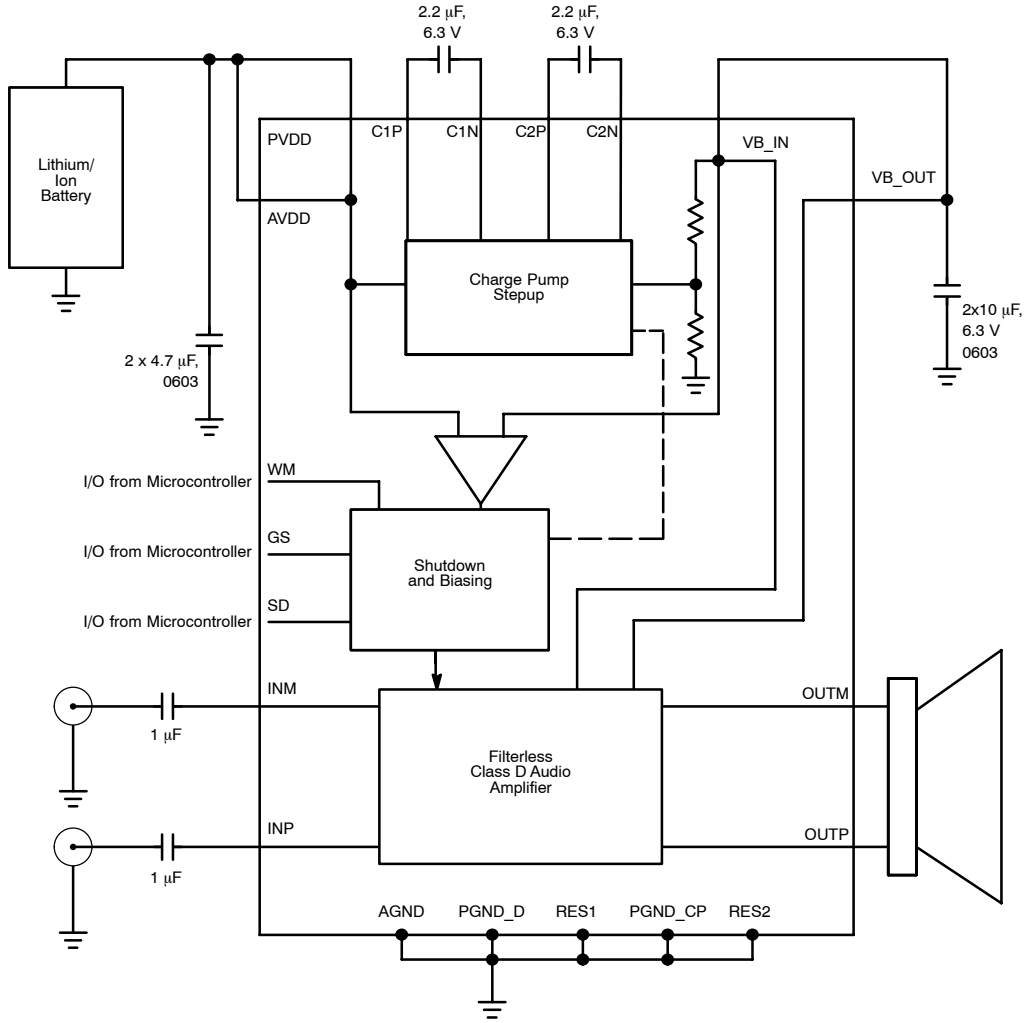


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
20	VB_IN	I	This pin must be externally connection in a star configuration with Pin n°15. The C_{out} filtering (10 μF/6.3 V/0603) capacitor must be connected as close as possible to the connection point.
3	AGND	P	Ground. These pins must be connected separately to the dedicated Ground plane with a minimum of track length. Thus, a star connection is required.
9	PGND_CP	P	Ground. These pins must be connected separately to the dedicated Ground plane with a minimum of track length. Thus, a star connection is required.
17	PGND_D	P	Ground. These pins must be connected separately to the dedicated Ground plane with a minimum of track length. Thus, a star connection is required.
4, 12	AVDD PVDD	P	These pins are dedicated to the signal connection for the battery input. They must be connected to the power source (ie lithium/Ion battery) in a star mode. It must be decoupled by a low ESR ceramic capacitor. (4.7 μF/6.3 V/0603). The use of a 4 or more layers board is advised. In that case, a dedicated plane for this battery voltage is mandatory.
1	INP	I	Positive audio input of the fully differential filterless Class D Audio Amplifier
2	INM	I	Negative audio input of the fully differential filterless Class D Audio Amplifier
16	OUTM	O	Negative audio output of the fully differential filterless Class D Audio Amplifier
18	OUTP	O	Positive audio output of the fully differential filterless Class D Audio Amplifier
5	WM	I	Wire Mode pin: When a low level is applied to this pin, the device operates in Normal mode (V_B = 5 V typ.). In case of a high level, it switches to a Wire Mode (V_B = V_{DD})
6	SD	I	Shutdown input. The device enters in shutdown mode when a low level is applied on this pin.
7	GS	I	Gain Select Input. When a low level is applied to this pin, an internal 2 V/V gain is setup. In case of a high level, it switches to an internal 4 V/V gain.
8	C2N	P	One side of the external charge pump capacitor is connected to this pin, associated with C2P. Using a low ESR ceramic capacitor is recommended to optimize charge pump efficiency (2.2 μF/6.3 V/0603 recommended).
10	C1N	P	One side of the external charge pump capacitor is connected to this pin, associated with C1P. Using a low ESR ceramic capacitor is recommended to optimize charge pump efficiency (2.2μF/6.3V/0603 recommended).
13	C2P	P	One side of the external charge pump capacitor is connected to this pin, associated with C2N. Using a low ESR ceramic capacitor is recommended to optimize charge pump efficiency (2.2 μF/6.3 V/0603 recommended).
14	C1P	P	One side of the external charge pump capacitor is connected to this pin, associated with C1N. Using a low ESR ceramic capacitor is recommended to optimize charge pump efficiency (2.2 μF/6.3 V/0603 recommended).
15	VB_OUT	O	This pin must be externally connection in a star configuration with Pin n°20. The C_{out} filtering (10 μF/6.3 V/0603) capacitor must be connected as close as possible to the connection point. This V_B input is dedicated to supply the internal power stages. Thus, it must be connected to C_{out} with the lowest impedance connection.
11	RES1	I	Reserved for production. Must be connected to GND plane in final application
19	RES2	I	Reserved for production. Must be connected to GND plane in final application

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
AVDD, PVDD Pins: Power Supply Voltage (Note 2)		V_{IN}	− 0.3 to + 7.0	V
Digital Input WM; SD; GS Pin:	Input Voltage Input Current	V_{DG} I_{DG}	−0.3 to V_{DD} + 0.3 1	V mA
Human Body Model (HBM) ESD Rating are (Note 3)		ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)		ESD MM	200	V
Latch up Current Maximum Rating		I_{LU}	(Note 4)	mA
QFN 3 x 3 mm Package (Note 7) Thermal Resistance Junction−to−Case		$R_{\theta JC}$	29 (Note 7)	°C/W
Operating Ambient Temperature Range		T_A	−40 to +85	°C
Operating Junction Temperature Range		T_J	−40 to +125	°C
Maximum Junction Temperature (Note 6)		T_{JMAX}	+150	°C
Storage Temperature Range		T_{STG}	−65 to +150	°C
Moisture Sensitivity (Note 5)		MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25 °C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating:
   ±100 mA for all pins, except digital pins per JEDEC standard: JESD78 class II.
   ±10mA for Digital Pins per JEDEC standard: JESD78 class II
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 150°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent of the PCB heat dissipation. The maximum power dissipation (PD) is dependent by the min input voltage, the max output current and external components selected.

$$R_{\theta CA}\frac{125 - T_A}{P_D} - R_{\theta JC}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 3.6 V (Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GLOBAL SYSTEM						
V_{DD}	Operating System Voltage		2.7	–	5.5	V
I_{SD}	Shutdown Current	V_{SD} = low, V_{GS} = Low, V_{WM} = Low	–	0.01	–	μA
I_{SD}	Shutdown Current	V_{SD} = low, V_{GS} = Low, V_{WM} = Low, V_p = 5.5 V (Note 9)	–	–	1.5	μA
I_Q	Quiescent Current	2X Mode, No load	–	9.5	11	mA
I_Q	Quiescent Current	1.5X Mode, No load	–	7	8	mA
I_Q	Quiescent Current	Wire Mode, No load	–	3	4.5	mA
R_{SD}	Resistance from SD to GND		–	350	–	kΩ
R_{WM}	Resistance from WM to GND		–	350	–	kΩ
R_{GS}	Resistance from GS to GND		–	350	–	kΩ
V_{IH}	Digital Pins High Voltage		1.2	–	–	V
V_{IL}	Digital Pins Low Voltage		–	–	0.4	V
BOOST SECTION						
F_{SW1}	Charge Pump Switching Frequency		550	650	750	kHz
V_B	Output Regulated Voltage	No Load, V_{INM}=V_{INP}=0, V_{WM}= Low, 2X Mode	4.75	5	5.25	V
V_B	Output Regulated Voltage	No Load, V_{INM} = V_{INP} = 0, V_{WM} = Low, 1.5X Mode	4.75	5	5.25	V
$V_{B-Ripple}$	Output Voltage Ripple	No Load, V_{INM} = V_{INP} = 0, V_{WM} = Low, 2X Mode or 1.5X Mode	–	7	–	mV
$T_{Precharge}$	Precharge time	C5 = C6 = 10 μF	–	1.6	–	ms
V_{TR1}	Transition Voltage between 2X Mode and 1.5X Mode		–	3.8	–	V
V_{TR2}	Transition Voltage between 2X Mode and Wire Mode		–	4.65	–	V
CLASS D SECTION						
F_{SW2}	Class D Switching frequency		275	325	375	kHz
R_{INL}	Audio Input resistance	V_{GS} = Low (Note 10)	–	15	–	kΩ
R_{INH}	Audio Input resistance	V_{GS} = High (Note 10)	–	7.5	–	kΩ
Z_{SD}	Shutdown impedance	V_{SD} = Low	–	20	–	kΩ
G_{HI}	Gain High	V_{GS} = High, RL = 8 Ω	1.85	2	2.15	V/V
G_{LO}	Gain Low	V_{GS} = Low, RL = 8 Ω	3.7	4	4.3	V/V
V_{OS}	Output Offset Voltage	V_{INM} = V_{INP} = 0	–	1	–	mV
T_{start}	Turn ON time	V_B = V_{DD}, V_{SD} = High	–	200	–	μs
T_{OFF}	Turn Off time		–	1	–	μs
V_N	Output Noise Voltage	No Filter	–	56	–	μV_{RMS}
V_N	Output Noise Voltage	A−Weighting filter	–	37	–	μV_{RMS}
THD+N	Total harmonic distortion + Noise	P_{out} = 0.25 W, f = 1 kHz, R_L = 8 Ω	–	0.04	–	%
THD+N	Total harmonic distortion + Noise	P_{out} = 1 W, f = 1 kHz, R_L = 8 Ω	–	0.2	–	%

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C.
9. The maximum value is measured at 85°C
10. Guaranteed by design

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 3.6 V (Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CLASS D SECTION						
PSRR	Power Supply Rejection Ratio	V_{in} = AC Grounded, f = 217 Hz, V_{WM} = V_{GS} = Low, V_{RIPPLE} = 200 mV_{PP}	–	−88	–	dB
CMRR	Common mode rejection ratio	Vic = 1 V_{PP} f = 1 kHz				dB
		V_{GS} = Low	–	−70	–	
		V_{GS} = High	–	−60	–	
η	Efficiency	R_L = 8 Ω				%
		V_{DD} = 5 V; P_{out} = 1 W	–	89	–	
		V_{DD} = 2.7 V; P_{out} = 0.5 W	–	80	–	
P_{OUT}	Output Power	THD+N < 10%, f = 1 kHz, V_{WM} = Low	1	1.2	–	W

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C.
9. The maximum value is measured at 85°C
10. Guaranteed by design

TYPICAL OPERATING CHARACTERISTICS

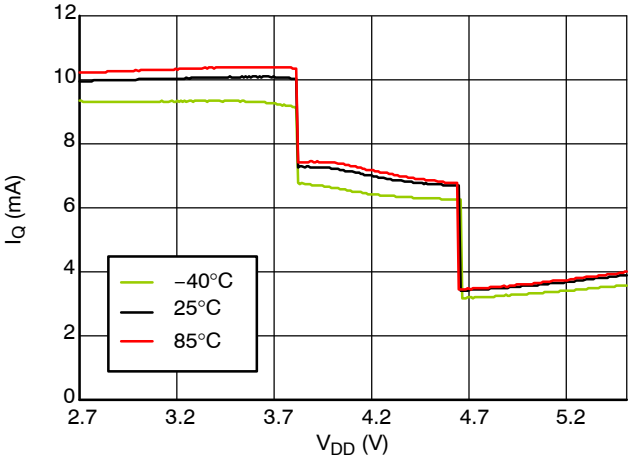


Figure 3. I_Q vs V_{DD}

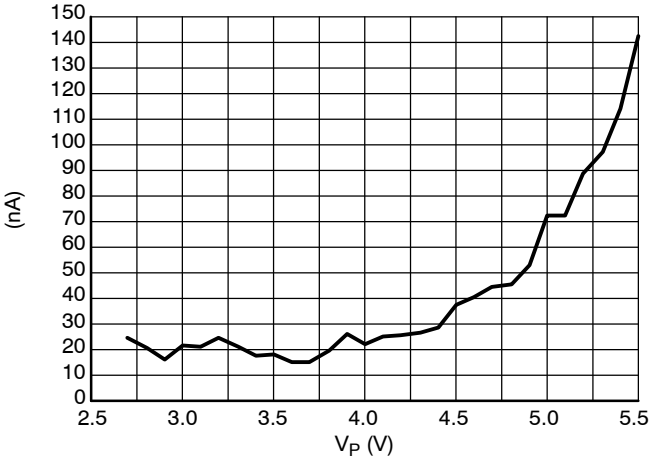


Figure 4. I_{SD} vs V_{DD}

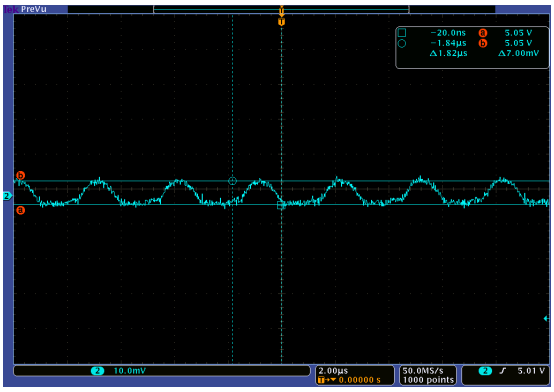


Figure 5. VB Output Ripple

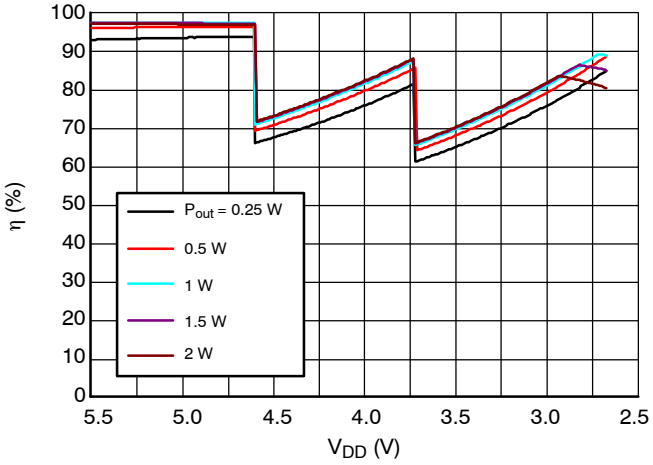


Figure 6. Boost efficiency vs Output Power

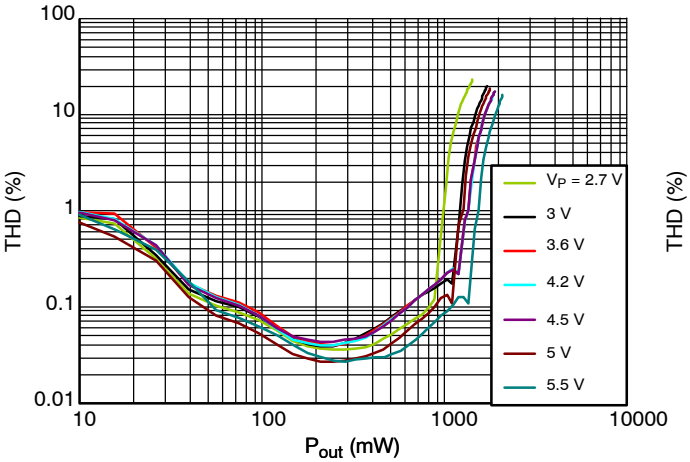


Figure 7. THD vs P_{out} R_L = 8 Ω, WM = Low

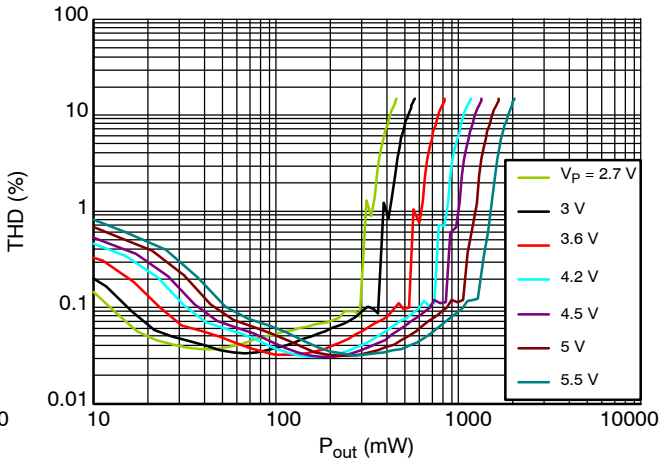


Figure 8. THD vs P_{out} R_L = 8 Ω, WM = High

TYPICAL OPERATING CHARACTERISTICS

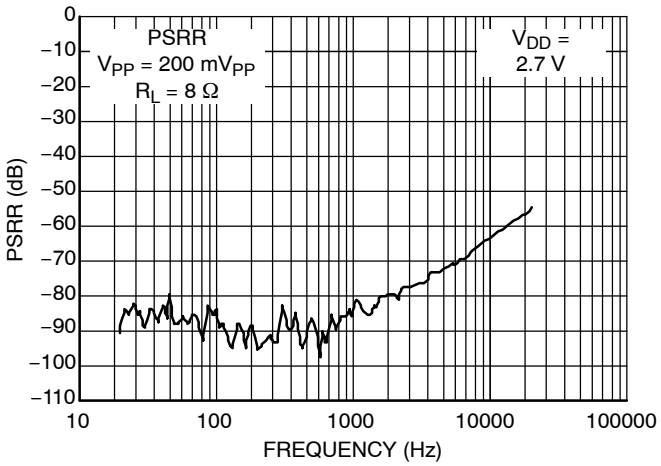


Figure 9. PSRR vs Frequency

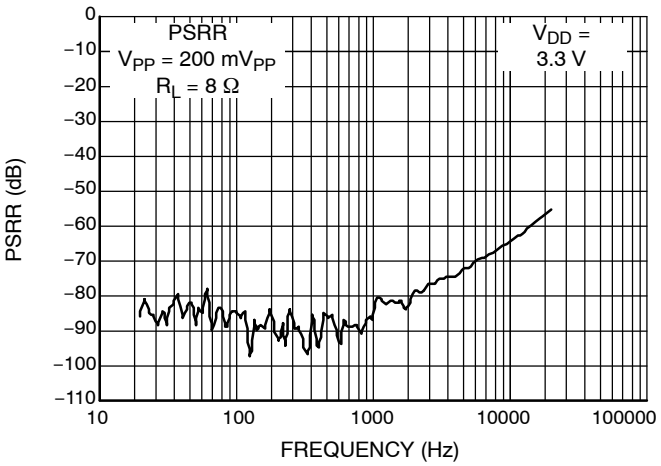


Figure 10. PSRR vs Frequency

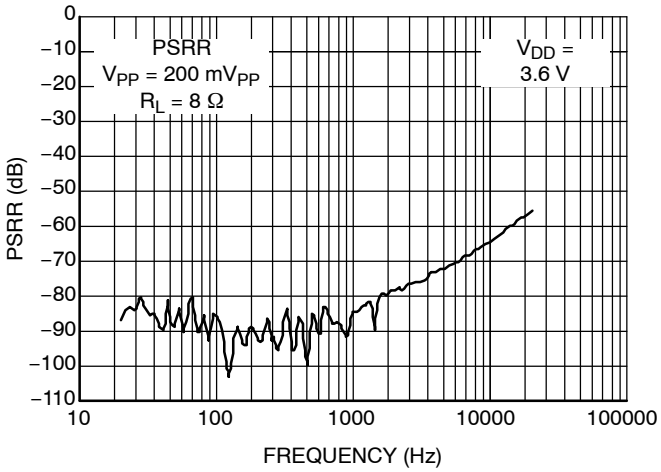


Figure 11. PSRR vs Frequency

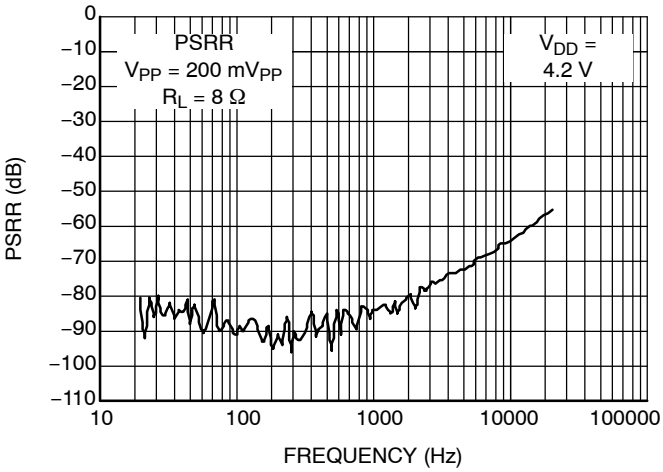


Figure 12. PSRR vs Frequency

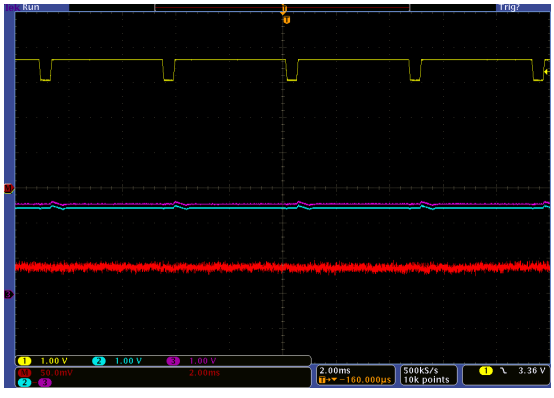


Figure 13. Outputs Behavior During GSM Burst

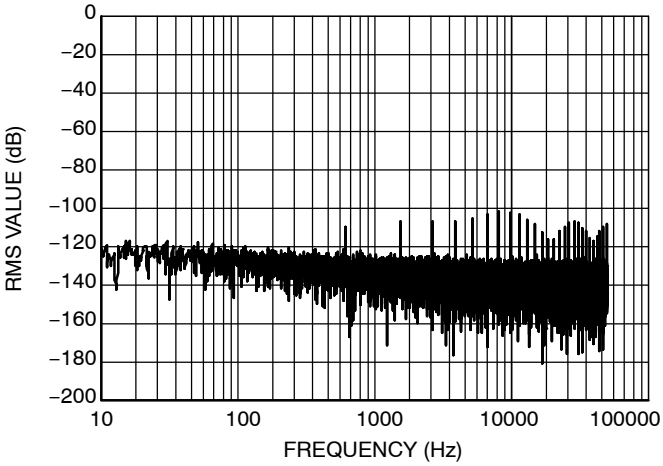


Figure 14. FFT of Switching Signal During GSM Burst

TYPICAL OPERATING CHARACTERISTICS

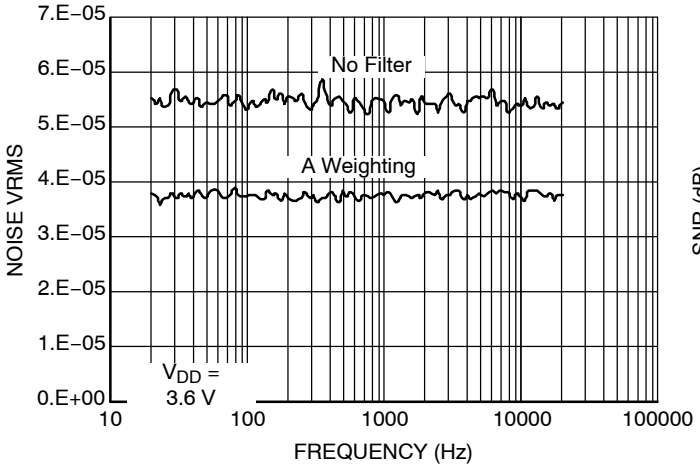


Figure 15. Noise vs Frequency

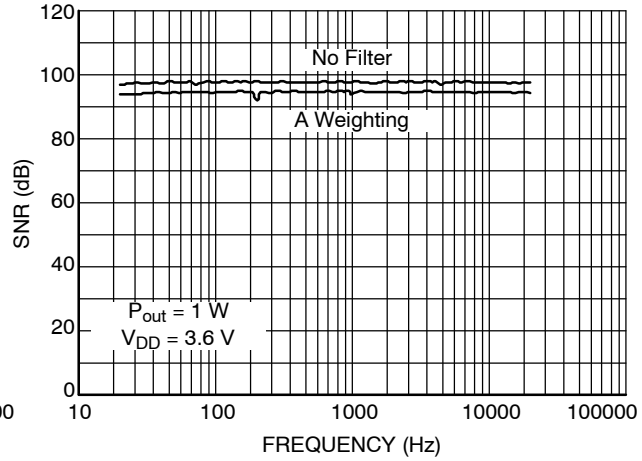


Figure 16. SNR vs Frequency

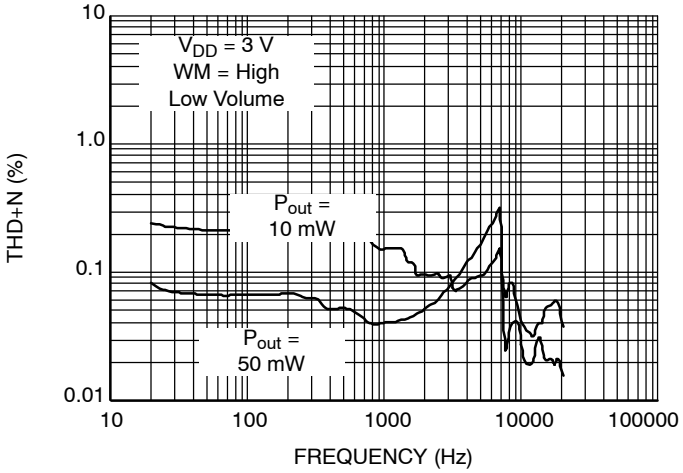


Figure 17. THD+N vs Frequency

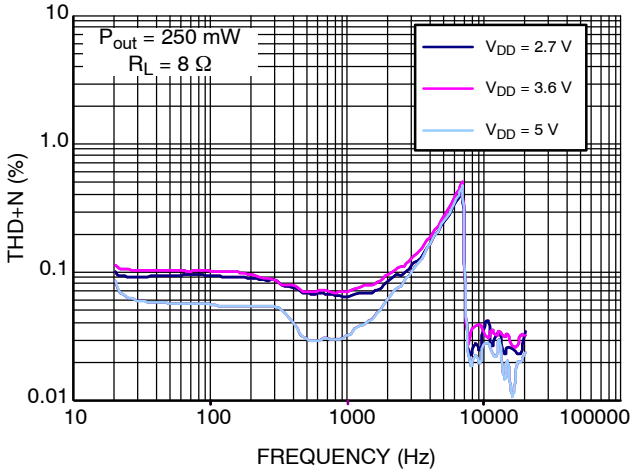


Figure 18. THD+N vs Frequency

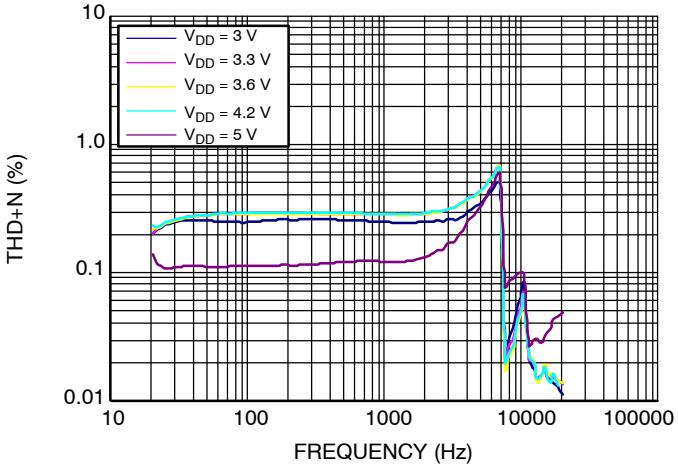


Figure 19. THD+N vs Frequency

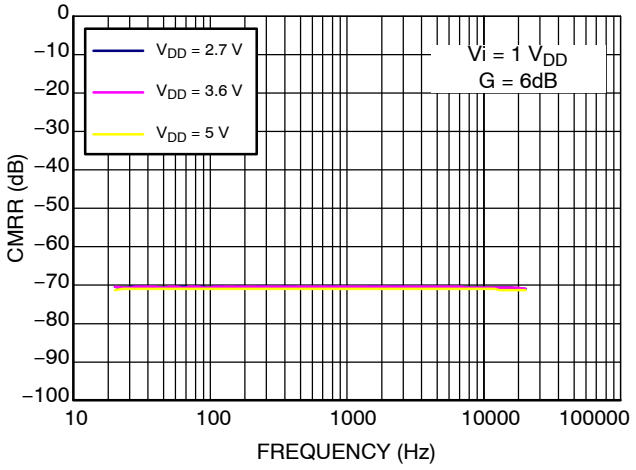


Figure 20. CMRR vs Frequency

TYPICAL OPERATING CHARACTERISTICS

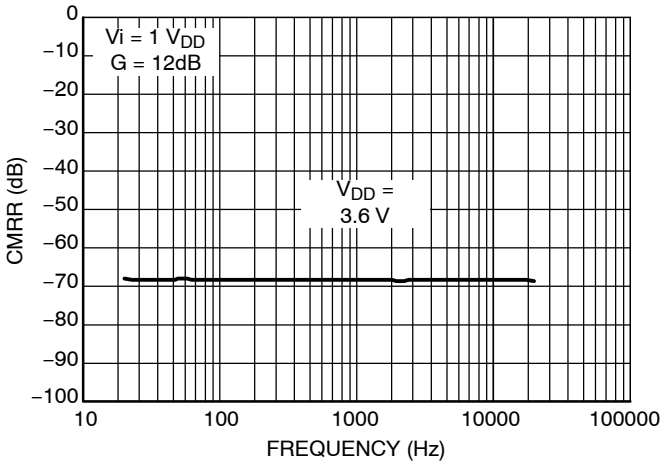


Figure 21. CMRR vs Frequency

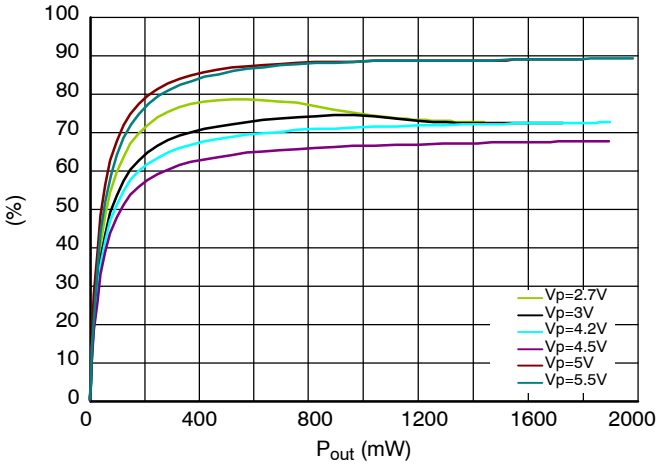


Figure 22. Global System Efficiency

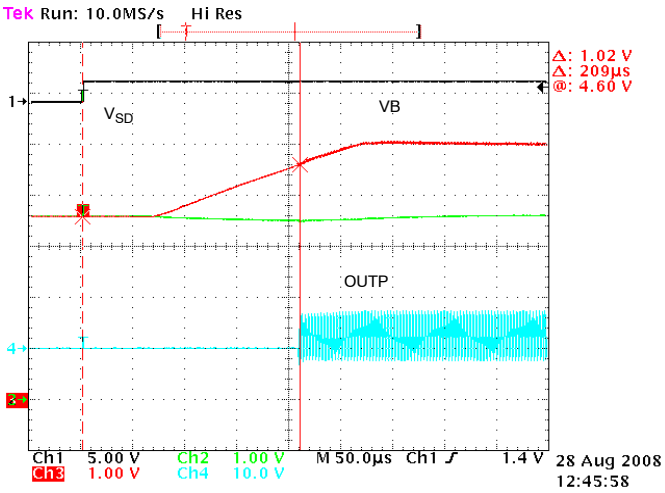


Figure 23. Turn ON Sequence

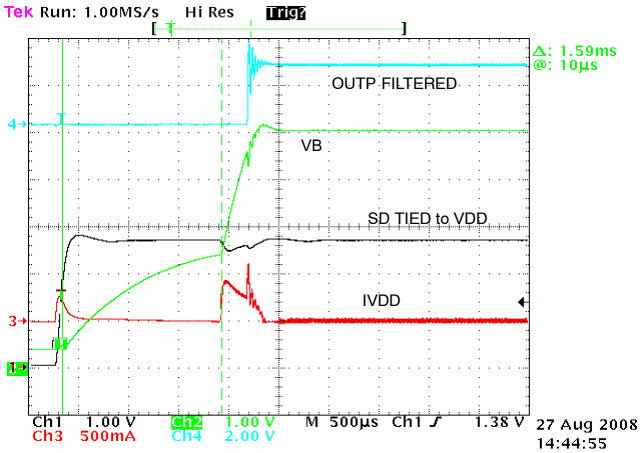


Figure 24. Turn ON Sequence

DETAIL OPERATING DESCRIPTION

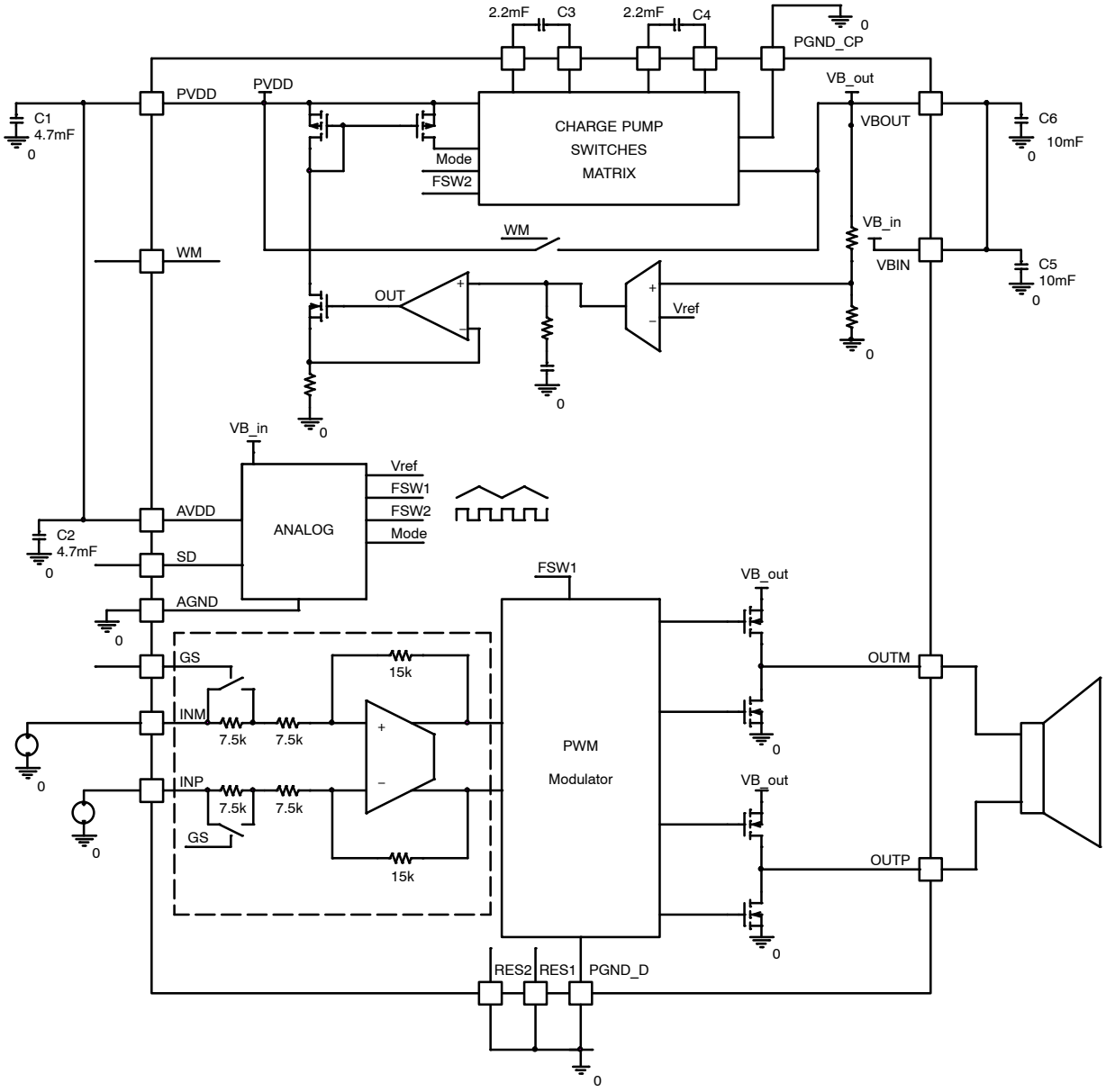


Figure 25. Functional Block Diagram

Detailed Descriptions

The NCP2830 consists of two parts: a DC−DC converter and a mono class D amplifier. These two parts are strongly matched in order to obtain the best operation of the global system.

DC−DC CONVERTER

The DC−DC converter is based on a charge pump technique. The switching frequency is synchronized with the class D amplifier (F_{SW2} = 2 x F_{SW1}) in order to avoid mixing frequency. The regulation is based on a voltage regulation. The output voltage is permanently monitored through a resistor ladder and compared to an internal reference. An error amplifier and a voltage to current conversion allow injecting in the Capacitors C3 and C4 the necessary current to maintain 5 V in output. This linear regulation reduces the output voltage ripple (7 mV typ) and allows a noise free operation.

Turn ON/OFF sequence

The turn ON and turn OFF sequence has been adapted to an audio applications environment. When the battery voltage is connected to the V_{DD} pins, the output capacitance is precharged to the V_{DD} voltage. When VSD is High, the charge pump is activated and the output voltage rises up to

5 V. Internally, the class D amplifier starts to operate when V_B equals 4.5 V.

When VSD is low, the charge pump is deactivated and the V_B voltage is maintain to the V_{DD} value. During this shutdown mode, it is not possible to sink current through the VB pin. Figure 26 depicts the turn ON/OFF sequence.

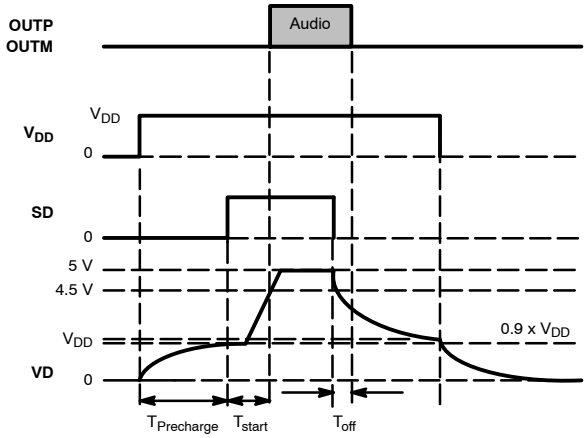


Figure 26. Turn ON/OFF Sequence

In order to maximize the global efficiency, the system permanently monitors the battery voltage and changes its operating mode:

- When V_{DD} is less than 3.8 V (typ) the system operates in **2X mode.**
- Between 3.8 V and 4.65 V the system operates in **1.5X mode.**
- If V_{DD} is greater than 4.65 V the system switches automatically to **Wire Mode** operation ($V_B = V_{DD}$)

WM pin

This external pin allows controlling the activation of the boost whatever the battery voltage is. For example, if no power is required, there is no need to boost the supply voltage of the class D amplifier. In that case, disabling the boost by a high logic on WM pin, allows supplying directly the class D by the battery voltage ($V_B = V_{DD}$) and optimizing the efficiency.

CLASS D AMPLIFIER

The NCP2830 is based on a mono class D audio amplifier. This structure is composed by a preamplifier stage, a PWM stage and a H−Bridge stage.

Gain selection

The preamplifier stage consists in applying a gain to the input signal selectable by a dedicated digital pin GS.

The gain setting is given by the following truth table:

GS	Gain Av V/V	Input Impedance kΩ
0	2	15
1	4	7.5

30 kHz Built−in Low Pass Filter

This filter allows directly connecting a DAC or a CODEC to the NCP2830 input without risk of output noise increase due to a mixing frequency with the DAC/CODEC output frequency. Consequently, the best operation with DACs or CODECs is guarantee without need of additional external components.

Input Capacitors C_{in}

Due to its fully differential architecture the NCP2830 does not require input capacitors if the differential source is biased from 0.5 V to V_{DD} − 0.8 V. However, it is possible to use input capacitors when the differential source is not biased or in single ended configuration. In this case it is necessary to take into account the corner frequency which can influence the low frequency response of the NCP2830. The following equation will help to choose the adequate input capacitors.

$$f_C = \frac{1}{2\pi \cdot Z_{in} \cdot C_{in}} \qquad \text{(eq. 1)}$$

With Z_{in} the input impedance of the NCP2830.

Overcurrent Protection

This protection allows detecting an over current in the H−Bridge. When the current is higher than 2 A the H−Bridge is put in high impedance. When the short circuit is removed or the current is lower, the NCP2830 go back to normal operation. This protection allows avoiding overcurrent due to a bad assembly (Output shorted together, to V_B or to ground).

DESIGN PROCEDURE

Components Selection

Use very low ESR ceramic capacitors (X5R/X7R) will help to reduce the output resistance of the charge pump and thus improve the system efficiency.

Input Capacitor (C1 and C2)

NCP2830 is aimed to be connected on the battery line. For such a device, it is mandatory to get as low ripple as possible so as to avoid conducted emission on the battery line. As stated above, the noise generated by turn−on and turn−off transients is optimized by a controlled switching speed.

Placing two 4.7 μF/6.3 V (0603 size) input capacitors as close as possible to PDD and AVDD pin will also help to avoid any disturbance for other sensitive parts also connected on the battery line.

Flying Capacitors (C3 and C4)

As stated above, the value of these capacitors has a direct impact on the load regulation and output resistance of the charge pump. The converter must provide a regulated DC voltage with a sine wave AC current, the frequency of which is twice the audio signal frequency. Selecting a 2.2 μF/6.3 V (0603 size) will help regarding the load regulation and the device's ability to provide sufficient current drive.

Output Capacitors (C5 and C6)

The value and ESR of this capacitor are directly linked to the ripple of the regulated output voltage. As the charge pump must provide up to 450 mA to the internal audio amplifier, two 10 μF/6.3 V capacitors (0603 size) should allow the converter to give its maximum output power capability.

Layout Recommendations

As all switching devices, special care must be observed in routing power supplies and ground.

V_{DD} pins must be decoupled by C1 and C2 placed as close as possible to the NCP2830 in order to reduce parasitic inductance.

GND pins must be connected to a ground plane. In order to reduce parasitic elements, it is better to connect all the ground pins to the same Ground plane.

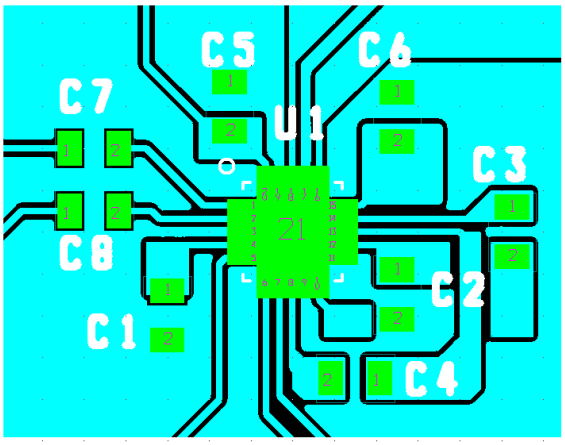


Figure 27. Recommended PCB Layout

Optional Output Filters

If the traces between the amplifier and the speaker are short, there's no need for an output filter.

In case of applications where short output traces are not possible, it is necessary to protect the application as much as possible from EMI pollution. The use of small 0603 Chip Ferrite beads is a good alternative.

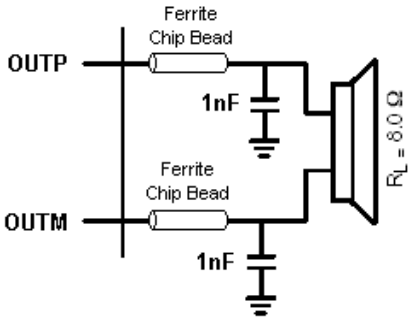


Figure 28. Optional EMI Filter

Thermal Considerations

For thermal dissipation, it is recommended to connect the exposed pad of the NCP2830 to a plan connected to the ground as depicted Figure 27.

Demo Board Available:

The NCP2830EVB/D evaluation board that configures the device in typical application.

TYPICAL APPLICATION

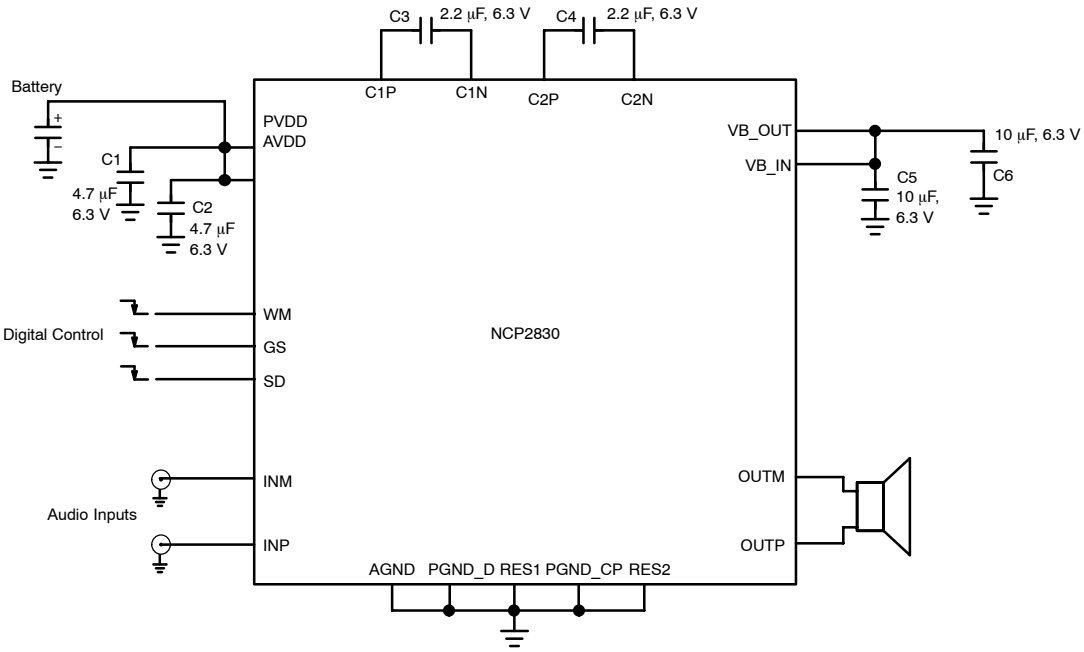


Figure 29. Fully Differential Configuration

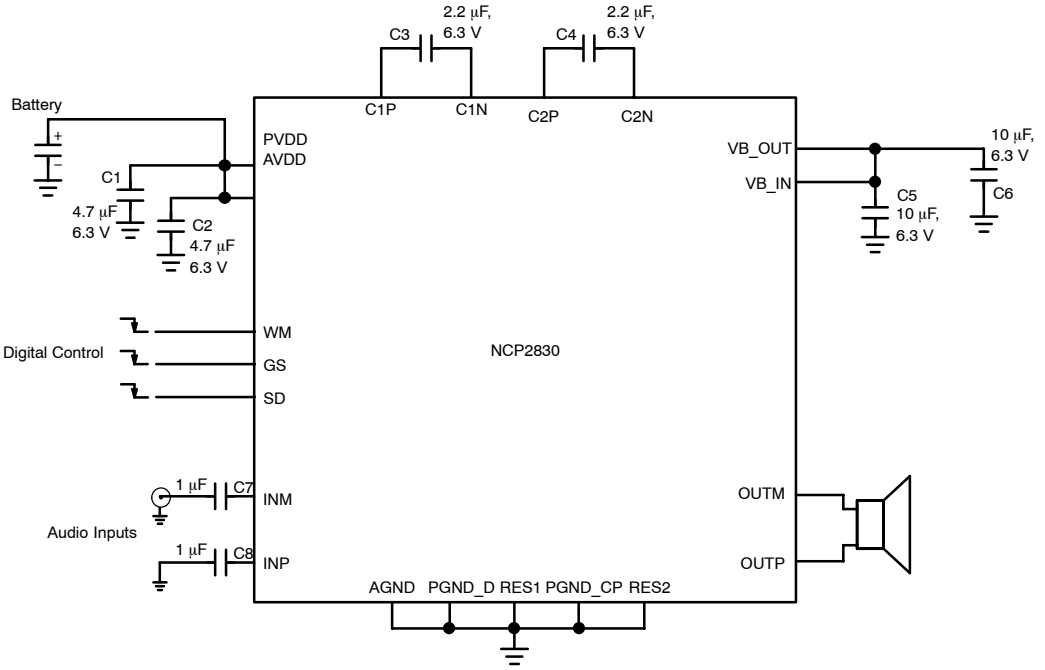


Figure 30. Single−Ended Configuration

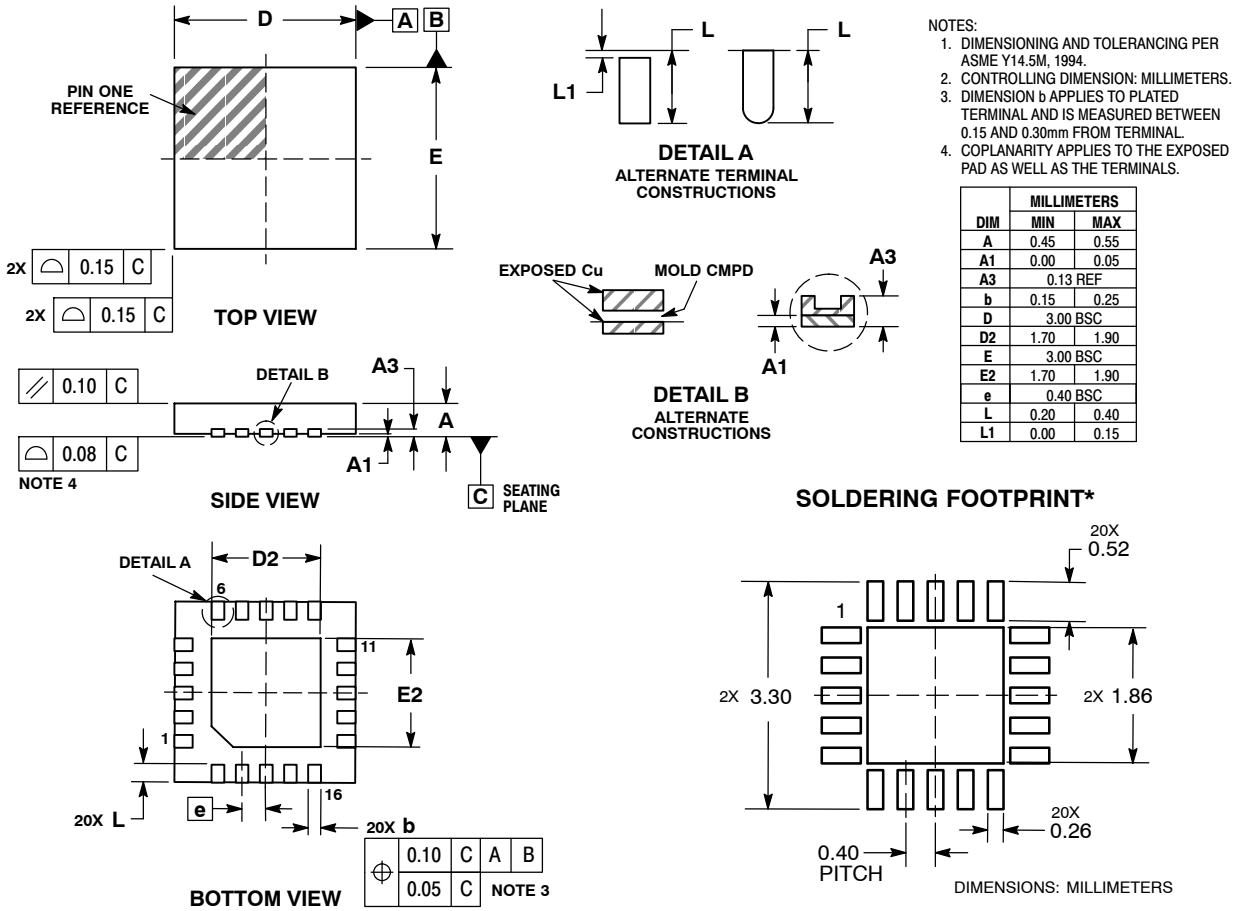
ORDERING INFORMATION

Device	Package	Shipping†
NCP2830MUTXG	UQFN20 3x3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UQFN20 3x3, 0.4P
CASE 523AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.00 BSC	
D2	1.70	1.90
E	3.00 BSC	
E2	1.70	1.90
e	0.40 BSC	
L	0.20	0.40
L1	0.00	0.15

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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