NXP six-channel display 2:1 multiplexers / 1:2 demultiplexers CBTL06121/122/141

High-bandwidth (de-)multiplexers for DisplayPort and PCIe

To support the new, high-speed motherboard graphics chipsets from Intel, AMD/ATI, nVidia, and others, these devices provide configurable routing of high-speed differential signals to DisplayPort and PCIe connectors, and use a high-bandwidth, 2:1 multiplexing or 1:2 de-multiplexing topology to preserve signal integrity.

Key features

- 2:1 multiplexing or 1:2 de-multiplexing of DisplayPort signals up to 2.7 Gbps (CBTL06121/141)
- 2:1 multiplexing or 1:2 de-multiplexing of PCIe signals up to 2.5 Gbps (CBTL06121/141) and 5.0 Gbps (CBTL06122)
  - Four high-speed differential channels
  - One channel for HPD
  - One channel for AUX differential signals or DDC clock and data
- High-bandwidth analog pass-gate technology
- Shutdown mode minimizes power consumption while switching all channels off
- Package and pinout options to support different motherboard configurations
- HWQFN56 and TFBGA48 packages

Applications

- DisplayPort and PCIe switching or multiplexing in desktop, notebook, and workstation motherboards
- Docking stations
- External, multipurpose dongles

NXP offers three high-bandwidth display multiplexers, the CBTL06121, the CBTL06141, and the CBTL06122, that route high-speed DisplayPort and PCIe signals to one of two external connectors. The switch position is controlled by a single digital input pin.

The CBTL06121 is a six-channel display multiplexer with a 2:1 multiplexing or 1:2 de-multiplexing topology. The CBTL06122 is a higher-bandwidth version of the CBTL06121. The CBTL06141 is a six-channel display multiplexer with an extended 4:1 multiplexing or 1:4 de-multiplexing topology for DDC/AUX.

The CBTL06121 and the CBTL06122 have four differential channels that use high-bandwidth pass-gate technology to switch or multiplex bidirectional or AC-coupled PCIe or DisplayPort signals. Two additional channels switch, multiplex, or demultiplex the Hot Plug Detect signals and the AUX or DDC signals.

NXP founded by Philips

The CBTL06121 is designed for first-generation (Gen1) speeds of 2.5 Gbps for PCIe and up to 2.7 Gbps for DisplayPort. The CBTL06122 is the same as the CBTL06121, but supports the higher, second-generation (Gen 2) PCIe speed of up to 5.0 Gbps.

To suit different motherboard layout requirements, the CTBL06121 and the CTBL06122 are available in two different pinout versions (A and B), orderable as separate part numbers.

The CBTL06141 is a Gen1 device like the CBTL06121, but the four channels it uses for DisplayPort and PCIe signals are capable of 1:2 switching and 2:1 multiplexing. Its AUX and DDC channels provide a four-position multiplexer and offer an additional level of (de-)multiplexing when, for example, the display source uses separate pins for the AUX and DDC I/O.

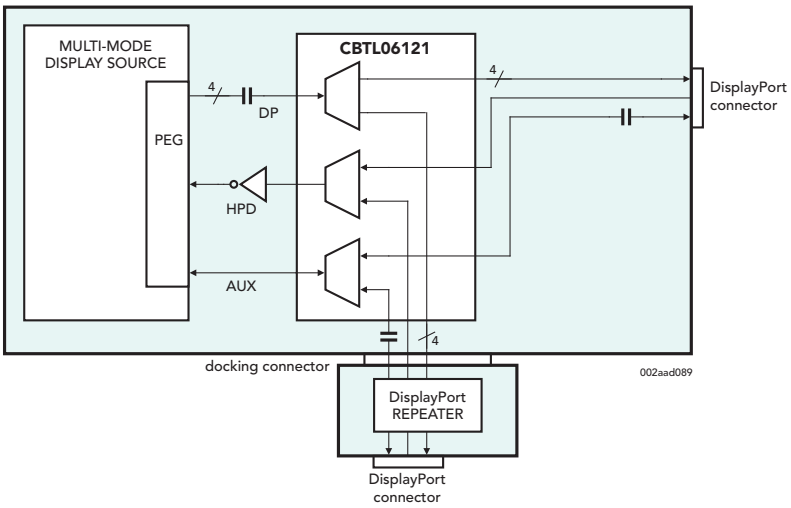
For all the (de-)multiplexers, the controller chip selects which path to use by setting a latchable select signal HIGH or LOW. When used with an HDMI/DVI level shifter device (NXP part numbers PTN3300 or PTN3301), the (de-)multiplexers also support HDMI/DVI connectivity.

All path delays are matched, for very low skew between differential channels. The intra-pair differential skew is less than 5 ps, and the inter-pair skew is less than 180 ps.

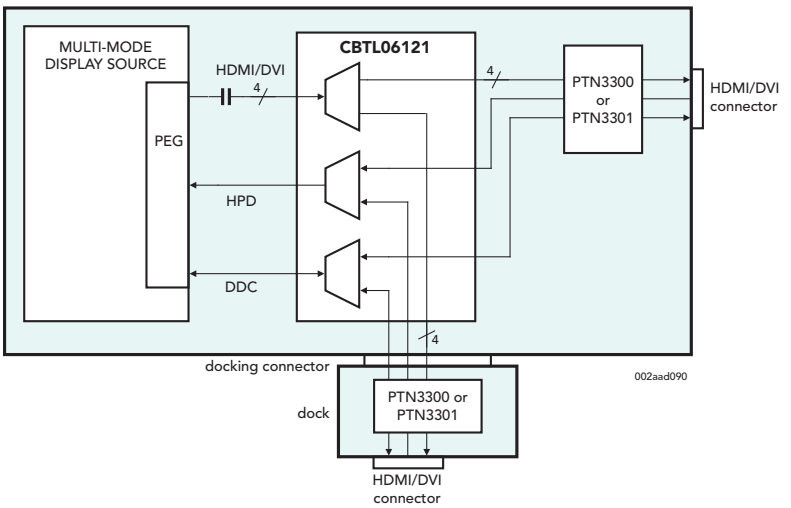
All three devices support input voltages up to 3.3 V (typical) and have an ESD resilience to 4 kV HBM and 1 kV CDM. A CMOS input for shutdown mode minimizes power consumption by switching all channels off. The operating current is only 1 mA (typical), and the shutdown current is less than 10 µA.

The CBTL06121 and the CBTL06122 are available in a 56-pin HWQFN package that measures 11 x 5 x 0.7 mm. The CBTL06141 is available in a 48-pin TFBGA package that measures only 5 x 5 x 0.8 mm.

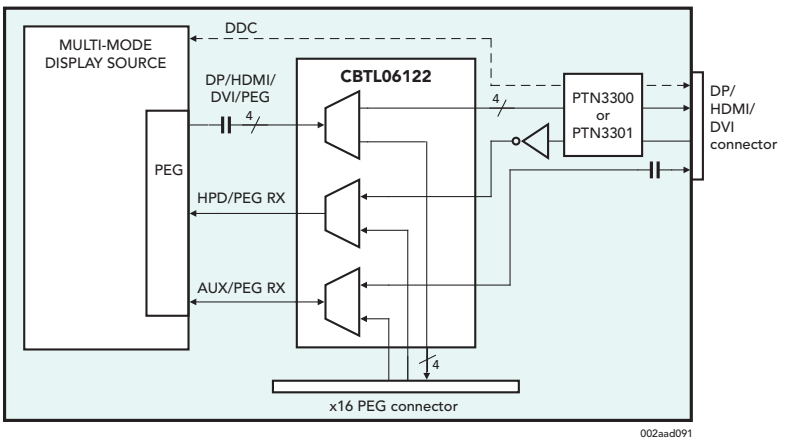
For more information visit
www.nxp.com/displayport



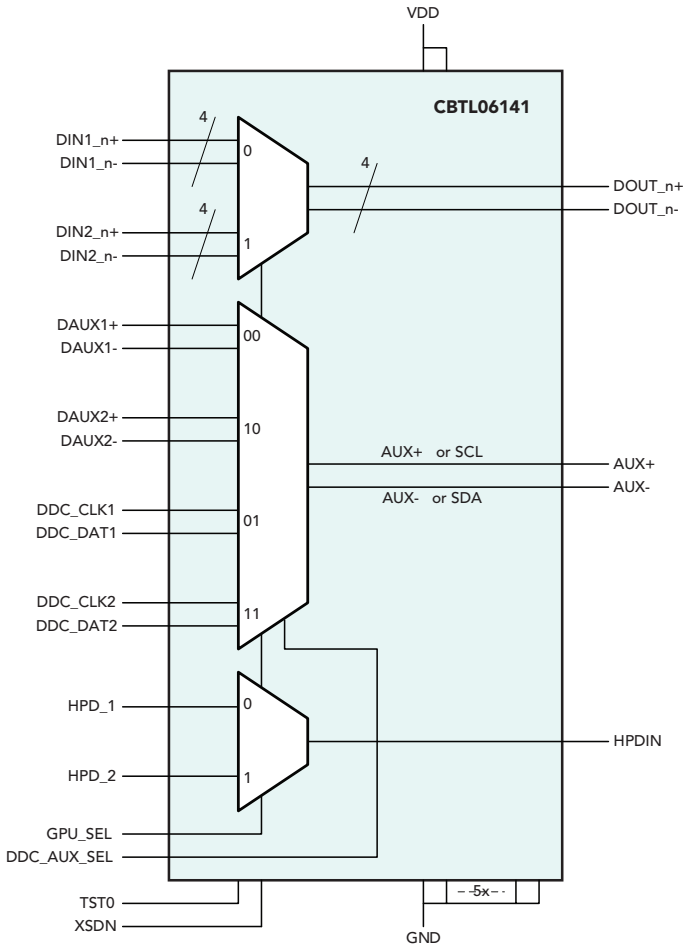
DisplayPort docking solution for mobile platform



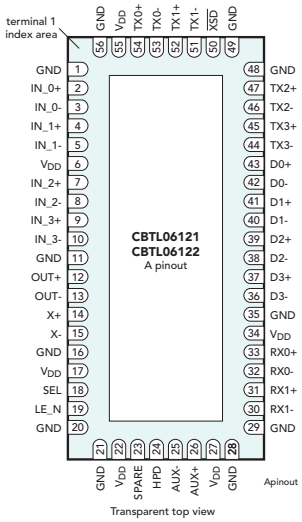
HDMI/DVI docking solution for mobile platform

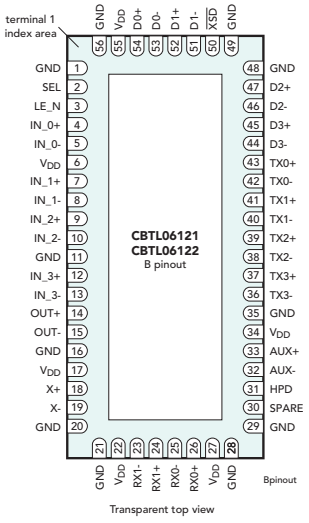


CBTL06122 used in a desktop platform for digital display and Gen2 PCI external graphics



CBTL06141 block diagram





	1	2	3	4	5	6	7	8	9
A	GPU_SEL	V_{DD}		DIN1_0-	DIN1_1-	DIN1_2-		DIN1_3+	DIN1_3-
B	DOUT_0-	DOUT_0+	GND	DIN1_0+	DIN1_1+	DIN1_2+	$\overline{XSD}$	DIN2_0+	DIN2_0-
C		DDC_AUX_SEL						GND	
D	DOUT_1-	DOUT_1+						DIN2_1+	DIN2_1-
E	DOUT_2-	DOUT_2+						DIN2_2+	DIN2_2-
F	DOUT_3-	DOUT_3+						DIN2_3+	DIN2_3-
G		TST0						GND	
H	AUX-	AUX+	HPD_2	GND	DDC_CLK2	DAUX2+	GND	DDC_CLK1	DAUX1+
J	HPDIN	HPD_1		V_{DD}	DDC_DAT2	DAUX2-		DDC_DAT1	DAUX1-

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CBTL06121 and CBTL06122 pinning diagrams and ball mapping

CBTL061xx selection guide

Feature	CBTL06121	CBTL06122	CBTL06141
Channel topology	6x differential	6x differential	6x differential
Topology of main channel multiplexer	4 x 1:2	4 x 1:2	4 x 1:2
Topology of HPD channel multiplexer	1 x 1:2	1 x 1:2	1 x 1:2
Topology of DDC / AUX channel multiplexer	1 x 1:2	1 x 1:2	1 x 1:4
PCIe / DisplayPort specification	Gen 1 Up to 2.7 Gbps	Gen 2 Up to 5 Gbps	Gen 1 Up to 2.7 Gbps
Shutdown mode	•	•	•
Package type	HWQFN56	HWQFN56	TFBGA48
Supply voltage	3.3 V	3.3 V	3.3 V

Ordering information

Type number	Package type	Dimensions	Version
CBTL06121AHF	HWQFN56	11 x 5 x 0.7 mm	SOT1033-1
CBTL06121BHF	HWQFN56	11 x 5 x 0.7 mm	SOT1033-1
CBTL06122AHF	HWQFN56	11 x 5 x 0.7 mm	SOT1033-1
CBTL06122BHF	HWQFN56	11 x 5 x 0.7 mm	SOT1033-1
CBTL06141EE	TFBGA48	5 x 5 x 0.8 mm	SOT918-1

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