LTC4266
IEEE 802.3at PoE
Quad PSE Controller

DESCRIPTION

Demonstration circuit DC1366B features the LTC®4266, a quad network power controller with I²C® interface, designed for use in IEEE 802.3at compliant Power Sourcing Equipment (PSE). Integrated into a tiny 5mm × 7mm 38-pin QFN package are four independent channels controlling external N-channel power MOSFETs. Each port features:

- Reliable 4-Point PD Detection
- Selectable 1 or 2-Event Classification
- Inrush Current Limiting
- Extremely Fast Short-Circuit Protection with Programmable Foldback Current Threshold
- Programmable Cutoff Current Threshold for Class Power Enforcement
- Voltage and Current Readback
- DC Disconnect Sensing

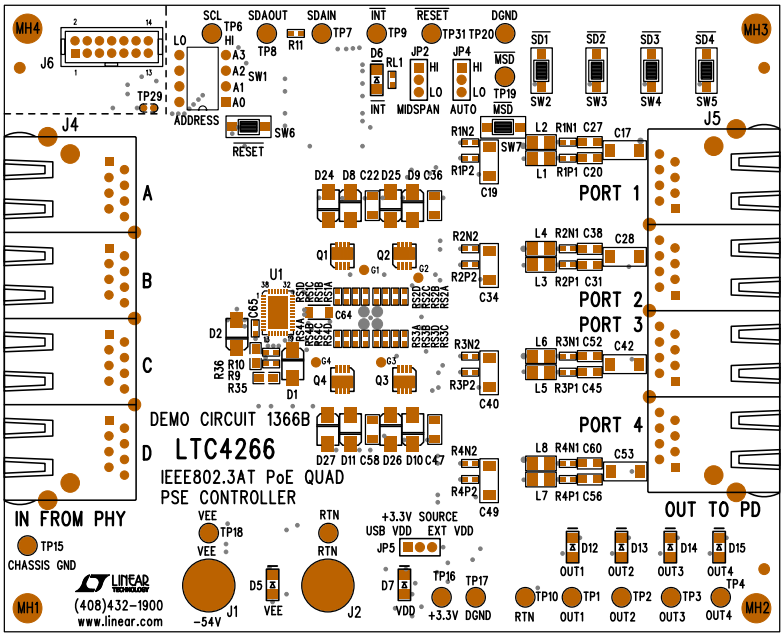
The DC1366B is configured like a midspan PSE with two RJ45 connectors for each port such that gigabit Ethernet data can pass through the board at full line rates while DC power is injected by the LTC4266 on the OUT TO PD side of the board.

Often one of the most challenging aspects of designing a PSE system is the power management software; Linear Technology makes the job easier with the fully-featured LTC4266 register set and a QuikEval™ GUI software application. The GUI allows the user full and easy access to the LTC4266 register set with detailed contextual help info.

LTC4266 example software is available only under a non-disclosure agreement (NDA).

The DC1366B has increased surge protection and more compact Hot Swap MOSFETs over the DC1366A.

Design files for this circuit board are available at http://www.linear.com/demo/DC1366B



DC1366B

QUICK START PROCEDURE

Figure 1 shows the basic setup. The LTC4266 requires two power supply rails: V_{DD} (nominally 3.3V) and V_{EE} (nominally –54V). The V_{DD} supply can be provided by a DC590 board or an external bench supply.

When running QuikEval on a Windows computer, the DC590 is used to interface a USB port on the PC to the I^2C bus on the DC1366B. The DC590 also provides opto-isolation of the I^2C bus, and an isolated 3.3V supply to run the LTC4266; the user need only provide the V_{EE} supply.

Alternatively, the user can omit the DC590 and connect an I^2C master device to the DC1366B. If the DC590 is omitted then a bench power supply must provide V_{DD}.

For applications where I^2C control is not required, the LTC4266 features an AUTO mode allowing it to operate completely autonomously.

Choose one of the setup procedures shown on the next page, depending on whether or not the QuikEval GUI application software is required.

Setup Procedure to Run the QuikEval GUI Software

1. Install the GUI software on the PC according to the instructions in the README.txt file included with the GUI software.
2. On the DC590:
   a. Set both sides (ISO and SW) of JP5 to ON.
   b. Set JP6 to 3.3V.
3. Connect the DC590 to the PC with a standard USB A-B cable.
   a. Verify the computer recognized the USB device. (The first time the DC590 is connected the Hardware Wizard may ask for help to locate the driver. Direct it to the location specified in the README.txt that came with the GUI software.)
   b. Verify the ISO PWR LED on the DC590 is lit.
4. On the DC1366B board:
   a. Set JP5 to the USB V_{DD} position.
   b. Set JP3 to the TIE position.
   c. Set JP4 (AUTO) to the HI position.
   d. If midspan operation is desired set JP2 to HI, for endpoint set to LO.
5. Connect the DC590 to the DC1366B with the 14-conductor ribbon cable supplied with the DC1366B. Verify the V_{DD} LED on the DC1366B is lit.
6. Before connecting the main power supply to the DC1366B verify the voltage is between 51V and 57V, and that the main supply is turned off.
7. Connect the main power supply to the DC1366B with two banana patch cords as shown in Figure 1. **Verify the polarity is correct before turning on the power; positive goes to RTN and negative to V_{EE}.**
8. Turn on the main power supply and verify the V_{EE} LED on the DC1366B is lit.
9. Connect PDs to any of the ports on the OUT to PD side of the DC1366B and verify they turn on by the respective OUTn LED.
10. Launch QuikEval.

QUICK START PROCEDURE

Setup Procedure without the DC590

1. On the DC1366B:
   a. Set JP5 to EXT V_{DD}.
   b. Set JP4 (AUTO) to the HI position.
   c. If midspan operation is desired set JP2 to HI, for endpoint set to LO.
2. Connect a 3.3V power supply across +3.3V and DGND test points as shown in Figure 1. Turn on the 3.3V supply and verify the V_{DD} LED on the DC1366B is lit.
3. Before connecting the main power supply to the DC1366B verify the voltage is between 51V and 57V, **and that the main supply is turned off.**
4. Connect the main power supply to the DC1366B with two banana patch cords as shown in Figure 1. **Verify the polarity is correct before turning on the power; positive goes to RTN and negative to V_{EE}.**
5. Turn on the main power supply and verify the V_{EE} LED on the DC1366B is lit.
6. Connect PDs to any of the ports on the OUT TO PD side of the DC1366B and verify they turn on by the respective OUTn LED.

QUICK START PROCEDURE

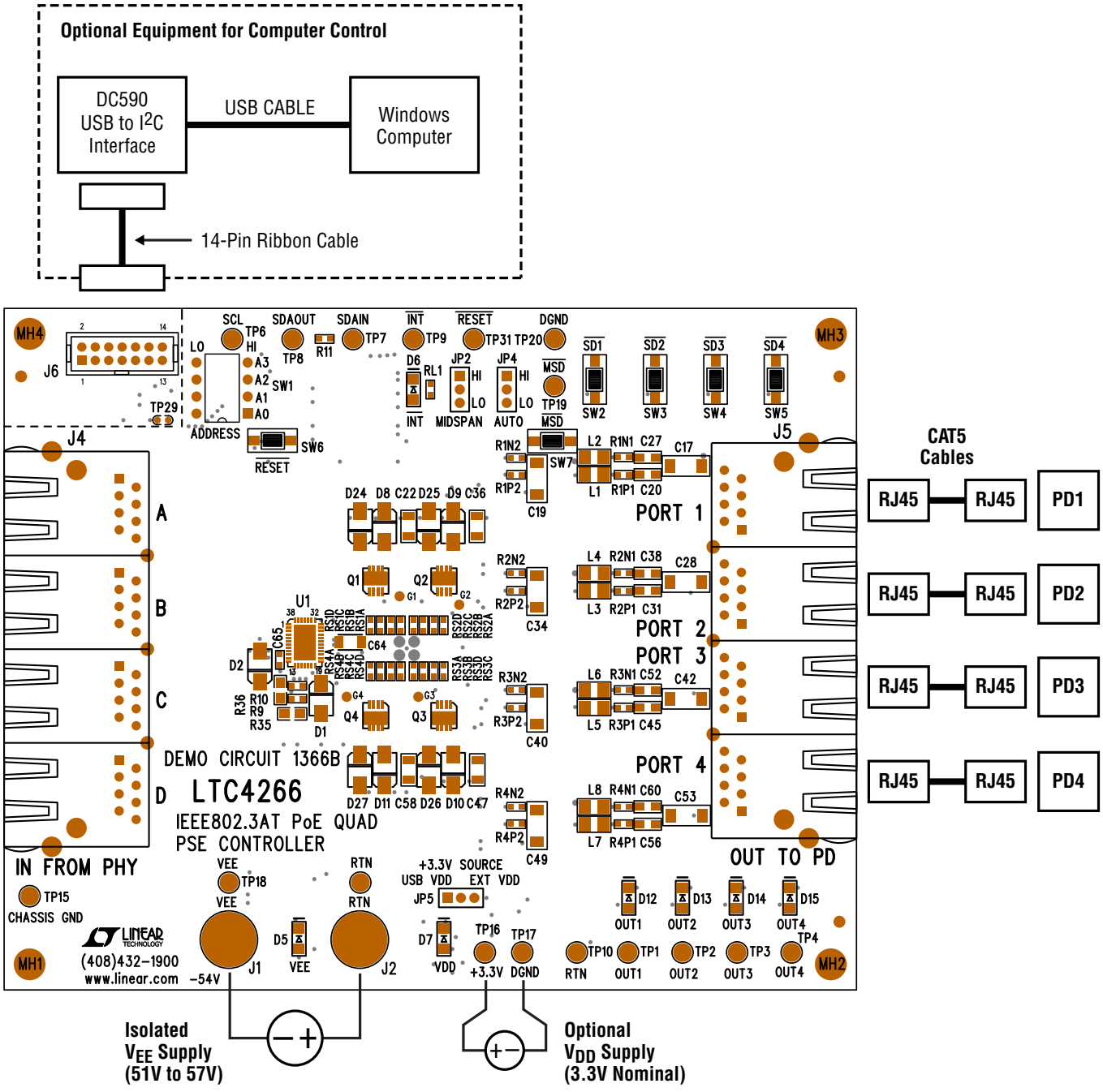


Figure 1. DC1366B Setup

OPERATION

Introduction

The DC1366B demonstrates the features and capabilities of the LTC4266, a quad controller for IEEE802.3at Power Sourcing Equipment (PSE). The DC1366B provides a quick and simple, fully compliant PSE solution requiring only a V_{EE} supply when used in conjunction with the DC590 USB-to-I^2C interface board.

Supply Voltages

The IEEE802.3at standard requires the port output voltage of a type 2 PSE to be in the range of 50V to 57V. The positive side is RTN and the negative side is V_{EE}. The V_{EE} supply voltage should be in this range for the sake of compliance; however, the LTC4266 is capable of operating with V_{EE} down to 30V, the max undervoltage lockout (UVLO) threshold.

Make sure to choose a V_{EE} supply with enough power to sustain all four ports at maximum load; if the total load is too great for the power supply its voltage may drop below the UVLO threshold, resetting the LTC4266 and shutting off all the ports. The worst case is when all four PDs are class 4: each class 4 PD may draw up to 600mA, totaling 2.4A. Therefore a V_{EE} supply rated for at least 2.6A is recommended.

The V_{DD} supply should nominally be 3.3V but the LTC4266 is capable of operating over the range of 3.0V to 4.3V. (The UVLO threshold for the V_{DD} supply is typically 2.2V.) The LTC4266 chip typically draws only 1.1mA from the V_{DD} supply; however, LEDs and other components on the DC1366B board also draw current from V_{DD}, so the total load is typically 9mA to 26mA at 3.3V depending on which LEDs are lit.

V_{DD} to DGND Configurations

The DC1366B, LTC4266 V_{DD} supply can be configured in one of two ways. The default DC1366B configuration ties the LTC4266 V_{DD} pin to the AGND pin through a 0 Ohm resistor R10. The DGND pin is at –3.3V below the AGND pin. The DC1366B can also be configured for a +3.3V at V_{DD} relative to AGND by removing R10 and installing a 0Ω resistor at R9. This ties the LTC4266 DGND pin and AGND pin.

Modes of Operation

The LTC4266 has four modes of operation:

- **Shutdown:** Ports are shutdown, detection and classification cycles are disabled.
- **Manual:** The port does not advance automatically from detection to classification, to power on. It waits for instructions from a host controller via the I^2C interface.
- **Semiauto:** The port automatically advances to classification after detecting a PD, but does not turn on power to the PD until told to do so by from a host controller via the I^2C interface.
- **AUTO Pin High:** The LTC4266 operates autonomously.

AUTO Pin

The AUTO pin determines several aspects of the LTC4266 initial behavior. AUTO is sensed by the LTC4266 at power up and after a reset.

If the AUTO pin is high then:

- All ports come up in AUTO pin high mode. Any valid PD will be turned on without software intervention.
- The current-sense resistors are assumed to be 0.25Ω (which they are on the DC1366B).
- High power is enabled. After the LTC4266 classifies a PD it applies power and automatically sets I_{CUT} and I_{LIM} appropriately for the class. With high-power enabled a class 4 PD will be able to draw up to 600mA without being cut off.

If the AUTO pin is low then:

- All ports come up in shutdown mode. A host controller must take action in order to power up any PDs.
- The current-sense resistors are assumed to be 0.50Ω; a host controller must change this to 0.25Ω for correct operation of the DC1366B.
- High power is disabled and is enabled by a host controller.

OPERATION

Endpoint vs. Midspan

The LTC4266 can be configured either for endpoint or midspan operation without software intervention by setting the MID pin high or low respectively. (You must reset the LTC4266 or cycle the power for the MID pin to be sensed.) The only difference in the behavior of the LTC4266 is that the detection back-off timer is enabled when midspan operation is selected.

Each port can be configured individually as either endspan or midspan via I^2C commands.

The DC1366B is wired for Alternative-A, MDI-X (power is injected on the data pairs of the CAT5/6e cable; positive on pins 3 and 6 of the RJ45 connector, and negative on pins 1 and 2). The original 802.3af standard required all midspans to use Alternative-B, but 802.3at allows midspans to use Alternative-A.

Disconnect Sensing

The LTC4266 employs DC disconnect sensing only. For the sake of software backward compatibility with the older LTC4259, the LTC4266 includes register bits for enabling AC disconnect sensing, but these bits simply enable the DC disconnect sensing.

Pushbutton Switches

The DC1366B includes several pushbutton switches to facilitate experimentation with the LTC4266.

- The RESET button (SW6) resets all ports just as if the power supplies were cycled.
- The Masked Shutdown (MSD) button (SW7) will turn off any ports that have their corresponding mask bit set in the MSD register.
- Each port has an individual shut down switch (SW2 through SW5 for ports 1 through 4 respectively).

Masked Shutdown

The MSD register can be used to pre-assign low-priority to selected ports so they can be shut down quickly when needed.

A PSE system design can utilize the MSD feature in various ways. For example, a PSE system may include a circuit that monitors the V_{EE} supply; if it becomes overloaded and the voltage begins to sag, the system can dump low-priority ports by asserting the $\overline{MSD}$ pin. Shedding excess load quickly may allow the V_{EE} voltage to recover before it reaches the UVLO threshold, thus avoiding shutting down higher-priority ports.

I^2C Addressing

The 7-bit I^2C address of the LTC4266 is $010A_3A_2A_1A_0b$, where A_3 through A_0 are determined by pins AD3 through AD0 respectively. On the DC1366B these pins are controlled by the quad DIP switch, SW1. The LTC4266 has internal pull-up resistors on these pins, so with all four switches of SW1 open the address will be 0101111b.

All LTC4266 chips also respond to the global address 0110000b regardless of the state of their AD3-AD0 pins.

I^2C Bus Lines

The LTC4266 has separate pins for SDAIN and SDAOUT to facilitate the use of opto-couplers. The DC1366B provides test points for both SDAIN and SDAOUT to make it easy to connect to any type of breadboard or development tools. The DC1366B ties SDAIN and SDAOUT with shunt R11.

The DC590 includes pull-up resistors on the SDA and SCL lines, while the DC1366B board has none. If the DC590 board is replaced by a different I^2C master, the user must make sure there are appropriate pull-up resistors on SDA and SCL.

Interrupts

The LTC4266 includes an open-drain interrupt line for signaling the host controller when it needs service. This signal can be accessed on the DC1366B at the $\overline{INT}$ test point. An LED is also included to indicate an interrupt.

Connecting Multiple DC1366B Boards

To use multiple DC1366B on a common I^2C bus, simply connect their J6 connectors together with ribbon cable (14-conductor, 1mm pitch).

OPERATION

Up to sixteen DC1366B can be controlled by a single I^2C master. Remember to set each board to a different I^2C address using the DIP switch.

The DC590 cannot supply enough current on V_{DD} for more than five or six DC1366B boards; an external V_{DD} power supply is recommended if more than five DC1366B boards are connected together.

If a large number of DC1366B boards are connected to a single V_{EE} supply, be aware that banana patch cords are only rated for approximately 14A. To avoid exceeding the ampacity of the patch cords, the boards should be connected in a star configuration rather than connecting the boards in a chain.

QuikEval GUI Software

The QuikEval GUI application software is a powerful tool for learning the LTC4266 registers. Also available is the LTC4266NDASI software interface data sheet that provides further details on these registers.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components are required at the main supply, at the LTC4266 supply pins and at each port.

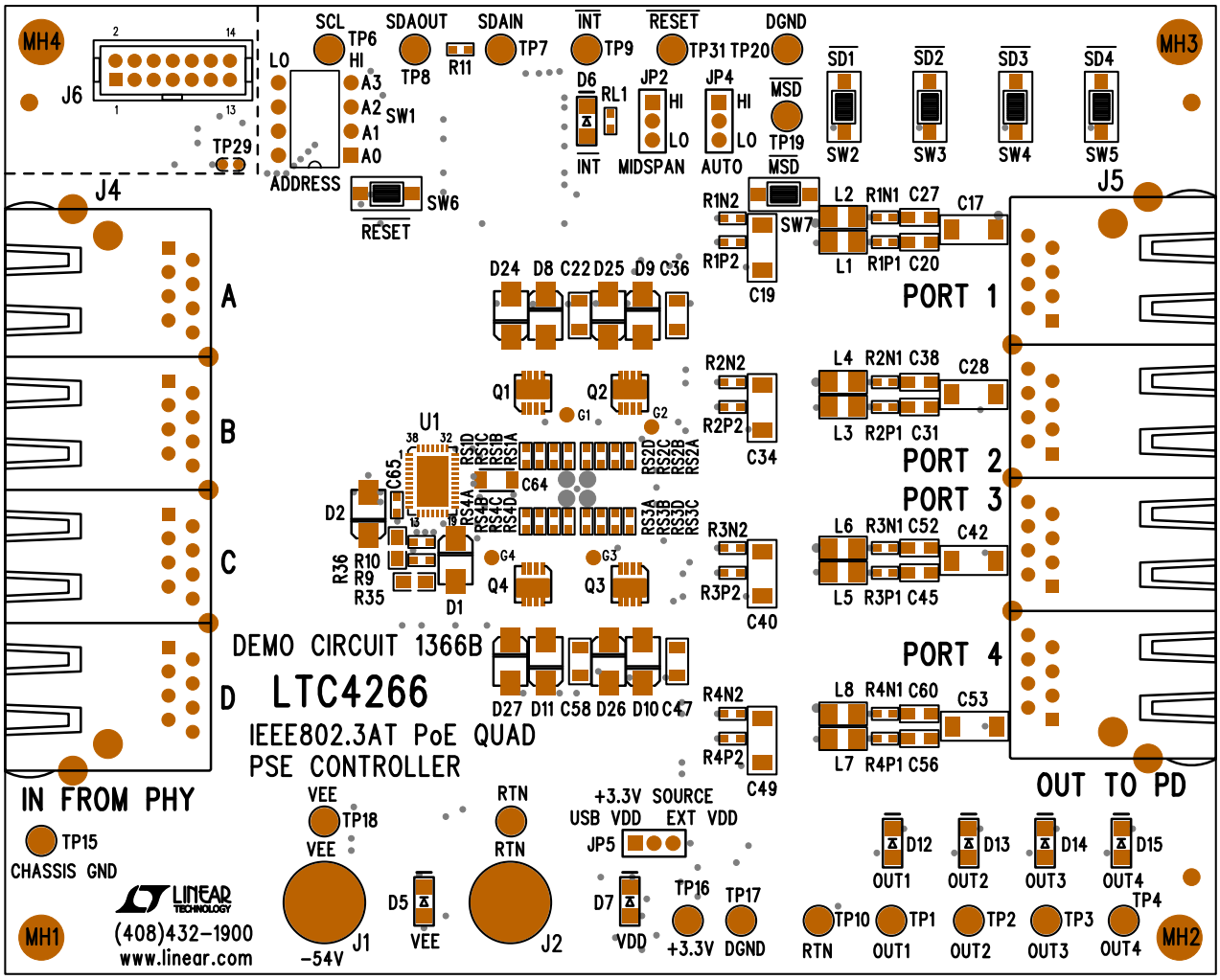
Bulk transient voltage suppression devices and bulk capacitance are required across the main PoE supply and should be sized to accommodate system level surge requirements. The DC1366B diode D18 and capacitor C2 are example components for this protection at the main PoE supply.

Each LTC4266 requires a 10Ω, 0805 resistor (R35) in series from supply AGND to the LTC4266 AGND pin. Across the LTC4266 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C64). These components must be placed close to the LTC4266 pins.

Each port requires a pair of S1B clamp diodes: one from OUTn to supply AGND and one from OUTn to supply V_{EE}. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

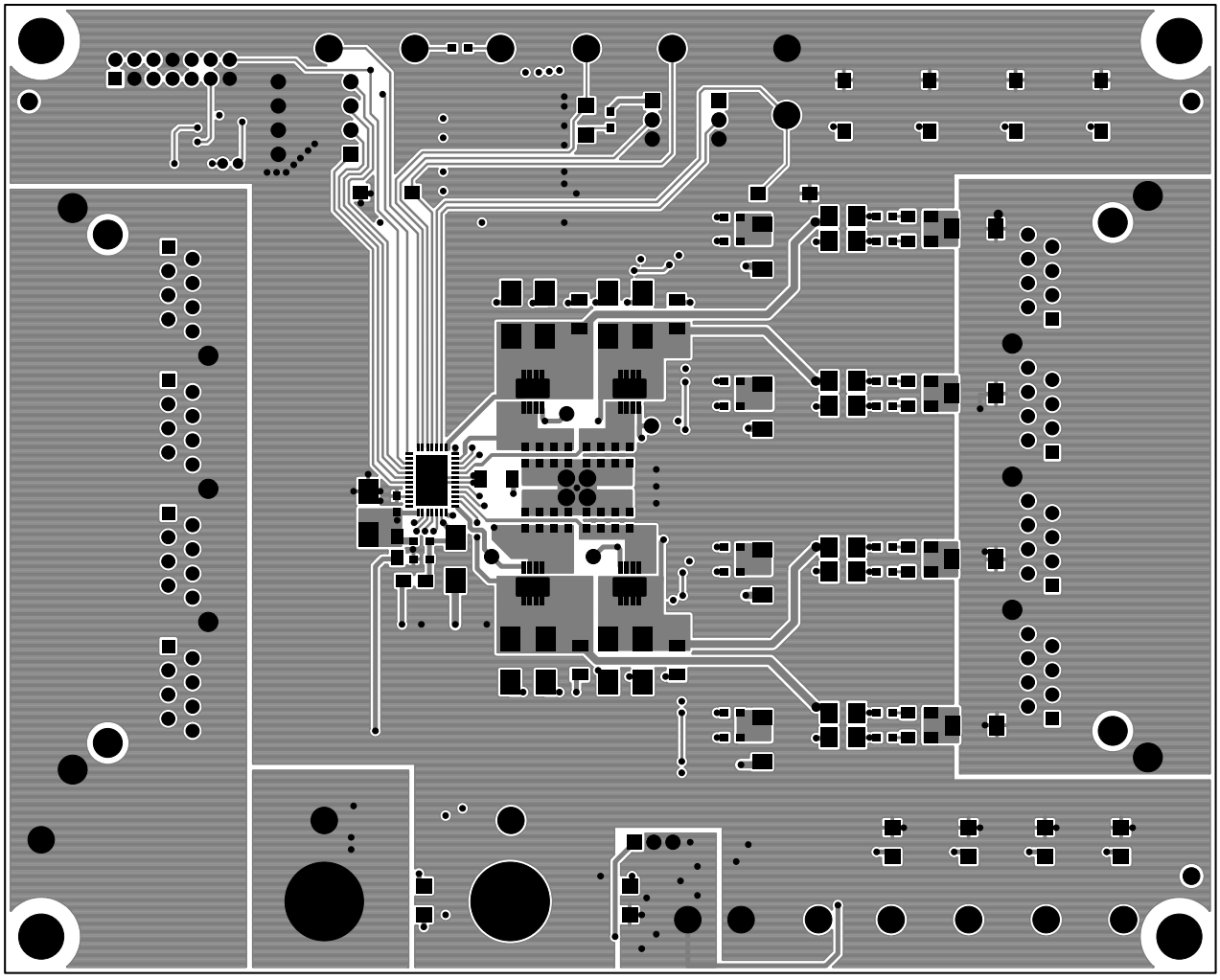
Finally, the V_{DD} logic supply and logic pins may also require additional surge protection. Components D23, C16, R36, D2, and C65 demonstrate surge protection for V_{DD} to DGND. For a positive V_{DD} configuration where V_{DD} is +3.3V above AGND and DGND is tied to AGND, the DC1366B has place holders at D28 and C66 for a 64V TVS and high voltage capacitance from V_{DD} to V_{EE}.

PCB LAYOUT



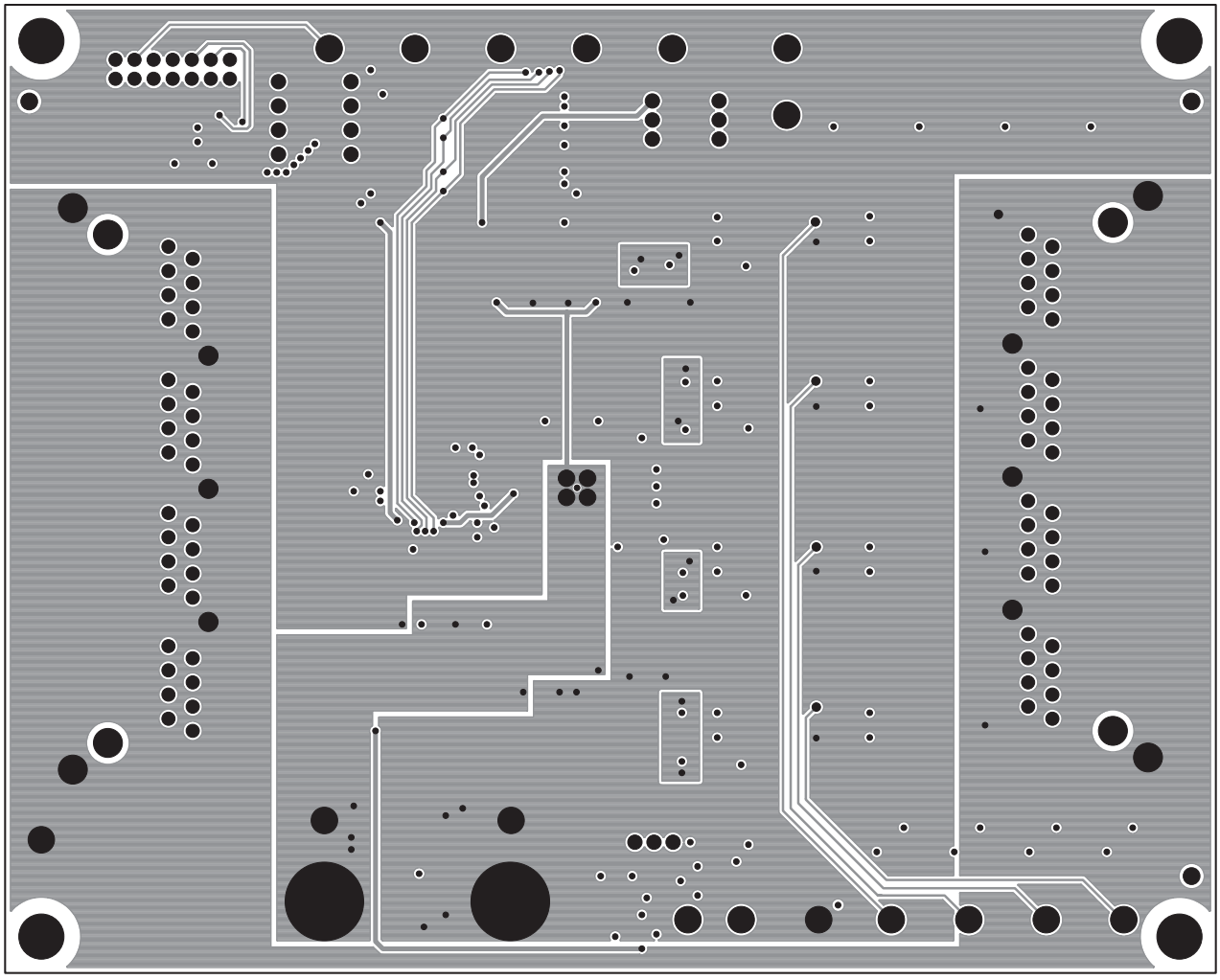
Top Assembly

PCB LAYOUT



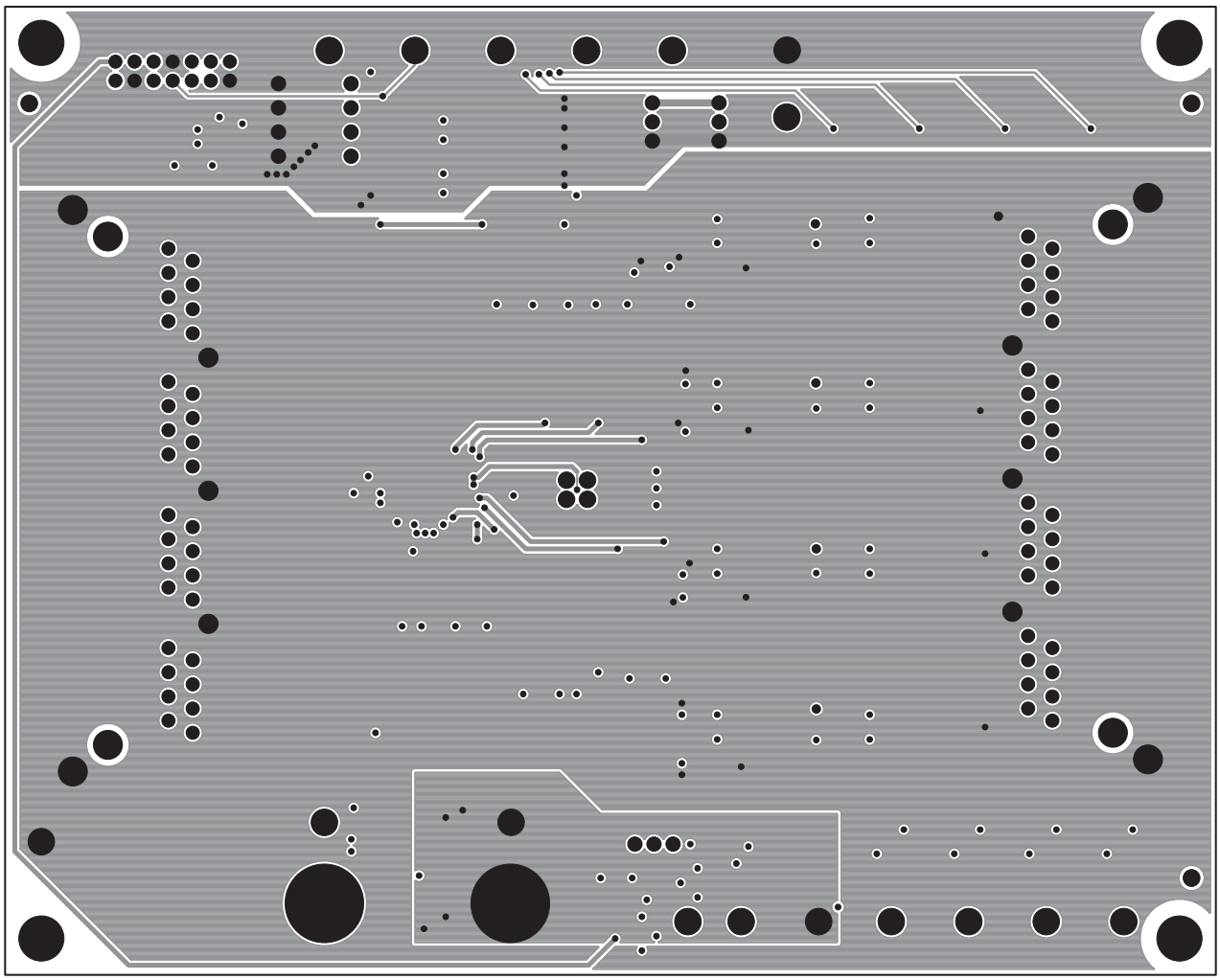
Layer 1

PCB LAYOUT



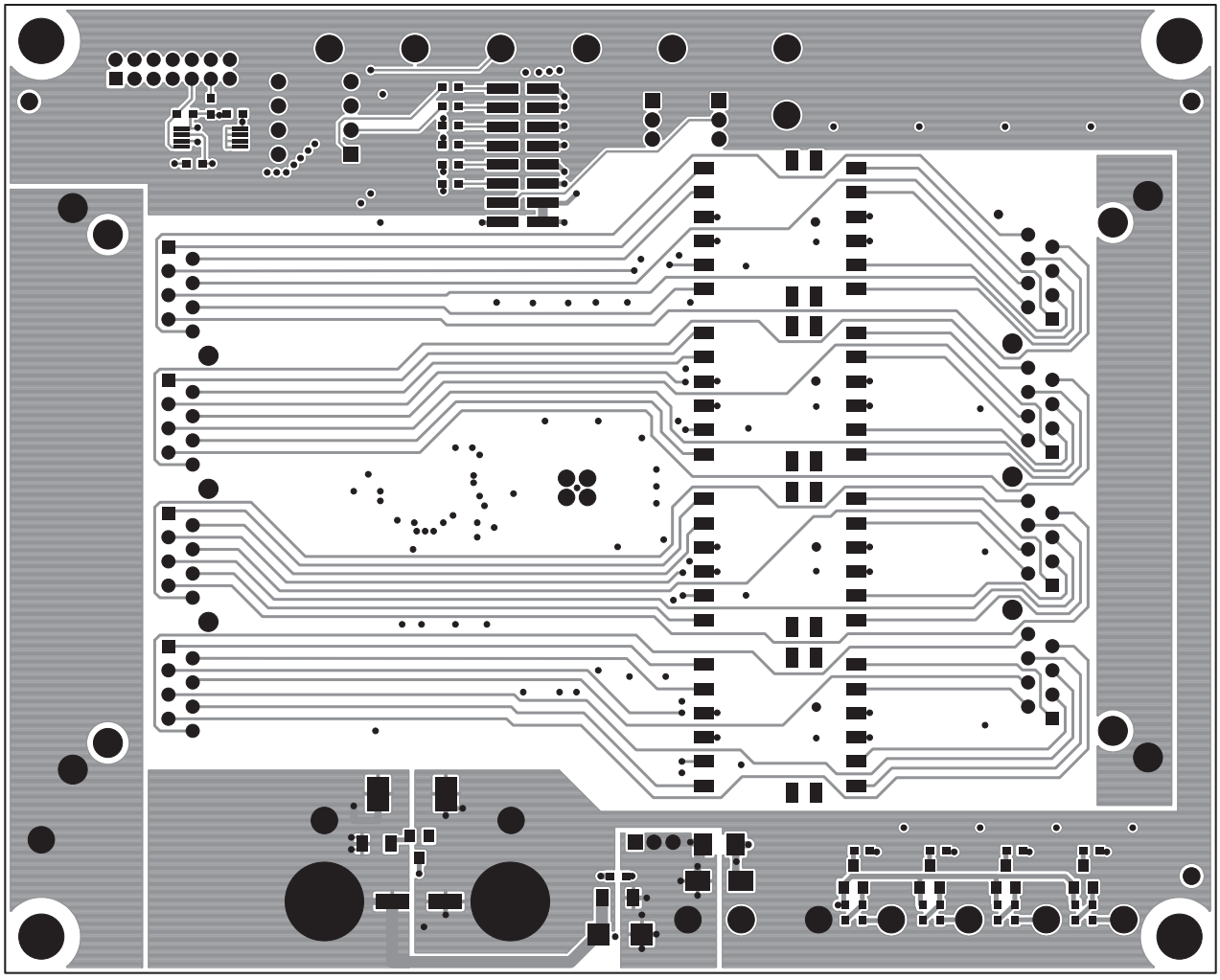
Layer 2

PCB LAYOUT



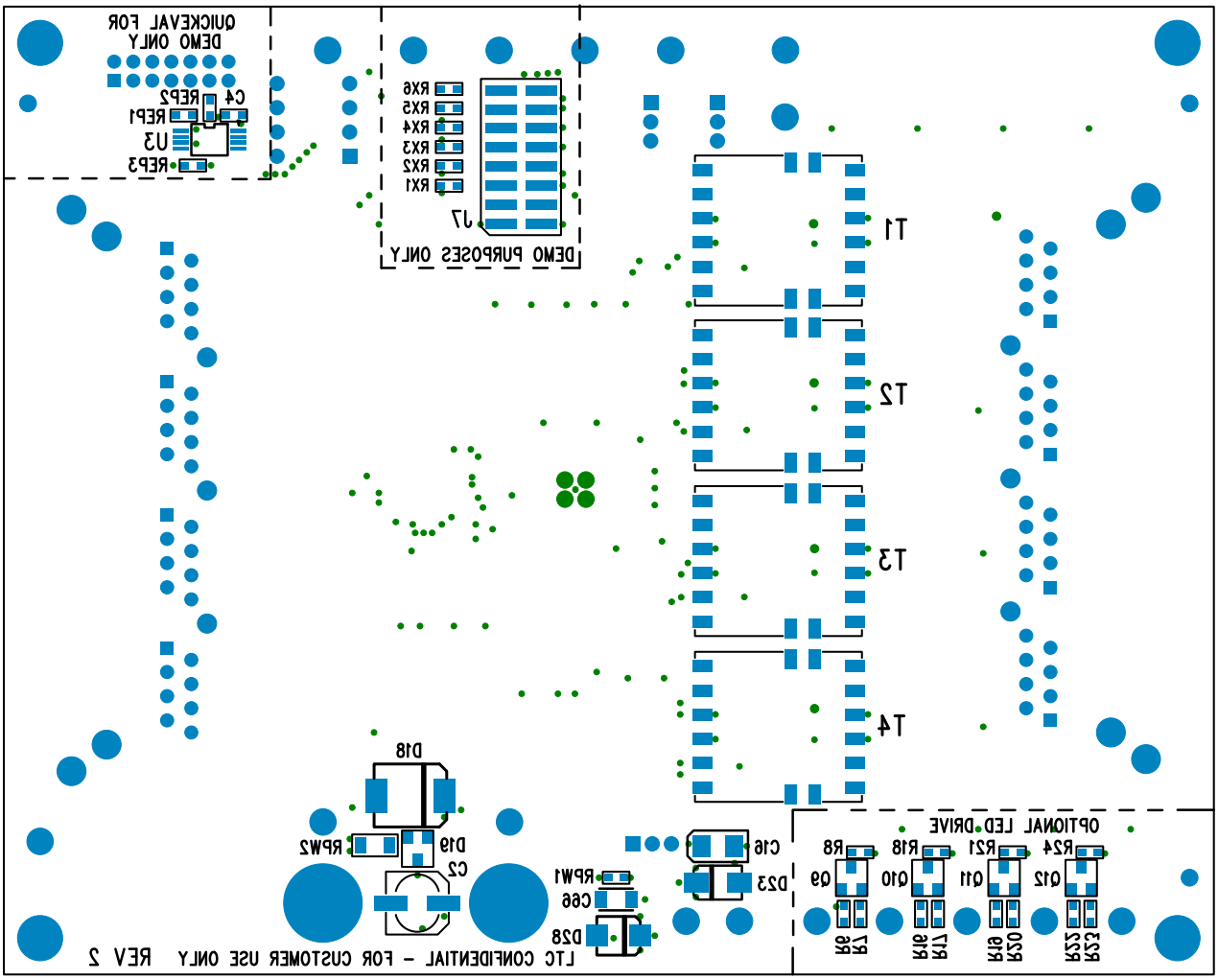
Layer 3

PCB LAYOUT



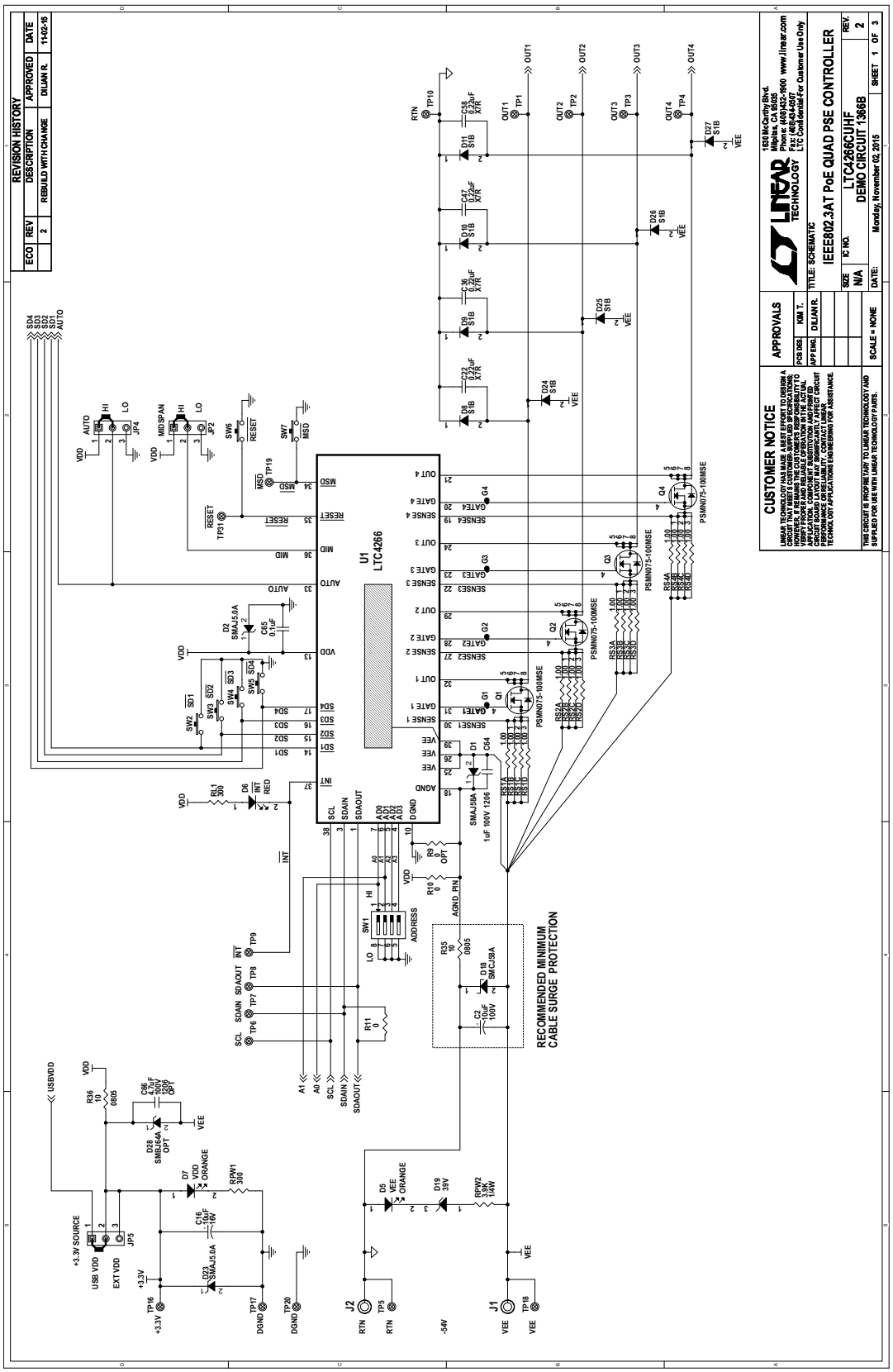
Layer 4

PCB LAYOUT

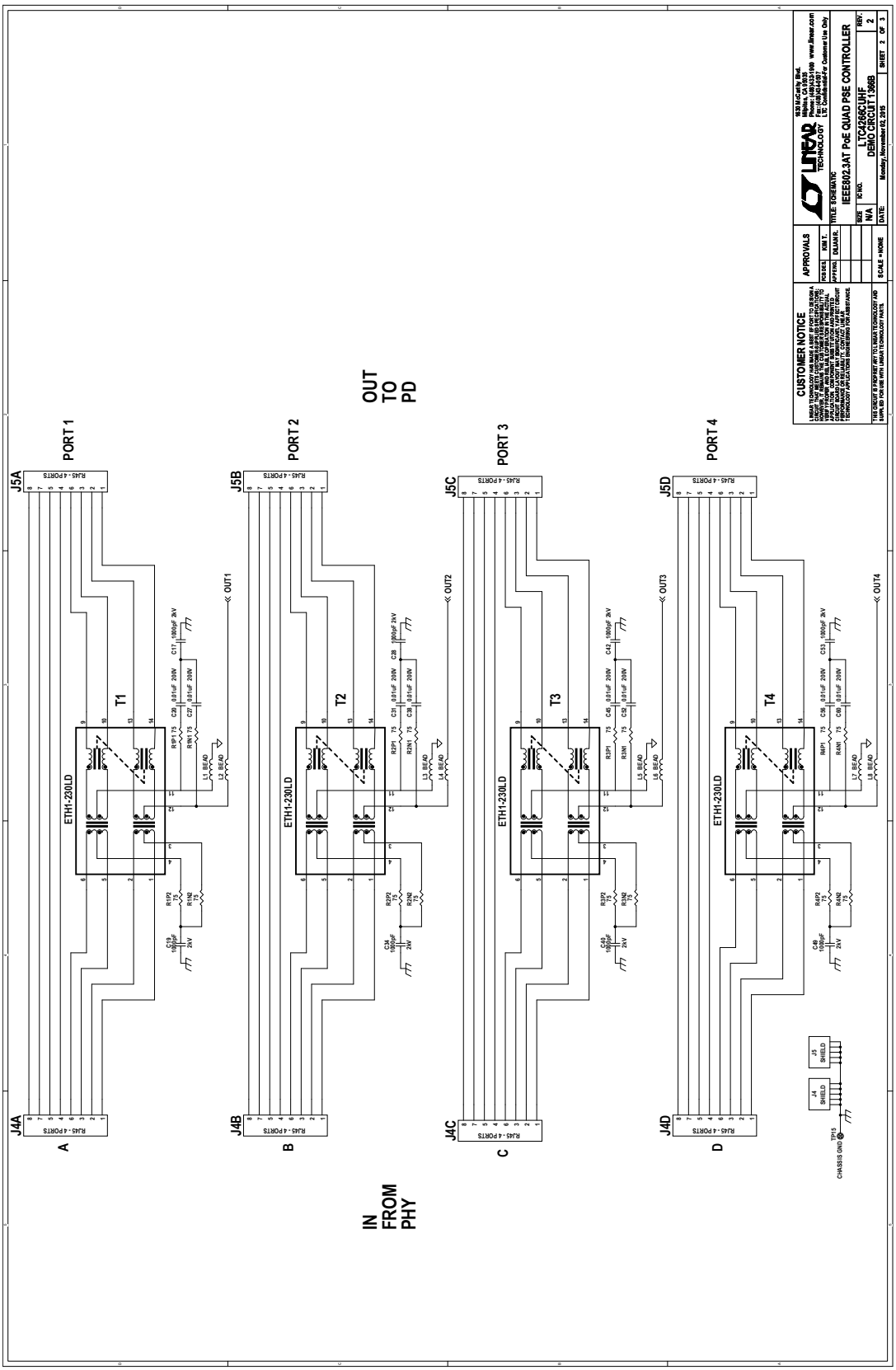


Bottom Assembly

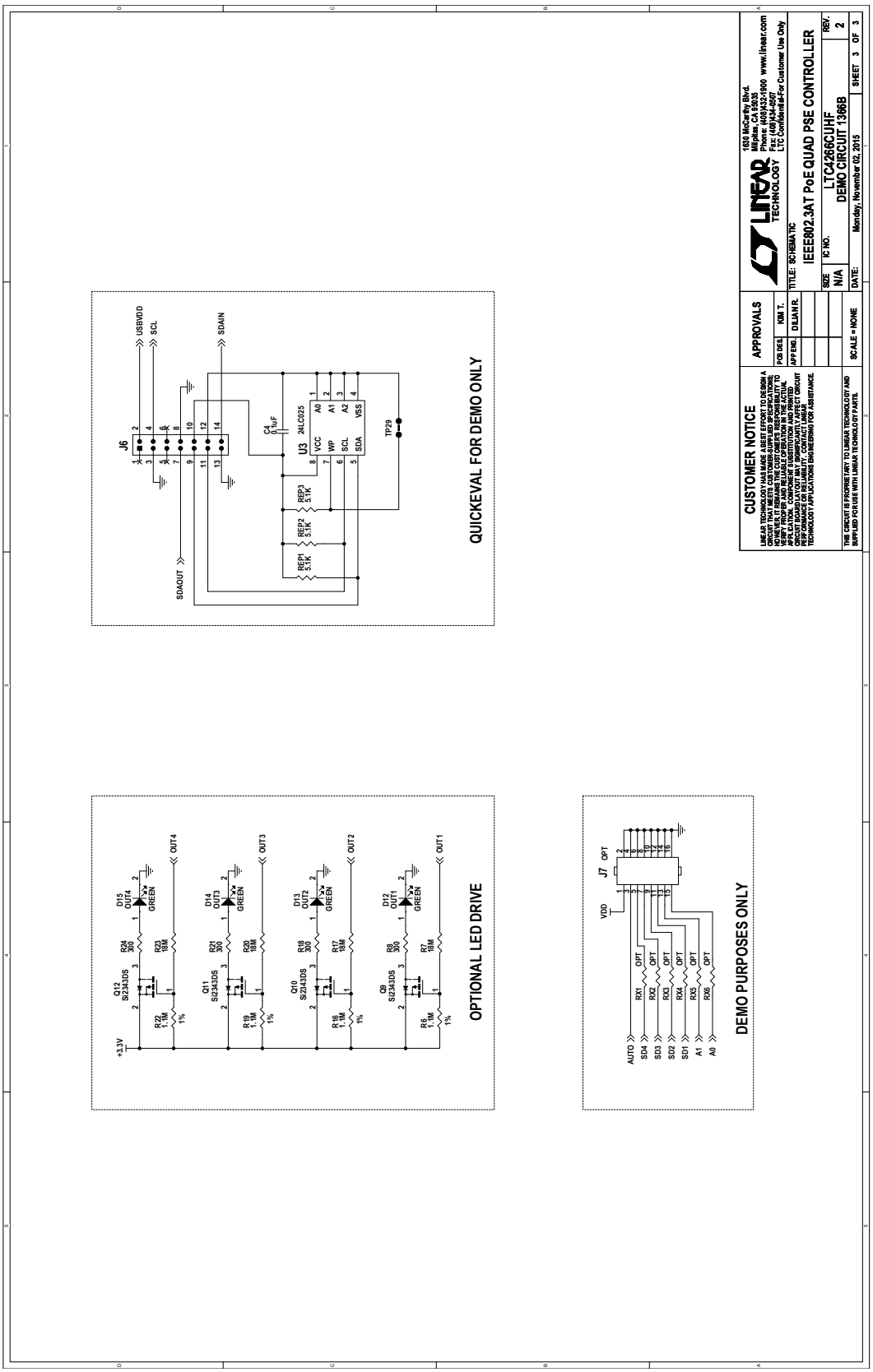
SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Replaced Q1-Q4 with NXP PSMN075-100MSE, LFPAK33 package. Replaced SDAIN/SDAOUT jumper, JP3, tie option with resistor shunt R11. Changed diode D18 to SMCJ58A, 58V TVS. Removed 3.3V LDO, U2. Added AGND pin surge protection 10Ω resistor R35, moved logic pull-ups to V_{DD} pin. Added V_{DD} pin surge protection 10Ω resistor R36. Added SMAJ5.0A, 5V TVS, D2, across LTC4266 V_{DD} and DGND pins. Changed diode D23 to SMAJ5.0A, 5V TVS. Renamed board logic ground to DGND, moved logic ground connections to DGND. Renamed V_{EE} high side supply connection to RTN. Added R10, V_{DD} pin shunt to AGND pin, and R9, DGND pin shunt option to AGND pin. Moved LED pull-up to +3.3V.	

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