STDLED625, STULED625

N-channel 620 V, 1.28 Ω typ., 5.0 A Power MOSFET in DPAK and IPAK

Datasheet – production data

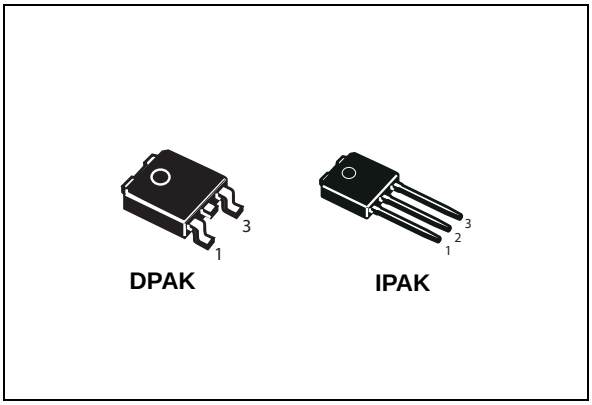
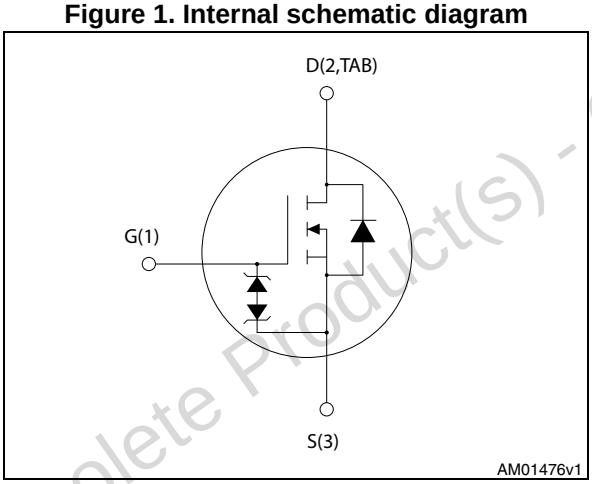


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STDLED625	620 V	1.6 Ω	5.0 A	25 W
STULED625				70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STDLED625	LED625	DPAK	Tape and reel
STULED625		IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	5.0(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.5(1)	A
I_{DM}(2)	Drain current (pulsed)	20.0(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4.2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120	mJ
dv/dt(3)	Peak diode recovery voltage slope	12	V/ns
di/dt(3)	Diode reverse recovery current slope	400	A/µs
V_{ISO}	Insulation withstand voltage (AC)		V
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq I_D$, peak $V_{DS} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		IPAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	1.79		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max.	62.50		°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max.		50	°C/W
T_J	Maximum lead temperature for soldering purpose	300		°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	620			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V; V_{DS} = 0			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.6	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.1 A		1.28	1.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	890	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance		-	18	-	pF
$C_{oss(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 480 V	-	28	-	pF
$C_{oss(tr)}$ (2)	Equivalent output capacitance time related		-	63	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 5.5 A, V_{GS} = 10 V (see *Figure 16*)	-	35	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

1. It is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. It is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 2.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	22	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	49	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
I_{SDM}(1)	Source-drain current (pulsed)				27	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 18*)	-	290		ns
Q_{rr}	Reverse recovery charge		-	1900		nC
I_{RRM}	Reverse recovery current		-	13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 18*)	-	335		ns
Q_{rr}	Reverse recovery charge		-	2400		nC
I_{RR}	Reverse recovery current		-	14.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1 mA, I_D = 0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK, IPAK

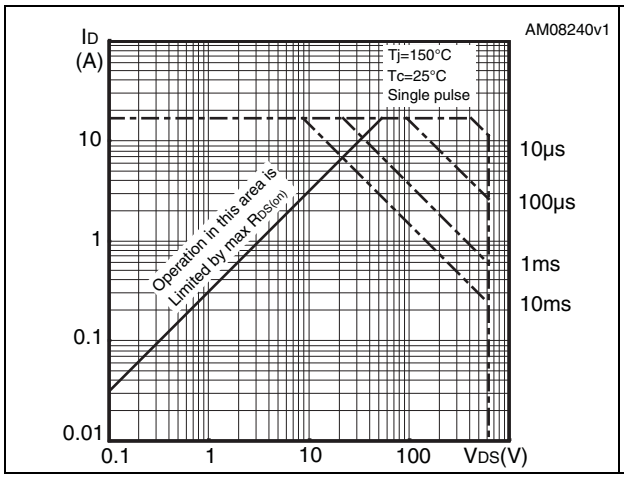


Figure 3. Thermal impedance for DPAK, IPAK

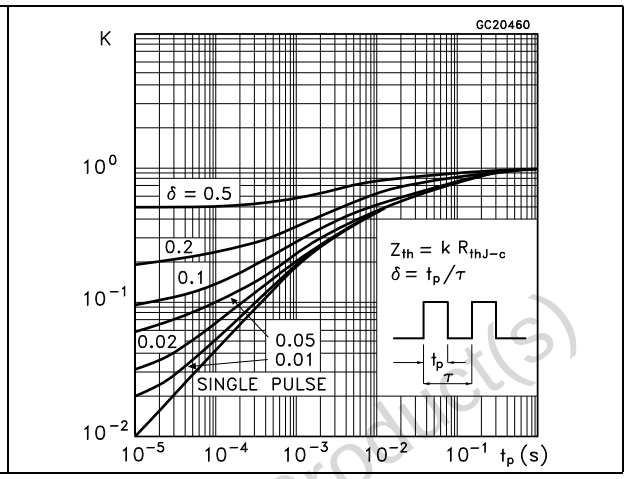


Figure 4. Output characteristics

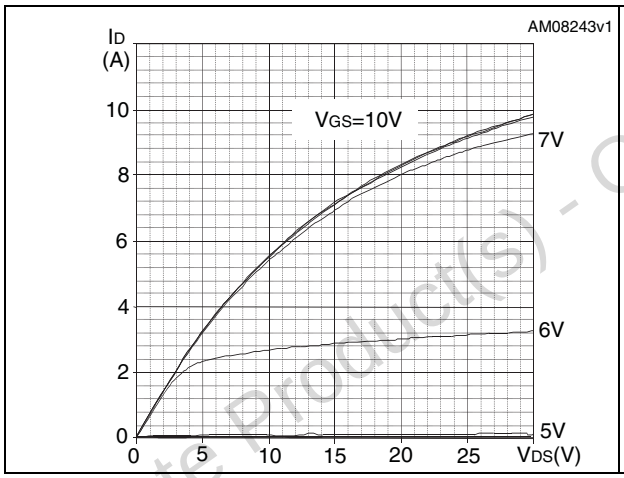


Figure 5. Transfer characteristics

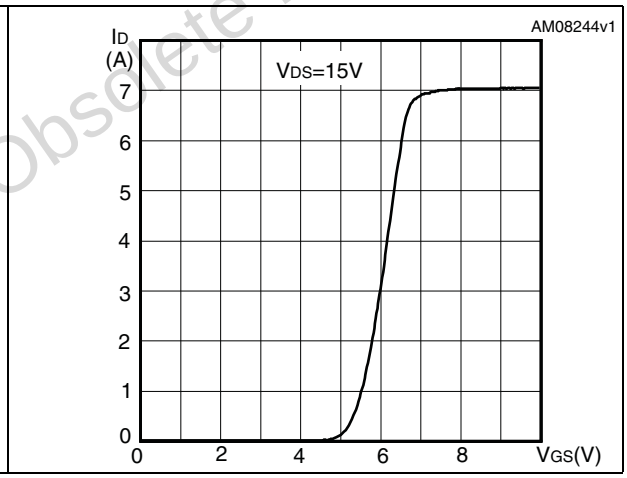


Figure 6. Gate charge vs gate-source voltage

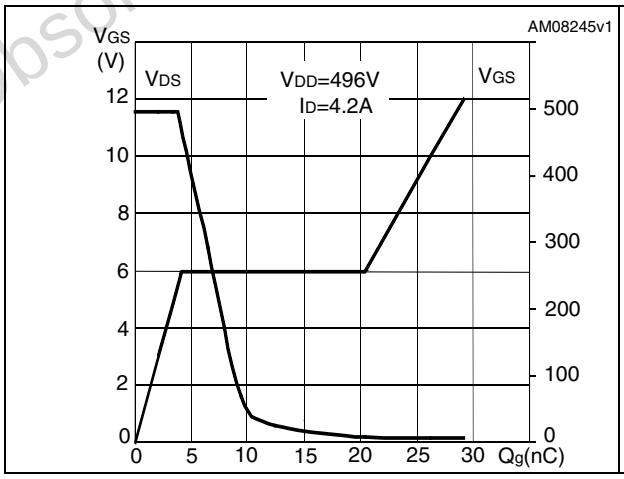


Figure 7. Static drain-source on-resistance

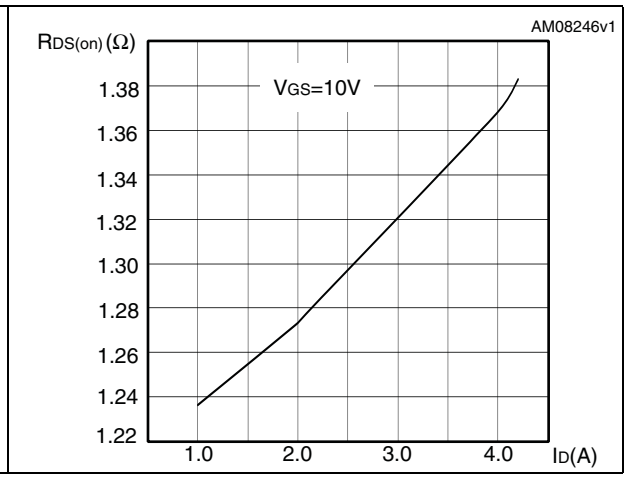


Figure 8. Capacitance variations

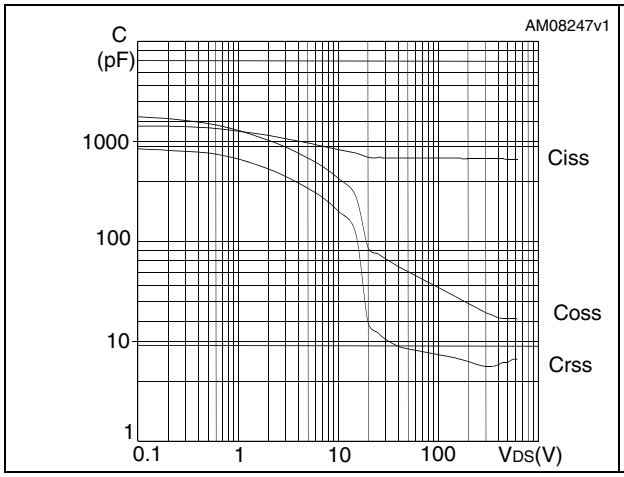


Figure 9. Output capacitance stored energy

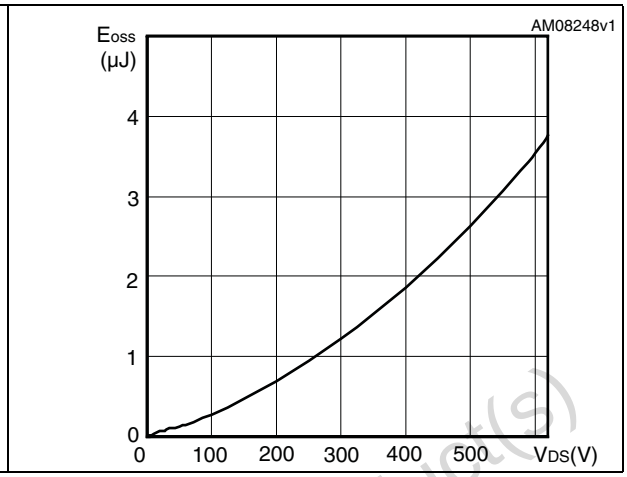


Figure 10. Normalized gate threshold voltage vs temperature

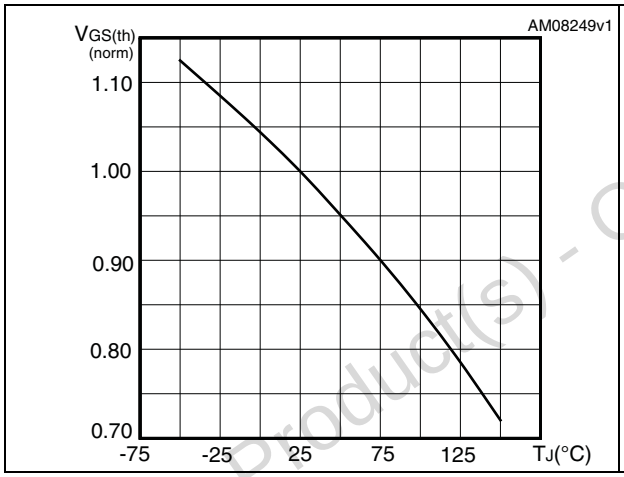


Figure 11. Normalized on-resistance vs temperature

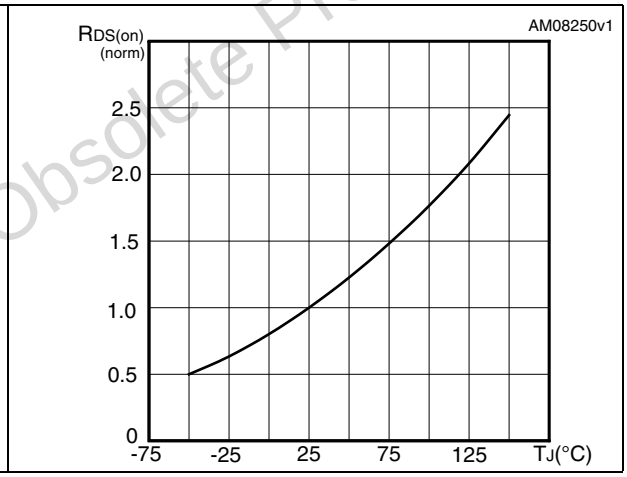


Figure 12. Source-drain diode forward characteristics

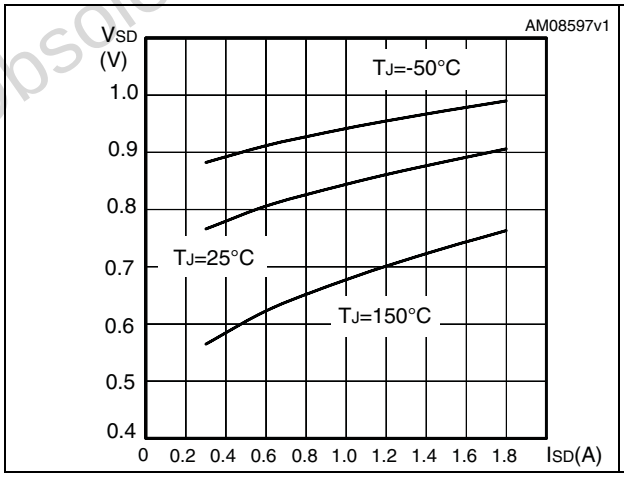


Figure 13. Normalized B_{VDSS} vs temperature

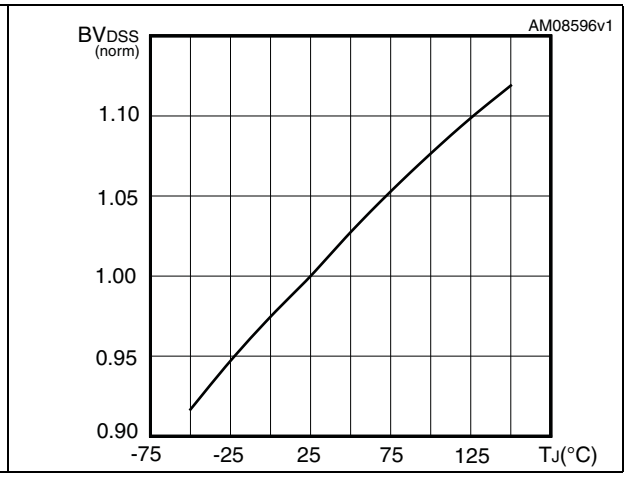
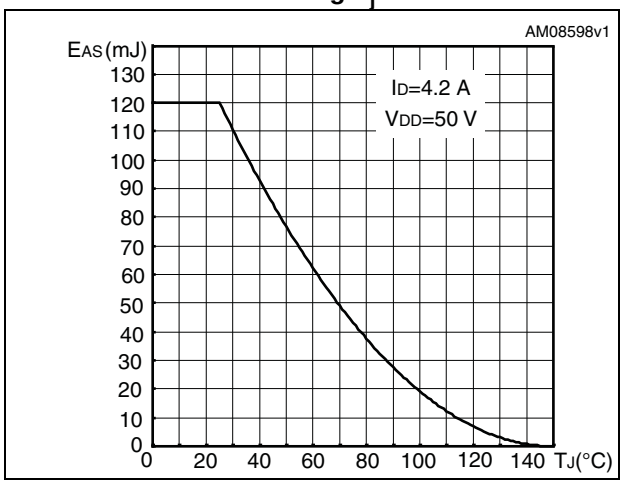


Figure 14. Maximum avalanche energy vs starting T_j



3 Test circuits

Figure 15. Switching times test circuit for resistive load

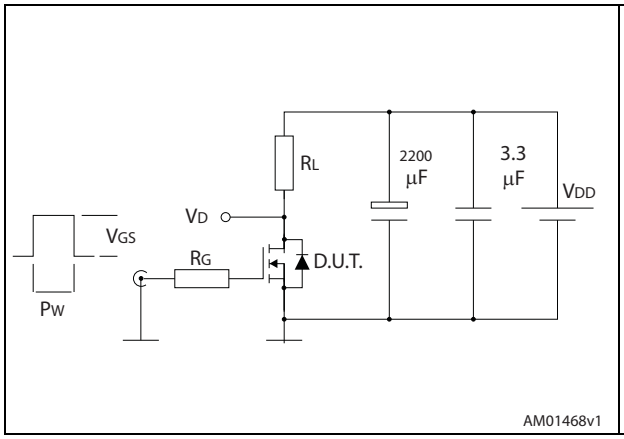


Figure 16. Gate charge test circuit

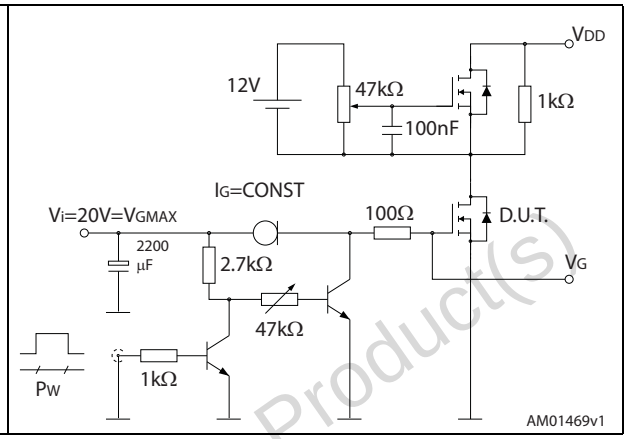


Figure 17. Test circuit for inductive load switching and diode recovery times

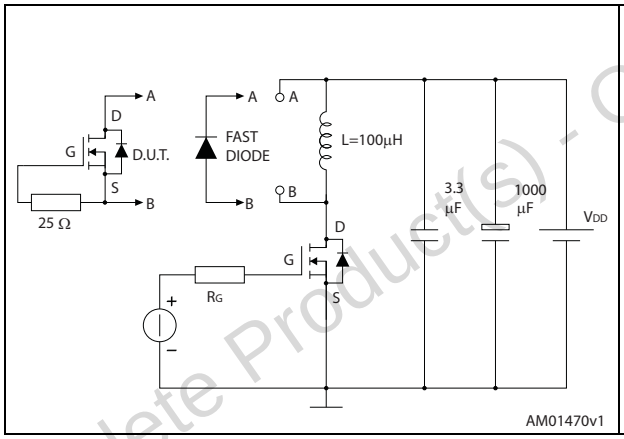


Figure 18. Unclamped inductive load test circuit

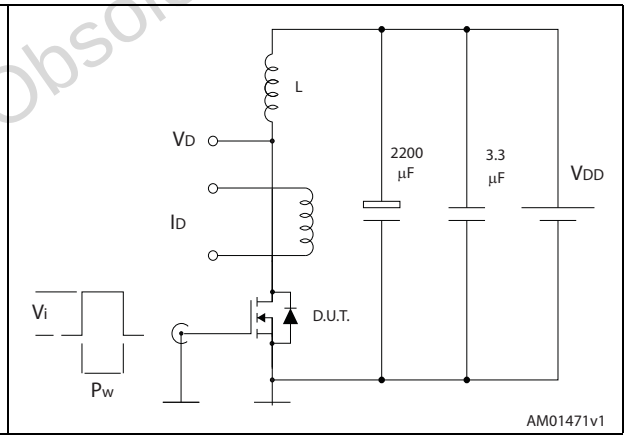


Figure 19. Unclamped inductive waveform

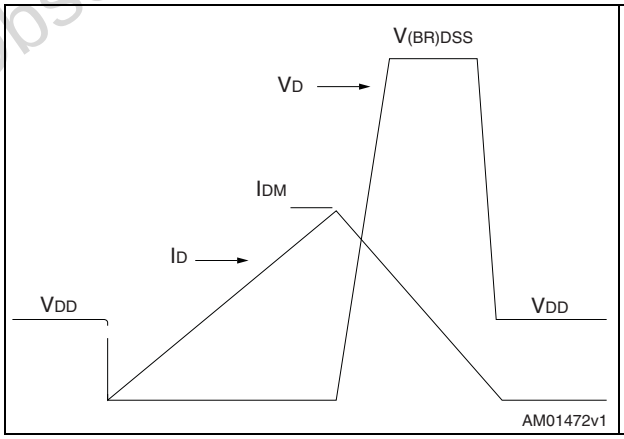
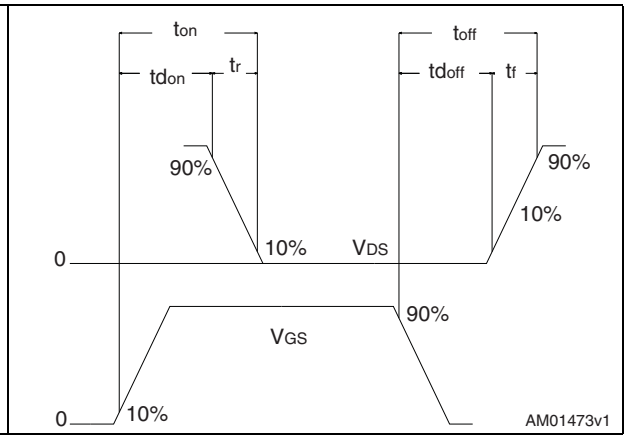


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) drawings

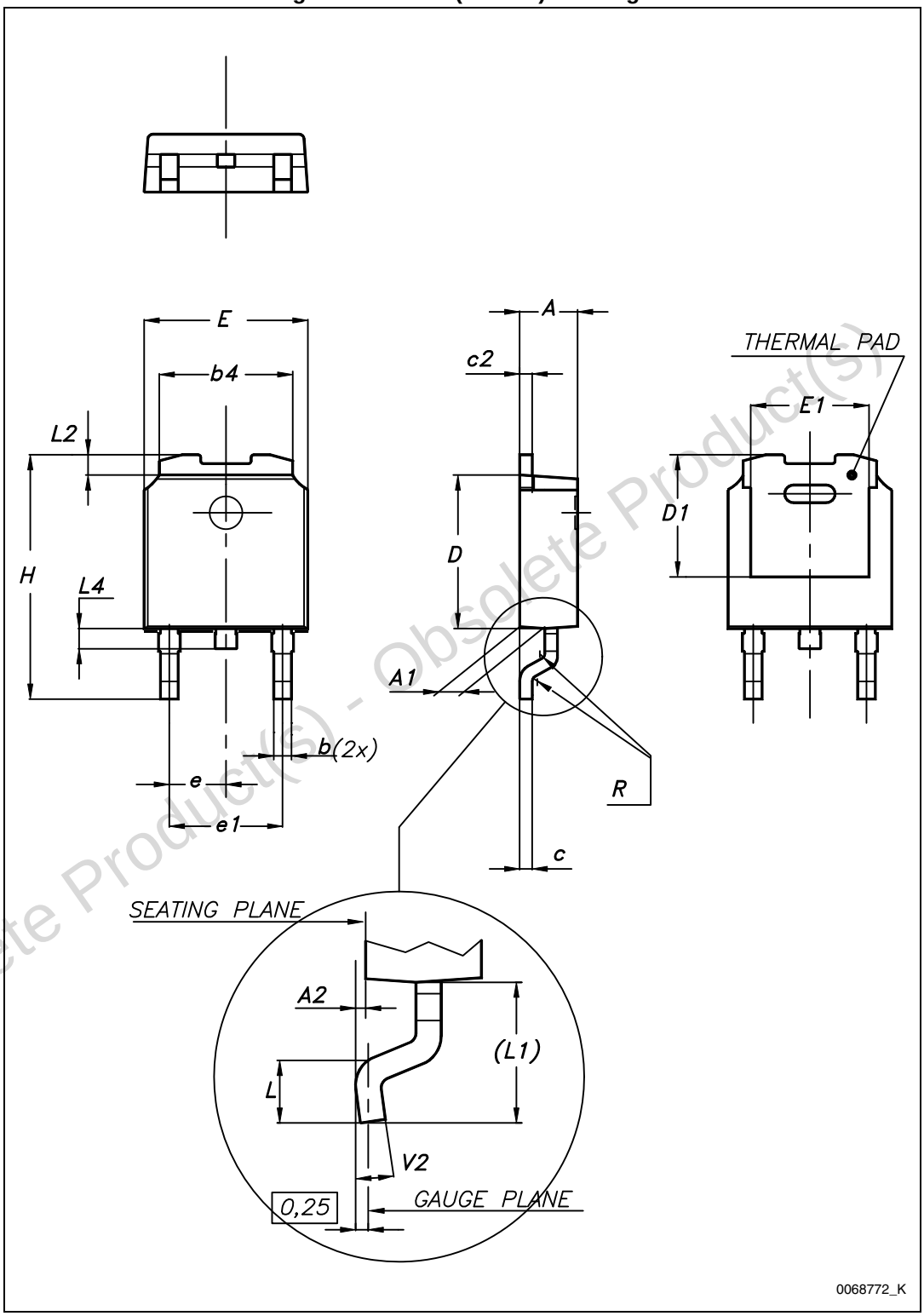
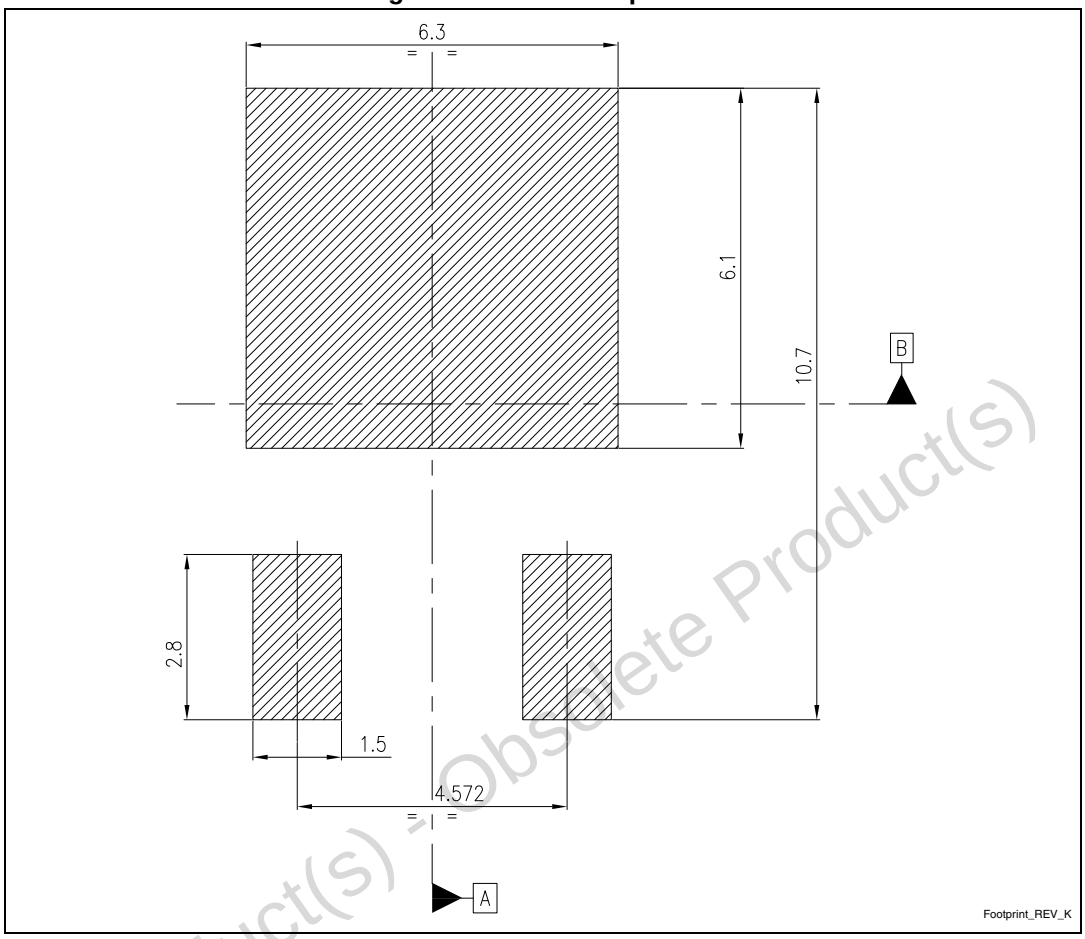


Figure 22. DPAK footprint [(a)]



a. All dimensions are in millimeters.

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 23. Tape for DPAK (TO-252)

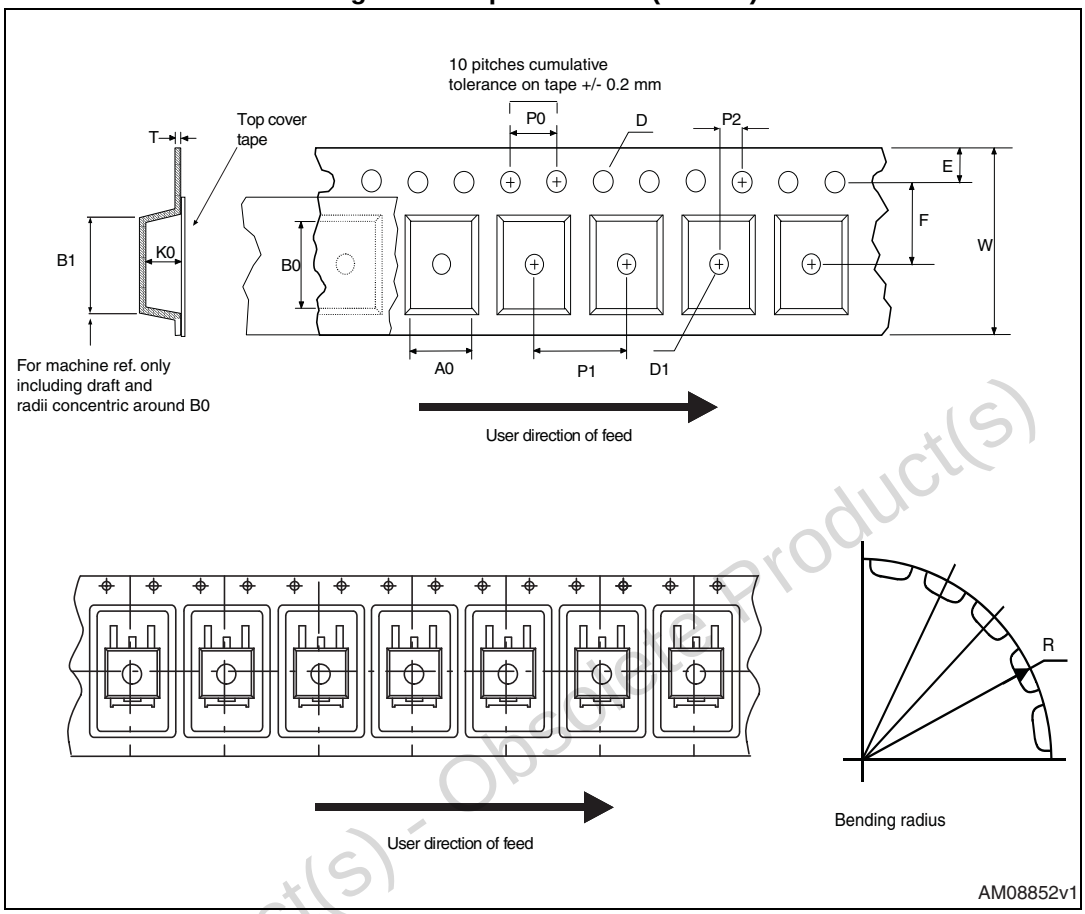


Figure 24. Reel for DPAK (TO-252)

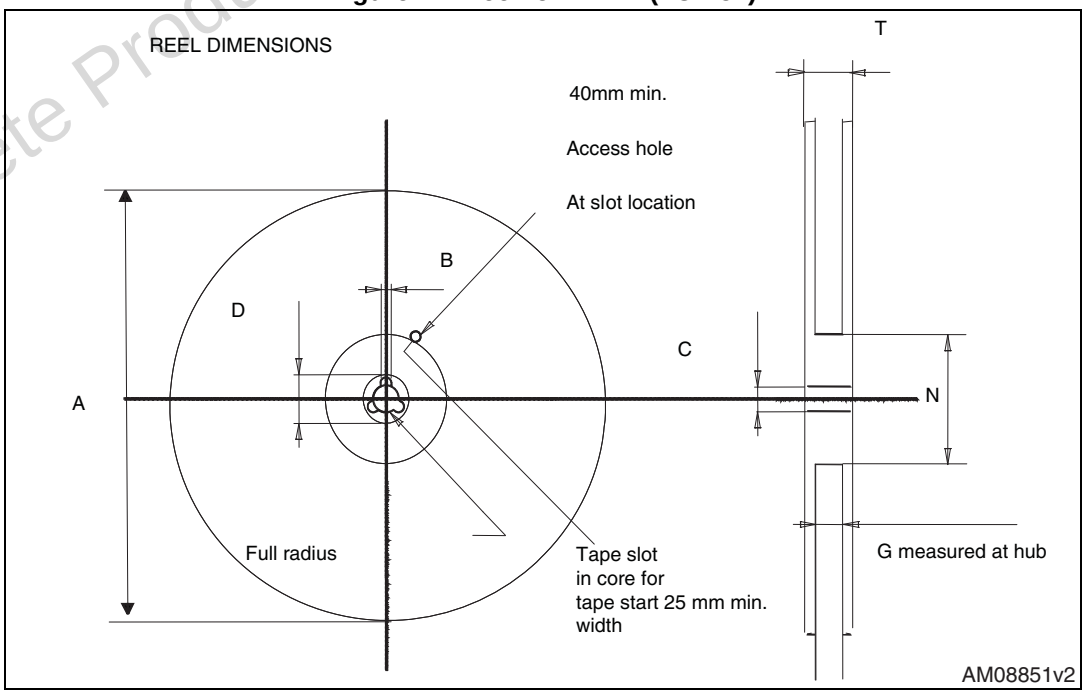
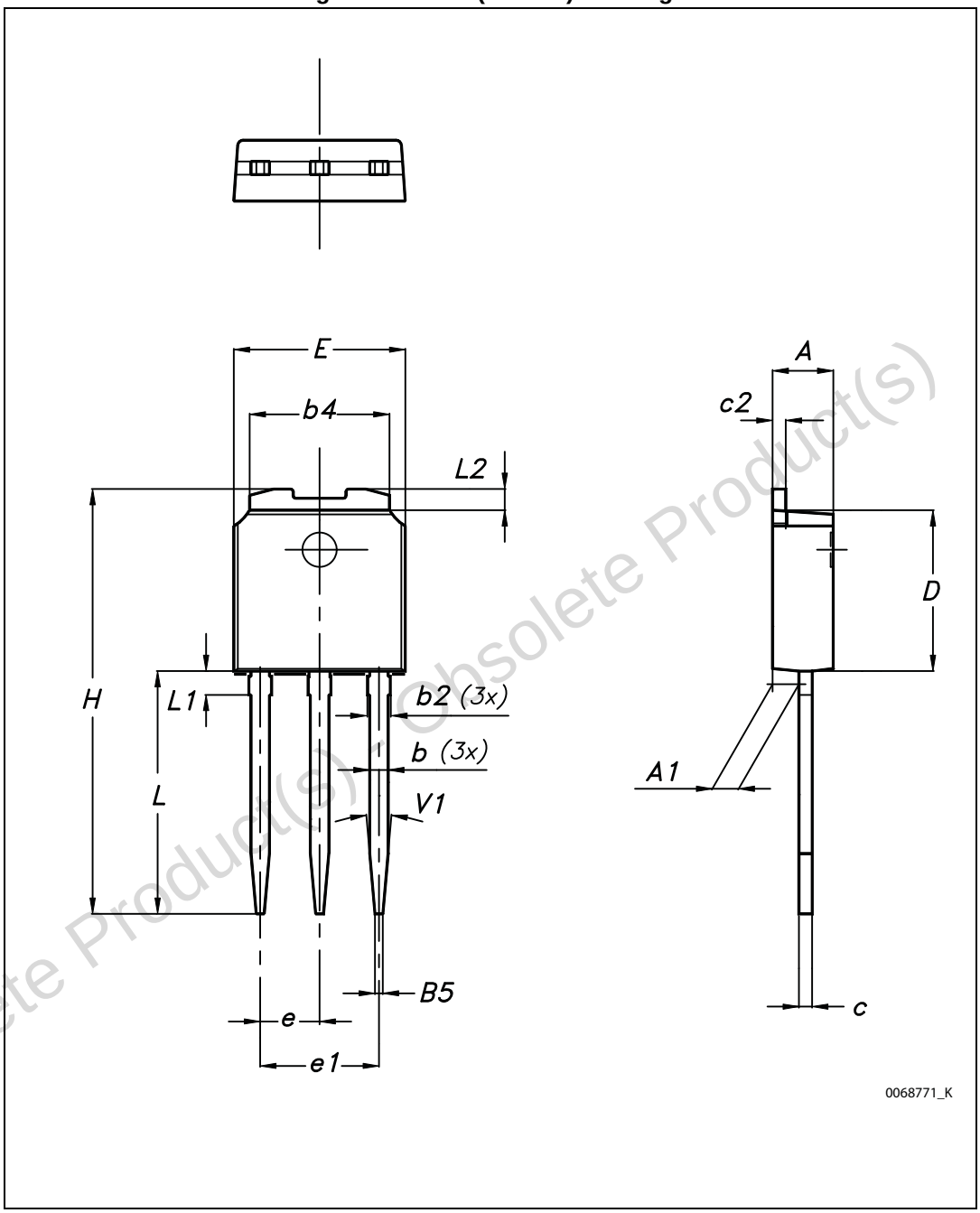


Table 11. IPAK (TO-251) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 25. IPAK (TO-251) drawings



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
28-Aug-2013	1	First release.

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