Document Number: MC13892ER
Rev. 10.0, 4/2012

MC13892, Silicon Errata

Introduction

Device Revision Identification

This errata sheet applies to the following devices:

Table 1. Silicon Revision

Package	Part Number	Silicon Revision	Part Marking	Die ID
139-PIN 7x7mm BGA	MC13892VK	2.0A	MC13892	DB00M29X
	MC13892JVK		MC13892J	
	MC13892AJVK	3.1 3.2 (1)	MC13892AJ	DB01M29X DB03M29X
	MC13892BJVK		MC13892BJ	
	MC13892CJVK MC13892DJVK	3.5	MC13892CJ MC13892DJ	DB05M29X DA03N57D
186-PIN 12x12mm BGA	MC13892VL	2.0A	MC13892VL	DB00M29X
	MC13892JVL		MC13892JVL	
	MC13892AJVL	3.1 3.2 (1)	MC13892AJVL	DB01M29X DB03M29X
	MC13892BJVL		MC13892BJVL	
	MC13892CJVL MC13892DJVL	3.5	MC13892CJVL MC13892DJVL	DB05M29X DA03N57D

Notes
1. Silicon revision 3.2 does not have a part marking difference. The revision is indicated with date code **1040** or greater.

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH0429”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “0429” indicates the 29th week of the year 2004.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

General Description

This errata document applies to MC13892 data sheet.

Table 2. Definitions of Errata Severity

Errata Type	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 3. High Severity Issues

Erratum ID	Erratum	System Impact	Description
8374	**RTC**: Loss on the crystal oscillator upon power up	The switch of the 32 kHz clock system from crystal to internal clock causes missing pulses in the 32 kHz clock, which lowers the frequency of the switcher PLL. The buck regulator then drops in output voltage.	**Workaround**: Place a 10 MOhm resistor in parallel with the crystal. **Fix/Plan Status:** Fixed in silicon in revision 3.1
8568	**Power**: If UVBUS is present before the battery, then an overshoot on the output of the switching regulators occurs	If UVBUS is present before the battery, the switcher acts as soon as the battery is present, instead of waiting until the power up sequence is initialized.This overshoot can tie the switcher output to BP for a short period.	**Workaround**: Place a 100 kOhm pull-down resistor on VCORE. **Note**: This workaround is only needed if the UVBUS supply is present before the battery. It is not needed if UVBUS is not used. **Fix/Plan Status:** Fixed in silicon in revision 3.1
8612	**Charger**: Reverse supply mode shuts off	The reverse supply mode shuts off when the temperature is above 90°C.	**Workaround**: Do not use reverse supply mode if the device is being used at this temperature. **Fix/Plan Status:** Fixed in silicon in revision 3.1
8690	**Buck Regulators**: Buck current limit does not function	The buck current limit does not function properly, there is no max current limit, and current limit may engage before the rated load current of the buck regulator.	**Workaround:** Immediately after power up firmware should disable the current limit by setting the SWILIMB SPI bit = 1. Application needs to provide current limit protection circuitry either in the battery or as a pre regulated supply to BP. **Fix/Plan Status:** None
8691, 8692	**Boost Regulator**: Serial LED Boost system interfering with REFCORE voltage	Activating the SWLED boost regulator can cause REFCORE perturbations which cause the part to shutdown.	**Workaround:** Do not use SWLED boost supply to provide power for backlight LED sinks. Use external supply to generate boost voltage required for backlight LEDs. **Fix/Plan Status:** None

Table 3. High Severity Issues

Erratum ID	Erratum	System Impact	Description
8870	**Charger**: BP over-voltage when hot plugging a high voltage charger	When hot plugging a high voltage charger, the BP node can spike greater than 7.5 V.	**Workaround:** Use an over-voltage protection IC on the charger input **Fix/Plan Status:** None
8938	**Charger**: Failure of charger removal detection	Charger removal may not always be detected by the PMIC. This causes the charge path to stay on and the battery voltage to be present at charger input. Which could cause the charge LED to be illuminated if present in the application.	**Workaround:** Use software to poll the charger current via an ADC reading every one second, to check if the charger is detected. Disable it when the charge current goes below a reading of 3, or is negative. MC13892 Charger LED Driver patch for the i.MX35PDK is posted to: http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=IMX35PDK&fpsp=1&tab=Design_Tools_Tab **Detailed Description of Software** • When a charger is detected, CHRGDETI = 1 and CHRGDETS = 1, software needs to poll the charge current ADC every one second. • Check the value of the “Charger Current (CHRGISNS-BPSNS)” by writing a 1 on CHRGICON (Reg#43, bit#1) and writing a 4 on ADA1 (Reg#44, Bits 5-7). • Take eight readings from the ADC for the charger current, discard the largest and smallest values, and average the remaining six. • Take this average and DISABLE THE CHARGER if the reading is “<= 3”, or “NEGATIVE”. All negative readings have the last bit set to 1. • To disable the charger, set ICHRG[3:0] = 0000 and set the CHGAUTOVIB = 1. • Wait 1000 ms. • Re-enable the charger by setting CHGAUTOVIB = 0. • If the average is > 3, then continue polling the charger current every 1 second. • If CHGDETI = 1 and CHGDETS =0, polling every one second should not take place. **Fix/Plan Status:** Fixed in silicon in revision 3.5

Table 4. Medium Severity Issues

Erratum ID	Erratum	System Impact	Description
8372	**Power**: REGSCPEN behavior does not match the spec.	The LDO SCPI does not work as per spec. The interrupt SCPI is generated when a short-circuit is detected, even if the REGSPEN bit is not set (the spec says that in this case the interrupt should not fire).	**Workaround**: Recommendation is to have a short circuit protection enabled by setting the REGSCPEN bit. However, if it is desired to disable REGSCPEN, when SCPI interrupt occurs follow the below steps to identify the interrupt source: a) If backlight is enabled, Read both LED Control 0 and LED Control 1 registers i. If both are equal to 0x), then SCPI indicates interrupt from the backlight LED drivers. ii. If both are not equal to 0x0, then SCPI indicates short circuit protection of a regulator b) If backlight is disabled, SCPI indicates short circuit protection of a regulator. **Fix/Plan Status:** Fixed in silicon in revision 3.1
8375	**Charger**: BP to CHRGRAW leakage.	When the BP is in POWER OFF state, the Standby leakage currents on the BPSNS and CHRGISNS pins are ~ 35 μA. If UVBUS is connected to CHRGRAW, there is an additional 35 μA of leakage current.	**Workaround:** None **Fix/Plan Status:** Fixed in silicon in revision 3.1
8382	**USB**: UVBUS turn on event works only if the ramp is < 50 ms.	The USB attach turn on event only works if the ramp of UVBUS from 0 to 4.4 V is <50 ms.	**Workaround**: (3 options are available): 1. Speed up the UVBUS turn on time. 2. Work with a common USB and charger path. A turn on event will occur when USB is plugged in. 3. Use any other turn on event to power up. **Fix/Plan Status:** Fixed in silicon in revision 3.1

Table 4. Medium Severity Issues

Erratum ID	Erratum	System Impact	Description
8719	**Charger**: Operation from wall charger with no battery via the charge path or if the battery is deeply discharged.	When using the battery charger as the only source of power, as in a battery-less application or if the battery is deeply discharged, the following precautions should be observed: 1. It is still necessary to connect ADIN5 to either VCOREDIG or a midpoint of a divider from GPIO1 to ground since the battery charger will still interpret this voltage as the battery pack thermistor by default. 2. Very careful budgeting of the total current consumption and voltage standoff from CHRGRAW to BPSNS must be made, since the power limiter is operational by default, and a battery less or if the battery is deeply discharged system won't have a source of current if the power dissipation limit is reached. 3. If operating from a USB host the unit load limit (100 mA max.) must still be observed. 4. If operating from a “wall charger”, and if there is no battery or if the battery is deeply discharged, there is an period of approximately 85 ms after RESETB is released, that the current limit is set to 80mA before setting the current limit is set to a nominal 560 mA. If the total current demand is greater than this limit, or if the battery is deeply discharged, the voltage may collapse and RESETB may pulse a few times (depending in part in the system load and dependence on RESETB.) Therefore, at the end of this time, RESETB may or may not be active. It may be necessary to use one of the other turn-on events (such as PWRONx) to turn the 13892 back on.	**Workaround:** • Add a 120mS RC delay on RESETBMCU. • Add a 68K pull-up resistor to the I/O rail at the RESETBMCU output. • Add a 100 Ohm resistor from the RESETBMCU output of the PMIC to the processors reset input. • Add a 2.2uF capacitor to ground on the processor side of the 100 Ohm resistor. • Repeat the above steps for RESETB. **Fix/Plan Status:** Fixed in silicon in revision 3.2
8732	**Buck Regulator**: Buck current limit interaction with DVS	The buck current limit can be reached if an output voltage increase is requested on a buck regulator while close to max load. The consequence is that the programmed output voltage is not reached, during the DVS ramp up phase, the coil current increases temporarily to permit an output rise, and can reach current limit.	**Workaround**: When ramping buck regulator voltage from a lower to a higher set point near max load, disable current limit by setting the SWILIMB SPI bit = 1. **Fix/Plan Status:** None
8945	**ADC**: Erroneous ADC Reading	Erroneous readings occur on the die temperature and the CHRGRAW ADC channels when the IC fails to detect the removal of the charger (see Errata 8938).	**Workaround:** None **Fix/Plan Status:** Fixed in silicon in revision 3.5
8982	**USB**: Leakage increases when VINUSB goes above 5.1 V	When the VINUSB voltage exceeds 5.1 V, excess current flows into the USB node.	**Workaround:** None **Fix/Plan Status:** Fixed in silicon in revision 3.5

Table 4. Medium Severity Issues

Erratum ID	Erratum	System Impact	Description
8939	**Charger**: Incorrect battery current measurement	When measuring the current from the battery, there is an offset of ~30 mA to 50 mA from the actual value.	**Workaround:** Calibrate the ADC offset during production. Calculate the average slope and add the offset to the battery current. **Fix/Plan Status:** None
8940	**Charger**: Incorrect charger voltage measurement	When measuring the voltage from the attached charger, there is an offset from the actual value.	**Workaround:** Calibrate the ADC offset during production. Calculate the average slope and add the offset to the battery voltage. **Fix/Plan Status:** None

Table 5. Low Severity Issues

Erratum ID	Erratum	System Impact	Description
8373	**Coin Cell**: Leakage current on the LICELL.	When the coin cell is present and the battery is disconnected, a leakage current around 2.0 to 3.0 μA with BP=high-impedance and 2mA if BP is actively pulled to ground can be observed from BP to GND, and also a leakage voltage of 0.3 to 0.49 V. This leakage current comes from the coin cell.	**Workaround:** Add NMOS switch or load switch between BP and VINAUDIO with source connected to BP and the drain connected to the VINAUDIO. Enable the switch when application is ON and disable when OFF. **Fix/Plan Status:** Fixed in silicon in revision 3.1
7640	**Lighting System**: LED currents are higher than spec	Signaling LED and backlight LED currents are higher than target value by ~ 10%	**Workaround**: If LEDs cannot handle 10% higher current, then program the current sinks to one level below the required setting. **Fix/Plan Status:** Fixed in silicon in revision 3.1
8718	**Control Logic**: PWRONx pin grounded not able to power on IC with other PWRONx pin	If any of the PWRONx pins are grounded, neither of the other 2 PWRON pins are able to generate a turn on event.	**Workaround**: Set the PWRONxDBNC bits (or at least the ones for the offending PWRON pin) to non-zero. **Fix/Plan Status:** None
8849	**Charger**: Charger path reverse current threshold is too high	Charger path reverse current threshold is too high. Threshold is ~ 120 to180 mA, where it should be 35 mA. This only impacts reverse supply mode from the battery to an external accessory via the charge path.	**Workaround**: None **Fix/Plan Status:** None
8944	**ADC**: Code spike on the ADC	1 out of 33 k readings can have a positive or negative code spike	**Workaround:** Take a minimum of 8 readings on ADC channels and remove the max and min. values, then take the average of these readings. **Fix/Plan Status:** None

Table 5. Low Severity Issues

Erratum ID	Erratum	System Impact	Description
8969	**Charger**: End of charge detection failure	When the CYCLB is set, the end of charge is not detected.	**Workaround:** The CYCLB bit must be cleared for correct End of Charge detection. **Fix/Plan Status:** None
8970	**Backlight Drivers**: Changing duty cycle of backlight LED current sinks (LEDMD, LEDAD, LEDKP) from 100% to 0% results in additional ~110uA being drawn from the battery intermittently	Additional ~110uA drawn from the battery intermittently	**Workaround**: 1. From 100% duty cycle go to an intermediate duty cycle before going to 0% duty cycle. 2. Set LEDxxRAMP = 1 while transitioning from100% to 0% duty cycle. 3. Don't use 100% duty cycle setting. Use 96.8% (31/32) setting instead, for example. **Fix/Plan Status:** None

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	2/2010	• Initial Release
5.0	5/2010	• Errata updated to add MC qualified part numbers to Silicon Revision
6.0	10/2010	• Added errata 8870, 8873, and 8849 • Removed errata 8682 and 7874
7.0	10/2010	• Removed paragraph describing the device revision identification, since it did not apply to part marking
8.0	11/2011	• Added MC13892CJVK and MC13892CJVL part numbers for P3.5 Silicon Revision • Added errata 8938, 8945, 8982, 8939, 8940, 8944, and 8969
9.0	3/2012	• Added erratum 8970
10.0	4/2012	• Added MC13892DJVK and MC13892DJVL part numbers to Silicon Revision

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Rev. 10.0
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