TEA1553T

GreenChip II SMPS control IC

Rev. 01 — 3 July 2007 Product data sheet

1. General description

The GreenChip II is the second generation of green Switched Mode Power Supply (SMPS) controller ICs operating directly from the rectified universal mains. A high level of integration leads to a cost effective power supply with a very low number of external components.

The special built-in green functions allow optimum efficiency at all power levels. This applies to quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates at reduced frequency and with valley detection.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. A second low voltage BICMOS IC is used for accurate, high speed protection functions and control.

Highly efficient, reliable supplies can easily be designed using the GreenChip II controller.

2. Features

2.1 Distinctive features

- Universal mains supply operation (70 V AC to 276 V AC)
- High level of integration, giving a very low external component count

2.2 Green features

- Valley/zero voltage switching for minimum switching losses
- Frequency reduction at low power standby for improved system efficiency (< 1 W)
- On-chip start-up current source
- Efficient quasi-resonant operation at high power levels
- Cycle skipping mode at very low loads; input power < 300 mW at no-load operation for a typical adapter application
- Standby indication pin to indicate low output power consumption

2.3 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection (zero switch-on current)
- Accurate and adjustable versatile Overvoltage Protection (OVP) (latched)
- Short winding protection
- Undervoltage protection (foldback during overload)

- Overtemperature Protection (OTP) (latched)
- Low and adjustable Overcurrent Protection (OCP) trip level
- General purpose LOCK input for external protection
- Mains voltage-dependent operation-enabling level
- Soft (re)start
- Advanced Overpower Protection (OPP) functions

3. Applications

Besides typical application areas, i.e. adapters and chargers, the device can be used in all applications that demand an efficient and cost effective solution up to 250 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1553T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

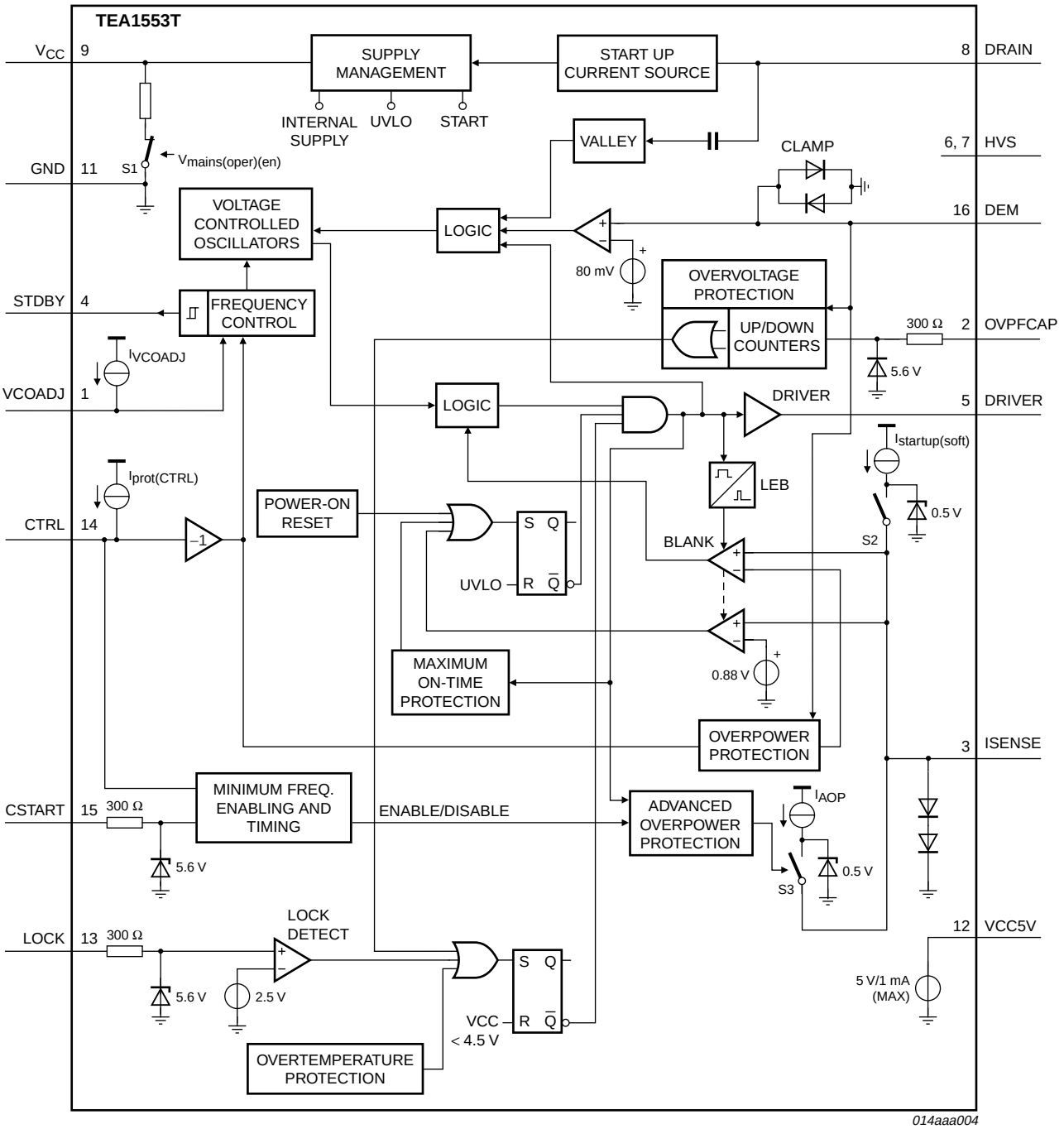


Fig 1. Block diagram of TEA1553T

6. Pinning information

6.1 Pinning

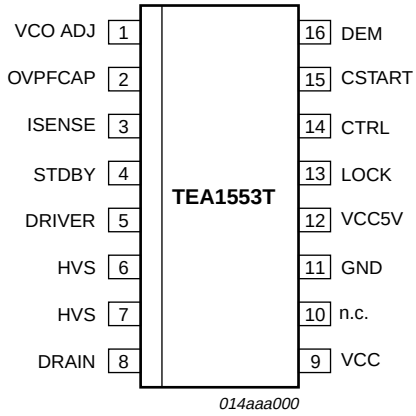


Fig 2. Pin configuration for TEA1553T

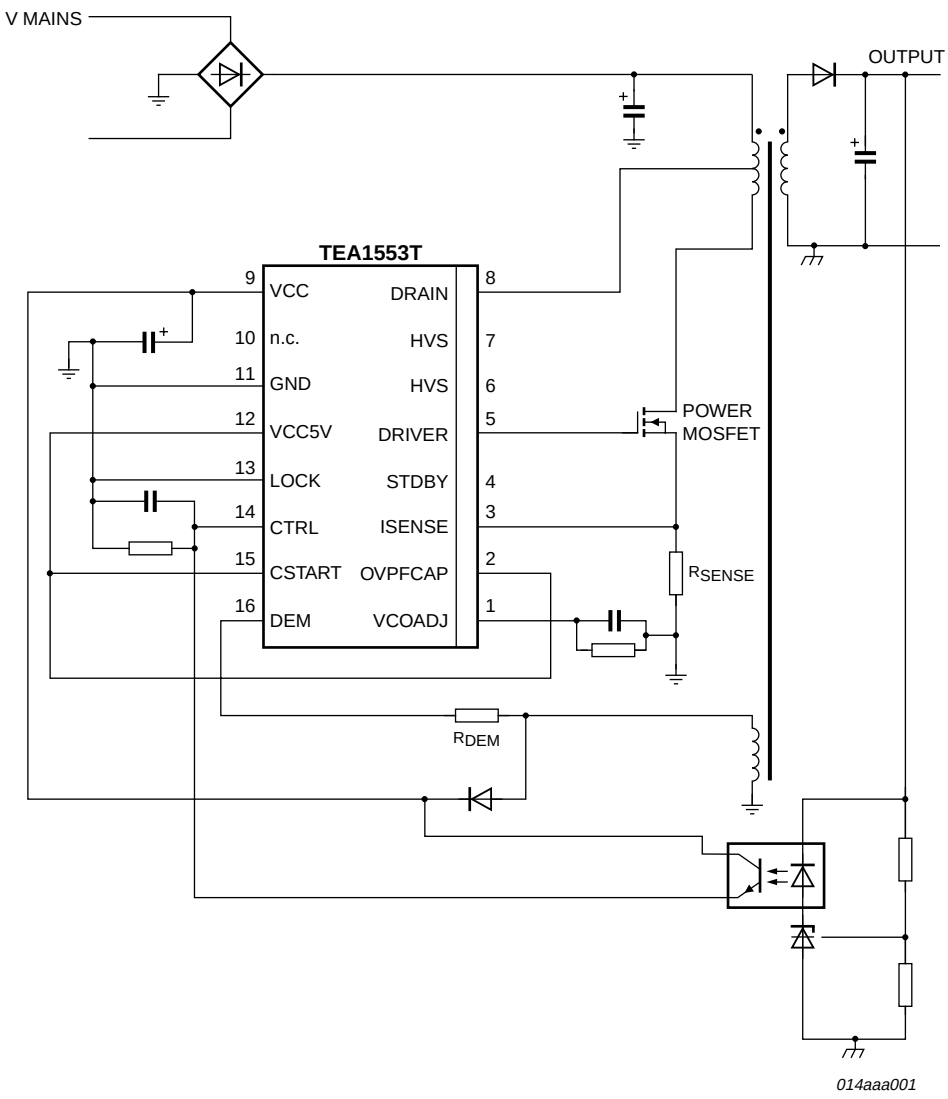
6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCOADJ	1	Voltage Controlled Oscillator (VCO) adjustment input
OVPFCAP	2	OVP filter timing capacitor
ISENSE	3	programmable current sense input
STDBY	4	standby control output
DRIVER	5	gate driver output
HVS	6	high voltage safety spacer, not connected
HVS	7	high voltage safety spacer, not connected
DRAIN	8	drain of external MOS switch, input for start-up current and valley sensing
V_{CC}	9	supply voltage
n.c.	10	not connected
GND	11	ground
VCC5V	12	5 V output
LOCK	13	LOCK input (“general purpose input for switching off the IC”).
CTRL	14	control input
CSTART	15	IPEAK reduction timing capacitor
DEM	16	input from auxiliary winding for demagnetization timing, OVP and OPP

7. Functional description

The TEA1553T is a controller for a compact flyback converter, with the IC situated on the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up.



(1) If a 600 V MOSFET is used, the DRAIN connection can be made directly to the Vin; a center-tap from the transformer is not necessary.

Fig 3. Basic application

The TEA1553T operates in multi modes, see Figure 4.

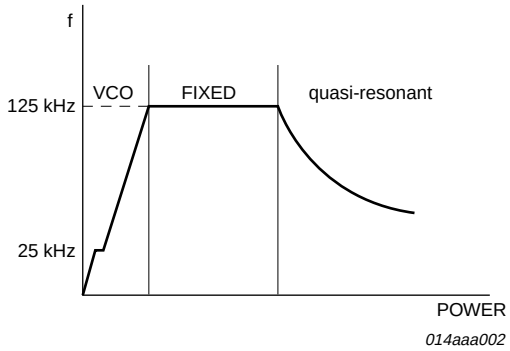


Fig 4. Multi mode operation

The next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to prevent switching losses (green function). The primary resonant circuit of primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can be achieved over almost the whole of the universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency Pulse Width Modulation (PWM) control.

At low power levels, the frequency is controlled via the Voltage Controlled Oscillator (VCO), down to a minimum of about 25 kHz.

At very low power levels (standby), a cycle skipping mode will be activated.

7.1 Start-up, mains enabling operation level and undervoltage lock-out

Initially, the IC is self-supplying from the rectified mains voltage via pin DRAIN. Supply capacitor C_{VCC} is charged by the internal start-up current source to a level of about 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds $V_{mains(oper)(en)}$ (mains-dependent operation-enabling voltage), the start-up current source will continue charging capacitor C_{VCC} (switch S1 will be opened); see Figure 1. The IC will activate the power converter as soon as the voltage on pin V_{CC} passes the $V_{startup}$ level. The IC supply is taken over by the auxiliary winding as soon as the output voltage reaches its intended level and the IC supply from the mains voltage is subsequently stopped for high efficiency operation (green function).

The moment the voltage on pin V_{CC} drops below the $V_{th(UVLO)}$ (undervoltage lock-out) level, the IC stops switching and enters a safe restart from the rectified mains voltage. Inhibiting the auxiliary supply by external means causes the converter to operate in a stable, well defined burst mode. (See Figure 14 and Figure 15).

7.2 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.3 Current mode control

Current mode control is used for its good line regulation behavior.

The on-time, is controlled by the internally inverted control pin voltage, which is compared with the primary current information. The primary current is sensed across an external resistor. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external control pin voltage, with an offset of 1.5 V. This means that a voltage range from 1 to 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 V to 0 V (a high external control voltage results in a small duty cycle).

7.4 Oscillator

The maximum fixed frequency of the oscillator is set by an internal current source and capacitor. The maximum frequency is reduced once the control voltage enters the VCO control window. It then changes linearly with the control voltage until the minimum frequency is reached (see Figure 5 and Figure 6).

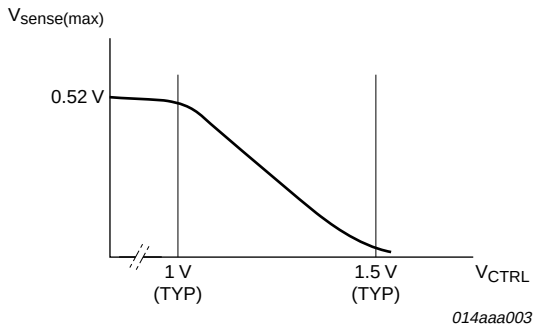


Fig 5. The $V_{sense(max)}$ voltage as a function of V_{CTRL}

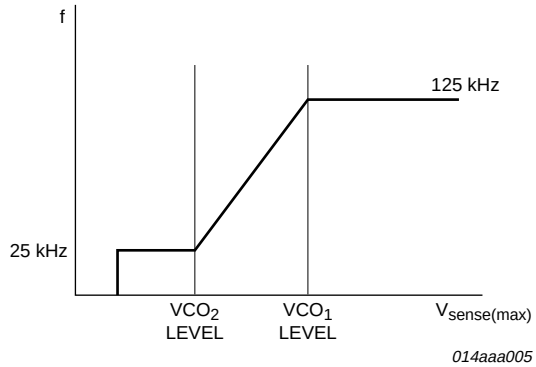


Fig 6. The VCO frequency as a function of $V_{sense\ (max)}$

7.5 VCO adjust

The VCOADJ pin can be used to set the VCO operation point. As soon as the peak voltage on the sense resistor is controlled below half the voltage on the VCOADJ pin (VCO_1 level), frequency reduction will start. (The actual peak voltage on R_{sense} will be somewhat higher due to switch-off delay, see Figure 8.) The frequency reduction will stop about 50 mV lower (VCO_2 level), when the minimum frequency is reached.

A current of typically 10 μA flows out of the VCOADJ pin, enabling the VCO operation point to be set with a single resistor. When a more low-ohmic connection is desired (e.g. due to noise), a voltage divider can be made from the VCC5V pin (see Figure 7).

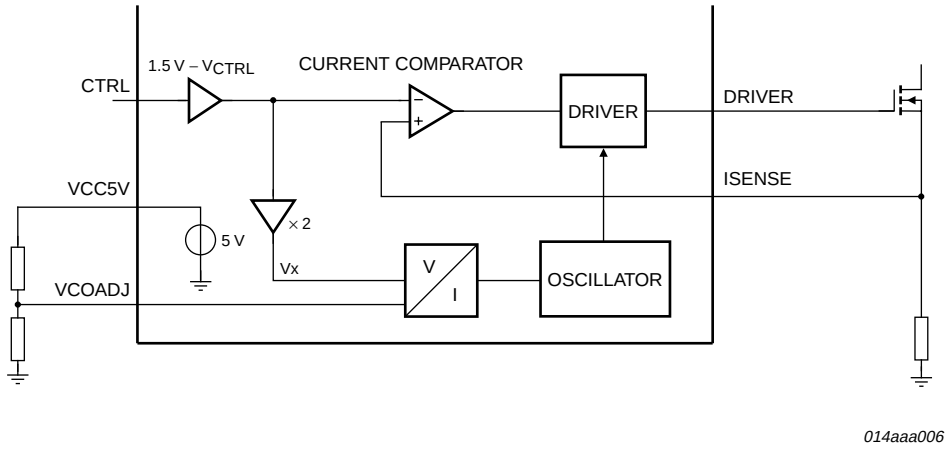
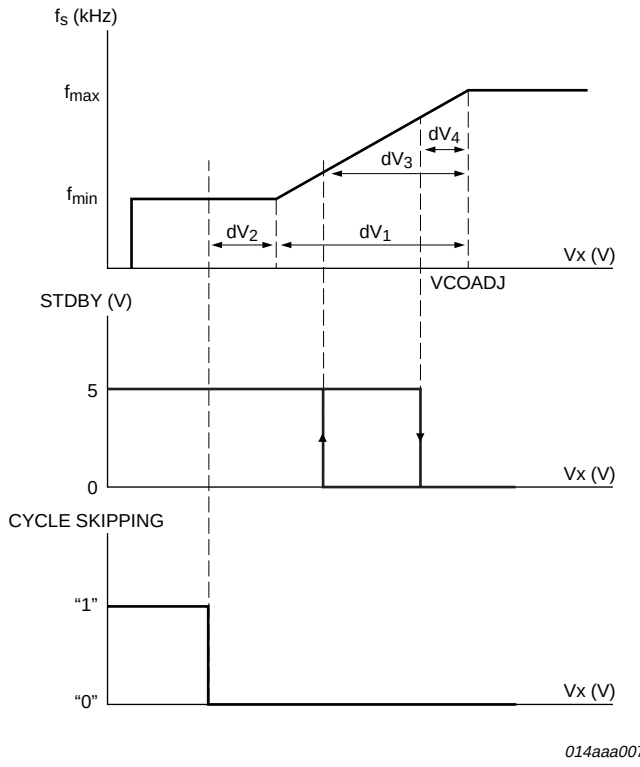


Fig 7. Implementation of STDBY and cycle skipping functionality



(1) The voltage levels dV_1, dV_2, dV_3 and dV_4 are fixed in the IC to 50 mV (typ.), 18 mV (typ.), 40 mV (typ.) and 15 mV (typ.) respectively. The level at which the VCO mode of operation starts/ends can be externally controlled with the VCOADJ pin.

Fig 8. Signal diagram for STDBY and cycle skipping functionality

7.6 Cycle skipping

At very low power levels, a cycle skipping mode will be activated. A high control voltage will reduce the switching frequency to a minimum of 25 kHz. If the voltage on the control pin is raised even more, switch-on of the external power MOSFET will be inhibited until the voltage on the control pin has dropped to a lower value again (see Figure 8).

For system accuracy, the absolute voltage on the control pin is not used to trigger the cycle skipping mode. Instead, a signal derived from the internal VCO will be used.

If the no-load requirement of the system is such that the output voltage can be regulated to its intended level at a switching frequency of 25 kHz or above, the cycle skipping mode will not be activated.

7.7 STDBY output

The STDBY output pin can be used to drive an external NPN or FET, V_{STDBY} = 5 V, in order to switch off a Power Factor Correction (PFC) circuit. The STDBY output is activated by the internal VCO: as soon as the VCO has reduced the switching frequency to almost the minimum frequency of 25 kHz, the STDBY output will be activated (see Figure 8). The STDBY output will go low again as soon as the VCO allows a switching frequency close to the maximum frequency of 125 kHz.

7.8 Demagnetization

The system will be in discontinuous conduction mode all the time. The oscillator will not start a new primary stroke until the secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages/start-up.

7.9 Overvoltage protection

An OVP mode is implemented in the GreenChip series. For the TEA1553T, this works by sensing the auxiliary voltage via the current flowing into pin DEM during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Any voltage spikes are averaged by an internal filter.

Pin OVPFCAP is used to program the OVP function as follows:

1. Pin grounded: OVP is disabled.
2. Pin at 5 V (e.g. connected to pin 12, the VCC5V pin): the internal OVP circuit is enabled.
3. A capacitor is connected from the pin to the ground: this capacitor is used to set the number of OVP events that can occur before the logic determines that an actual OVP condition exists. The minimum timing is the internal OVP timing.

In the last case, the number of OVP events can be set by an external capacitor connected to pin OVPFCAP:

$$C_{OVP} = n \times \frac{I_{ch(OVPFCAP)} \times t_{p(OVPFCAP)}}{V_{OVPFCAP}}$$

Where n is the number of OVP counts which are allowed to occur before an actual OVP state is detected.

If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detections which could occur during ESD / lightning events.

If the output voltage exceeds the OVP trip level a few times, and then does not exceed it in the next cycle, the internal counter will count down twice as fast as it counted up. However, when typically 10 cycles of subsequent OVP events are detected, the IC assumes a true OVP state exists and the OVP circuit switches the MOSFET off. Next, the controller waits until the $V_{th(UVLO)}$ level is reached on pin V_{CC}, and then capacitor C_{VCC} is recharged to the $V_{startup}$ level.

Operation only recommences when the V_{CC} voltage drops below a level of about 4.5 V, in practice this only occurs when the mains input voltage has been disconnected for a short period of time

The output voltage at which the OVP function trips, $V_{trip(OVPFCAP)}$, can be set by the demagnetization resistor, R_{DEM}:

$$V_{trip(OVPFCAP)} = \frac{N_S}{N_{aux}} \times (I_{ovp} \times R_{DEM} + V_{CL(pos)})$$

Where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer.

Current I_{ovp} is internally trimmed.

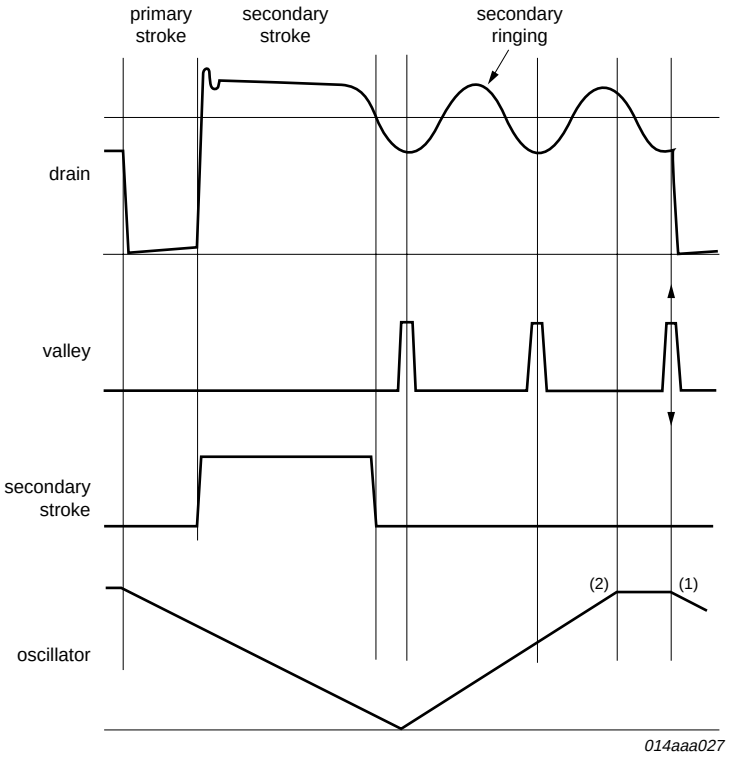
The value of the demagnetization resistor, R_{DEM}, can be adjusted to the turns ratio of the transformer, thus making an accurate OVP possible.

7.10 Valley switching

(See Figure 9.) A new cycle starts when the power switch is switched on. After the 'on-time' (which is determined by the 'sense' voltage and the internal control voltage), the switch is opened and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)})}$ where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 9 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is possible, preventing large capacitive losses $\left(P = \frac{1}{2} \times C \times V^2 \times f\right)$, and allowing high frequency operation, which results in small and cost effective inductors.



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical PWM system at high drain voltage.

Fig 9. Signals for valley switching

7.11 Overcurrent protection

The cycle-by-cycle peak drain current limit circuit uses the external source resistor to measure the current accurately. This allows optimum size of the transformer core to be determined (cost issue). The circuit is activated after the leading edge blanking time, t_{leb}. The OCP protection circuit limits the 'sense' voltage to an internal level.

7.12 Overpower protection

During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current is dependent on the mains voltage, according to the following formula:

$$I_{DEM} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$$

Where: $N = \frac{N_{aux}}{N_p}$

The current information is used to adjust the peak drain current, which is measured via pin ISENSE. The internal compensation is such that a maximum output power can be achieved that is almost mains independent.

The OPP curve is given in Figure 10.

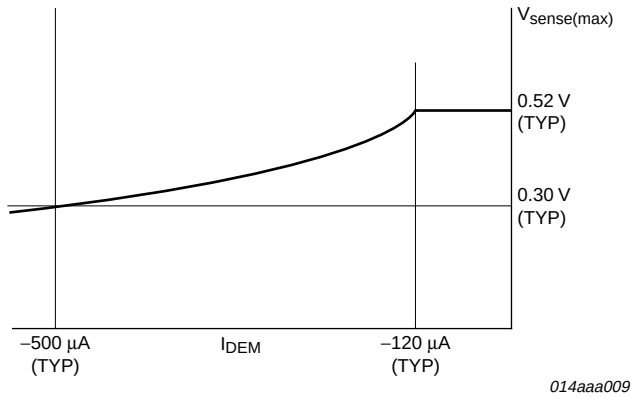


Fig 10. OPP correction curve

7.13 Advanced overpower timing via pin CSTART

Overload conditions might lower the switching frequency below 20 kHz, since demagnetization prevents next cycle occurrence before the transformer current reaches zero (demagnetization protection). To prevent audible noise, an extra timer of typically 25 kHz is added. When the timer is activated (the frequency is typically below 25 kHz), a current (I_{AOP}) of approximately 10 µA is injected into the external soft-start resistor and capacitor. The current that is being injected is dependent on the V_{SENSE} voltage and the duty cycle, see also Figure 11 and Figure 12.

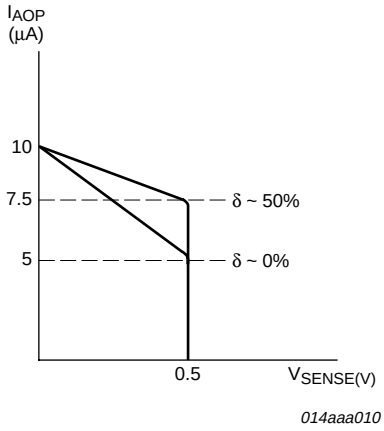


Fig 11. I_{AOP} as a function of V_{SENSE}

The current injection results in a decrease of the primary peak current and a higher frequency. The injection is only possible when the voltage on the control pin is below 0.5 V and the CSTART voltage is above 2.5 V. The current injection is disabled when V_{CTRL} > 0.5 V (that is, in normal operation and also in frequency reduction mode), during start-up (CSTART timing) and when V_{SENSE} > 0.5 V.

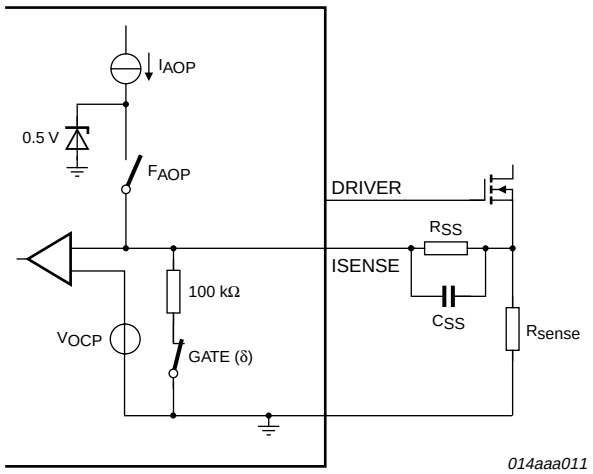


Fig 12. Advanced overpower current injection

The charging current, $I_{opp(adv)}$, will flow as long as the voltage on pin ISENSE is below approximately 0.5 V. If it exceeds this value, the current source will start to limit the current $I_{opp(adv)}$.

7.14 Minimum and maximum ‘on-time’

The minimum ‘on-time’ of the SMPS is determined by the Leading Edge Blanking (LEB) time. The IC limits the maximum ‘on-time’ to 50 µs. When the system requires an ‘on-time’ longer than 50 µs, a fault condition is assumed (e.g. C_i has been removed), the IC will stop switching and enter the safe restart mode.

7.15 Short winding protection

After the leading edge blanking time, the short winding protection circuit is also activated. If the ‘sense’ voltage exceeds the short winding protection voltage, V_{swp}, the converter will stop switching. Once V_{CC} drops below the $V_{th(UVLO)}$ level, capacitor C_{VCC} will be recharged and the supply will restart again. This cycle will be repeated until the short circuit is removed (safe restart mode).

The short winding protection will also protect in case of a secondary diode short circuit.

7.16 LOCK input

Pin 13 is a general purpose (high impedance) input pin, which can be used to switch off the IC. As soon as the voltage on this pin is raised above 2.5 V, switching will stop immediately. The voltage on the V_{CC} pin will cycle between $V_{startup}$ and $V_{th(UVLO)}$, but the IC will not start switching again until the latch function is reset. The latch is reset as soon as V_{CC} drops below 4.5 V (typical value). The internal OVP and OTP will also trigger this latch (see Figure 3).

The detection level of this input is related to the VCC5V pin voltage in the following way: $0.5 \times V_{VCC5V} \pm 4$ %. An internal Zener clamp of 5.6 V will protect this pin from excessive voltages. No internal filtering is done on this input.

7.17 Overtemperature protection

An accurate temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching. When V_{CC} drops to $V_{th(UVLO)}$, capacitor C_{VCC} will be recharged to the $V_{startup}$ level, however the IC will not start switching again. Subsequently, V_{CC} will drop again to the $V_{th(UVLO)}$ level, and so on.

Operation only recommences when the V_{CC} voltage drops below a level of about 4.5 V, in practice this only occurs when the mains input voltage has been disconnected for a short period of time.

7.18 5 V output

Pin 12 can be used for the supply of external circuitry. The maximum output current must be limited to 1 mA. If higher peak currents are required, an external RC combination should limit the current drawn from this pin to 1 mA maximum.

The 5 V output voltage will be available as soon as the start-up voltage is reached. As the high voltage supply cannot supply the VCC5V pin during start-up or shutdown, during latched shutdown (via pin 13 or other latched protection such as OVP or OTP), the voltage is switched to zero.

7.19 Open/not connected CTRL pin protection

If the CTRL pin is open/not connected, a fault condition is assumed and the converter will stop switching. Operation will recommence as soon as the fault condition is removed.

7.20 Soft start-up (pin ISENSE)

To prevent transformer rattle during hiccup, the transformer peak current through the sense resistor, I_{DM}, is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin ISENSE (pin 3) and the sense resistor, R_{sense}. An internal current source charges the capacitor to $V = I_{startup(soft)} \times R_{ss}$, with a maximum of about 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{ss} and C_{ss}.

$$I_{DM} = \frac{V_{sense(max)} - (I_{startup(soft)} \times R_{ss})}{R_{sense}}$$

$$\tau = R_{ss} \times C_{ss}$$

The charging current $I_{startup(soft)}$ will flow as long as the voltage on pin ISENSE is below approximately 0.5 V. If the voltage on pin ISENSE exceeds 0.5 V, the soft start current source will start limiting the current $I_{startup(soft)}$. At the $V_{startup}$ level, the $I_{startup(soft)}$ current source is completely switched off (see Figure 13).

Since the soft start current $I_{startup(soft)}$ is subtracted from pin V_{CC} charging current, the R_{SS} value will affect the V_{CC} charging current level by a maximum of 60 µA (typical value).

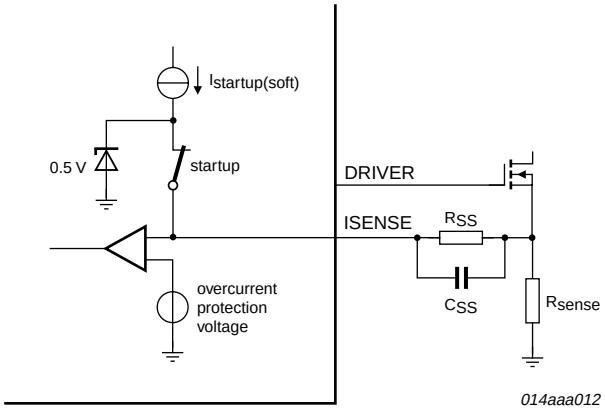


Fig 13. Soft start-up

7.21 Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 170 mA and a current sink capability of typically 700 mA. This permits fast turning on and off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the $\Delta V/\Delta t$ at switch-on. This reduces the Electromagnetic Interference (EMI) and also limits the current spikes across R_{sense}.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 11); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCOADJ}	voltage on pin VCOADJ	input voltage; continuous	–0.4	+5	V
$V_{OVPFCAP}$	voltage on pin OVPFCAP	continuous	–0.4	+7	V
V_{ISENSE}	voltage on pin ISENSE	current limited	–0.4	-	V
V_{DRAIN}	voltage on pin DRAIN		–0.4	+650	V
V_{CC}	supply voltage	continuous	–0.4	+20	V
V_{LOCK}	voltage on pin LOCK	continuous	–0.4	+7	V
V_{CTRL}	voltage on pin CTRL		–0.4	+5	V
V_{CSTART}	voltage on pin CSTART		–0.4	+7	V
V_{DEM}	voltage on pin DEM	current limited	–0.4	-	V
Currents					
I_{ISENSE}	current on pin ISENSE	input current	–1	+10	mA
I_{STDBY}	current on pin STDBY		–1	-	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %	–0.8	+2	A
I_{DRAIN}	current on pin DRAIN		-	+5	mA
$I_{O(VCC5V)}$	output current on pin VCC5V		–1	0	mA
I_{CTRL}	current on pin CTRL		-	+5	mA
I_{DEM}	current on pin DEM		–1.25	+1.25	mA
General					
P_{tot}	total power dissipation	T_{amb} < 70 °C	-	0.7	W
T_{stg}	storage temperature		–55	+150	°C

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 11); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			–20	+145	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
	human body model	pins 1 to 7 and pins 9 to 16	[1]	-	2000	V
		pin 8 (DRAIN)	[1]	-	1500	V
	machine model		[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 11); currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin 8)						
I_{DRAIN}	current on pin DRAIN	input current; V_{CC} = 0 V; V_I on pin DRAIN > 100 V	1.0	1.2	1.4	mA
		with auxiliary supply; V_I on pin DRAIN > 100 V	-	100	300	µA
V_{BR}	breakdown voltage		650	-	-	V
$V_{mains(oper)(en)}$	mains-dependent operation-enabling voltage		60	-	100	V
V_{CC} management (pin 9)						
$V_{startup}$	start-up voltage		10.3	11	11.7	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		8.1	8.7	9.3	V
V_{hys}	hysteresis voltage	$V_{startup}$ - $V_{th(UVLO)}$	2.0	2.3	2.6	V

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 11); currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{ch(high)}$	high charging current	V_I on pin DRAIN > 100 V; V_{CC} < 3 V	–1.2	–1	–0.8	mA
$I_{ch(low)}$	low charging current	V_I on pin DRAIN > 100 V; 3 V < V_{CC} < $V_{th(UVLO)}$	–1.2	–0.75	–0.45	mA
$I_{restart}$	restart current	V_I on pin DRAIN > 100 V; $V_{th(UVLO)}$ < V_{CC} < $V_{startup}$	–650	–550	–450	µA
$I_{CC(oper)}$	operating supply current	no load on pin DRIVER	1.1	1.3	1.5	mA
Demagnetization management (pin 16)						
V_{DEM}	voltage on pin DEM		50	80	110	mV
$V_{CL(neg)}$	negative clamp voltage	voltage on pin DEM, I_I on pin DEM = –500 µA	–0.5	–0.25	–0.05	V
$V_{CL(pos)}$	positive clamp voltage	voltage on pin DEM, I_I on pin DEM = 1 mA	0.5	0.7	0.9	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.1	1.5	1.9	µs
Pulse width modulator						
$t_{on(min)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max)}$	maximum on-time		40	50	60	µs
Oscillator						
$f_{osc(low)}$	low oscillator frequency	V_I on pin CTRL > 1.5 V	20	25	30	kHz
$f_{osc(high)}$	high oscillator frequency	V_I on pin CTRL < 1 V	100	125	150	kHz
$V_{VCO(start)}$	start VCO voltage	peak voltage at pin ISENSE, where frequency reduction starts. See Figure 6 and Figure 8	-	VCO_1	-	mV
$V_{VCO(max)}$	maximum VCO voltage	peak voltage at pin ISENSE, where the frequency is equal to $f_{osc(low)}$	-	VCO_1 – 50	-	mV
Duty cycle control (pin 14)						
$V_{min(\delta max)}$	minimum voltage (maximum duty cycle)		-	1.0	-	V
$V_{max(\delta min)}$	maximum voltage (minimum duty cycle)		-	1.5	-	V
I_{CTRL}	current on pin CTRL	input current, V_I on pin CTRL = 1.5 V	–1 [1]	–0.8	–0.5	µA
5 V output (pin 12)						
$V_{O(VCC5V)}$	output voltage on pin VCC5V	current on pin VCC5V = –1 mA	4.75	5.0	5.25	V
$I_{O(VCC5V)}$	output current on pin VCC5V		–1.0	-	-	mA
LOCK input (pin 13)						

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 11); currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{trip}	trip voltage		2.37	2.5	2.63	V
$V_{VCC(latch)(reset)}$	latch reset voltage on pin V_{CC}	V_{trip} < 2.3 V	-	4.5	-	V
V_{LOCK}/V_{VCC5V}	voltage on pin LOCK to voltage on pin VCC5V ratio	$V_{trip} = 0.5 \times V_{O(VCC5V)}$	–4	-	+4	%
Advanced overpower timing via pin CSTART (pin 15)						
$I_{ch(CSTART)}$	charge current on pin CSTART		–11.5	–10	–8.5	µA
$V_{trip(CSTART)}$	trip voltage on pin CSTART		2.37	2.5	2.63	V
$I_{opp(adv)}$	advanced over-power protection current	V_I on pin SENSE < 0.1 V	–11.5	–10	–8.5	µA
$f_{act(opp)(adv)}$	advanced over-power protection activation frequency	V_I on pin CTRL < 0.5 V and V_I on pin CSTART > 2.5 V	20	25	33	kHz
VCOadj input (pin 1)						
I_{VCOADJ}	current on pin VCOADJ		–11.5	–10	–8.5	µA
Valley switch (pin 8)						
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time		–85	-	+85	V/µs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time		-	150 [1]	-	ns
Current and short winding protection (pin 3)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 0.1 V/µs	0.48	0.52	0.56	V
t_{PD}	propagation delay	$\Delta V/\Delta t$ = 0.5 V/µs	-	140	185	ns
V_{swp}	short-winding protection voltage		0.83	0.88	0.96	V
t_{leb}	leading edge blanking time		300	370	440	ns
$I_{startup(soft)}$	soft startup current	V_I on pin SENSE < 0.5 V	45	60	75	µA
Overvoltage protection (pin 16 and pin 2)						
I_{ovp}	over-voltage protection current	[2]	279	300	321	µA
$I_{ch(OVPFCAP)}$	charge current on pin OVPFCAP	V_I on pin OVPFCAP = 1 V [3]	–36	–32	–28	µA
$I_{dch(OVPFCAP)}$	discharge current on pin OVPFCAP	V_I on pin OVPFCAP = 1 V [3]	52	60	68	µA
$V_{trip(OVPFCAP)}$	trip voltage on pin OVPFCAP		2.37	2.5	2.63	V
$t_{p(OVPFCAP)}$	pulse duration on pin OVPFCAP		2.3	2.8	3.4	µs

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 11); currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{OVPFCAP}$	charge on pin OVPFCAP	charge delivered	[4]	–103	–90	–77	pC
		charge subtracted	[5]	145	170	195	pC
Overpower protection (pin 16)							
$I_{opp(DEM)}$	over-power protection current on pin DEM		[6]	-	–120	-	µA
$I_{opp(red)(DEM)}$	reduced over-power protection current on pin DEM	V_{ISENSE} < 0.3 V	[7]	-	–500	-	µA
STDBY output (pin 4)							
$V_{O(STDBY)}$	output voltage on pin STDBY			4.75	5.0	5.25	V
$I_{source(STDBY)}$	source current on pin STDBY	pin STDBY source current, V_{STDBY} = 1.5 V		–25	–22	–20	µA
$I_{sink(STDBY)}$	sink current on pin STDBY	pin STDBY sink current, V_I on pin STDBY = 1.5 V		2	-	-	mA
Driver (pin 5)							
$I_{source(DRIVER)}$	source current on pin DRIVER	pin DRIVER source current, V_{CC} = 9.5 V; V_I on pin DRIVER = 2 V		-	–170	–88	mA
$I_{sink(DRIVER)}$	sink current on pin DRIVER	pin DRIVER sink current, V_{CC} = 9.5 V; V_I on pin DRIVER = 2 V		-	300	-	mA
		V_{CC} = 9.5 V; V_I on pin DRIVER = 9.5 V		400	700	-	mA
$V_{o(max)}$	maximum output voltage	V_{CC} = 12 V		-	11.5	12	V
Temperature protection							
$T_{pl(max)}$	maximum protection level temperature			130	140	150	°C
$T_{pl(hys)}$	protection level hysteresis temperature			-	8 [1]	-	°C

[1] Guaranteed by design.

[2] Set by the demagnetization resistor, R_{DEM}; see Section 7.9 “Overvoltage protection”.

[3] Set by the OVPFCAP capacitor; see Section 7.9 “Overvoltage protection”.

[4] Value equal to the product of the OVPFCAP current pulse width and the OVP filter timing charge current.

[5] Value equal to the product of the OVPFCAP current pulse width and the OVP filter timing discharge current.

[6] Set by the demagnetization resistor, R_{DEM}; see Section 7.12 “Overpower protection”.

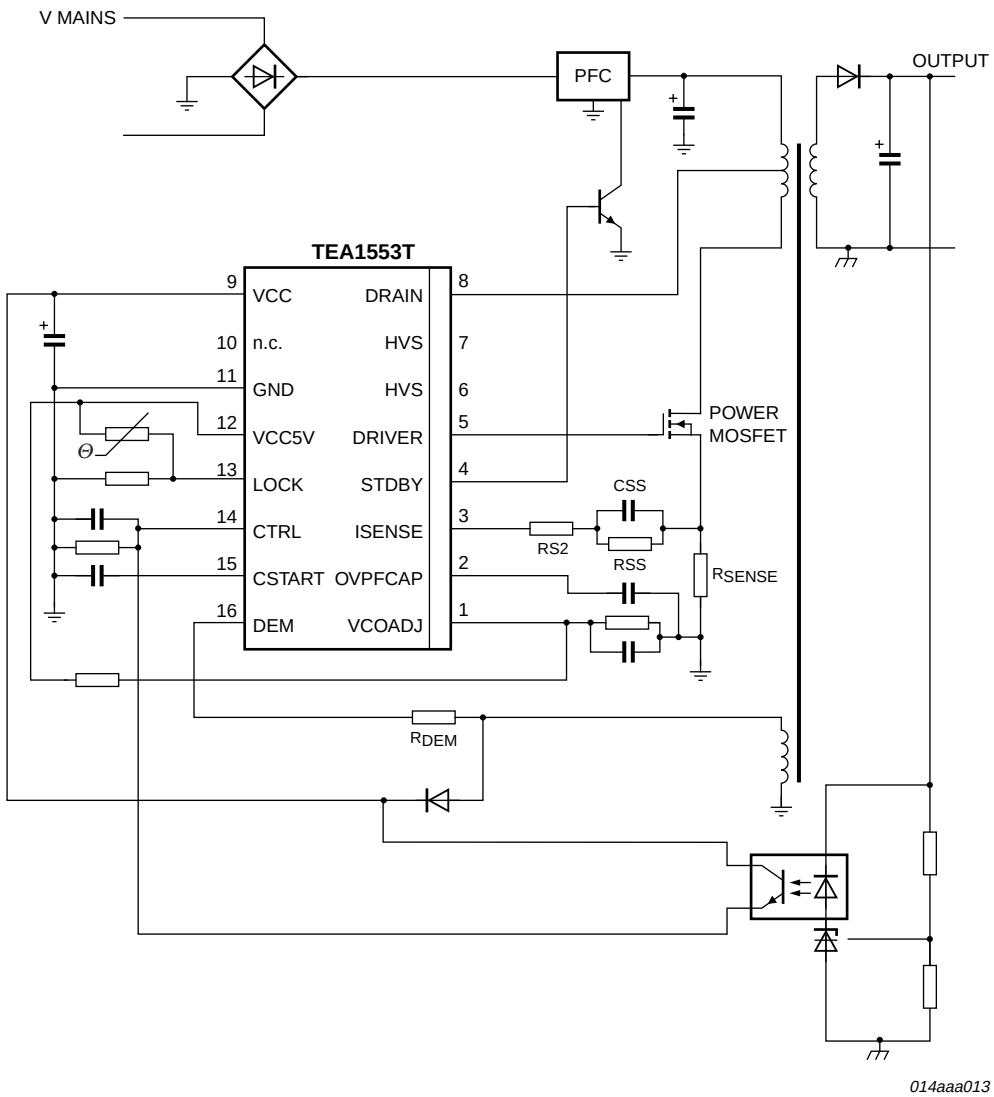
[7] Maximum source voltage is limited to 0.3 V.

11. Application information

A converter using the TEA1553T consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} (at pin 9) buffers the supply voltage of the IC, which is powered via the high voltage rectified mains during start-up and via the auxiliary winding during operation.

A sense resistor converts the primary current into a voltage at pin ISENSE (pin 3). The value of this sense resistor defines the maximum primary peak current.



(1) The LOCK pin is used in this example for an additional external overtemperature protection. If this pin is not used, it must be tied to ground.

Fig 14. Application diagram of TEA1553T with controlled PFC

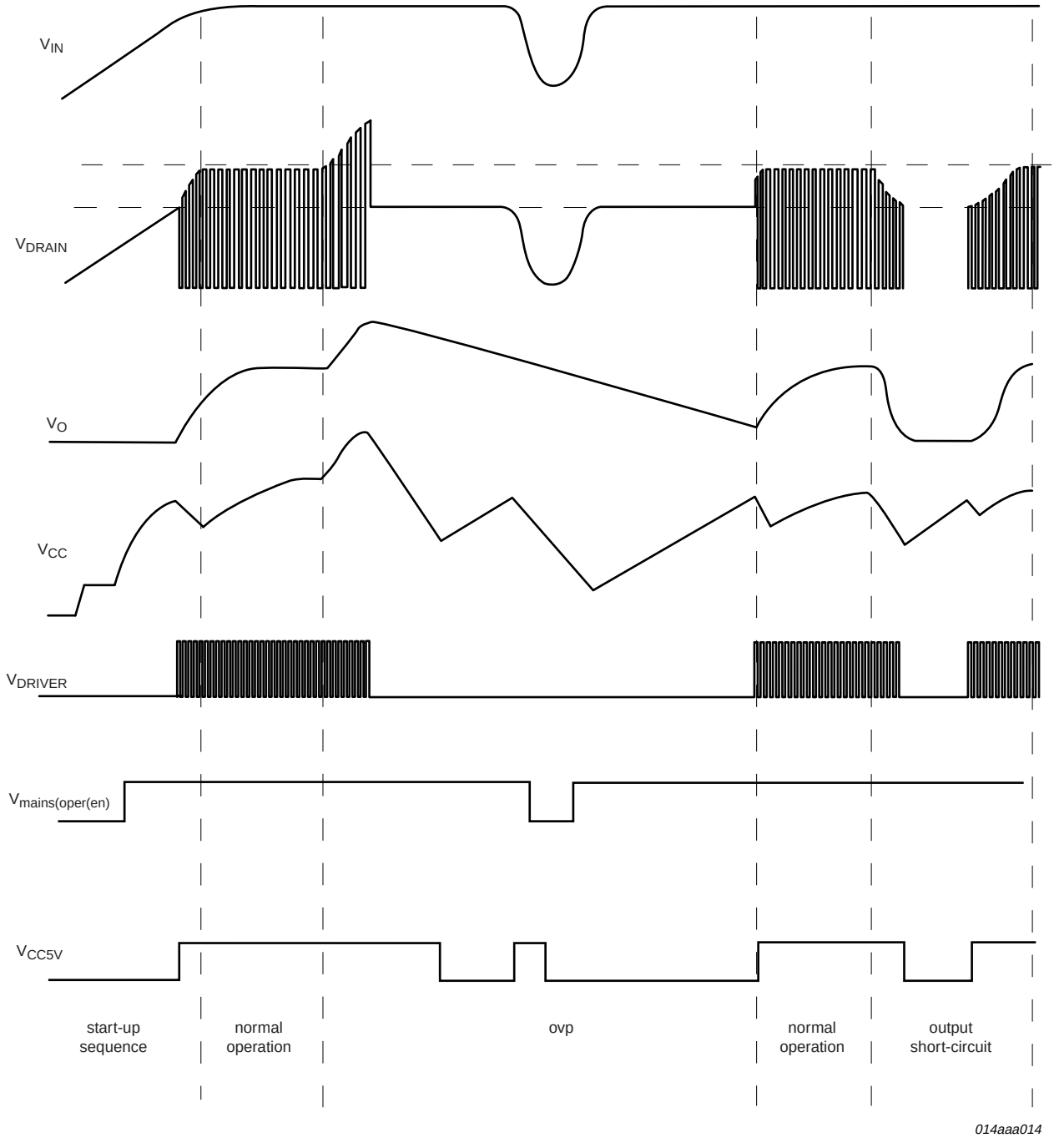
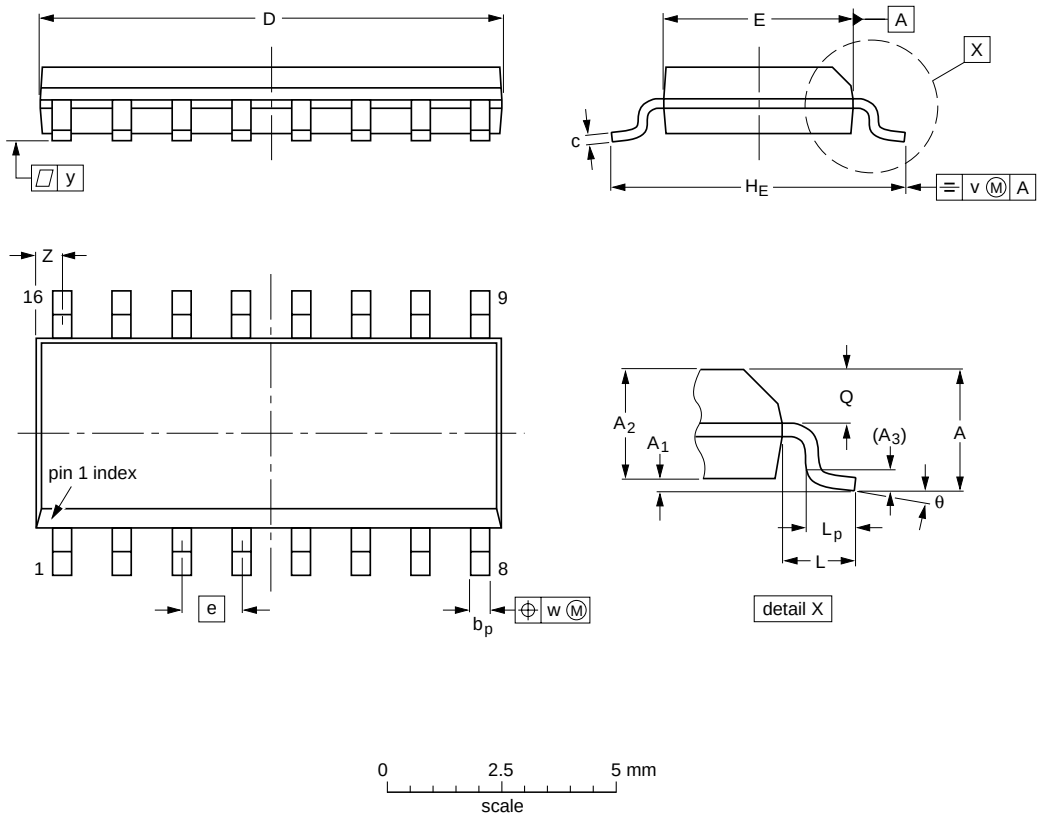


Fig 15. Typical waveforms

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1553T_1	20070703	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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