

BLM2425M7S60P

LDMOS 2-stage power MMIC

Rev. 3 — 9 September 2015

AMMPLION

Product data sheet

1. Product profile

1.1 General description

60W dual path, 2-stage power MMIC transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLM2425M7S60P is designed for high power CW applications and is assembled in a high performance plastic package.

Table 1. Application performance
Per section unless otherwise specified.

Test signal	f	V _{DS}	P _L	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	30	27.5	45

1.2 Features and benefits

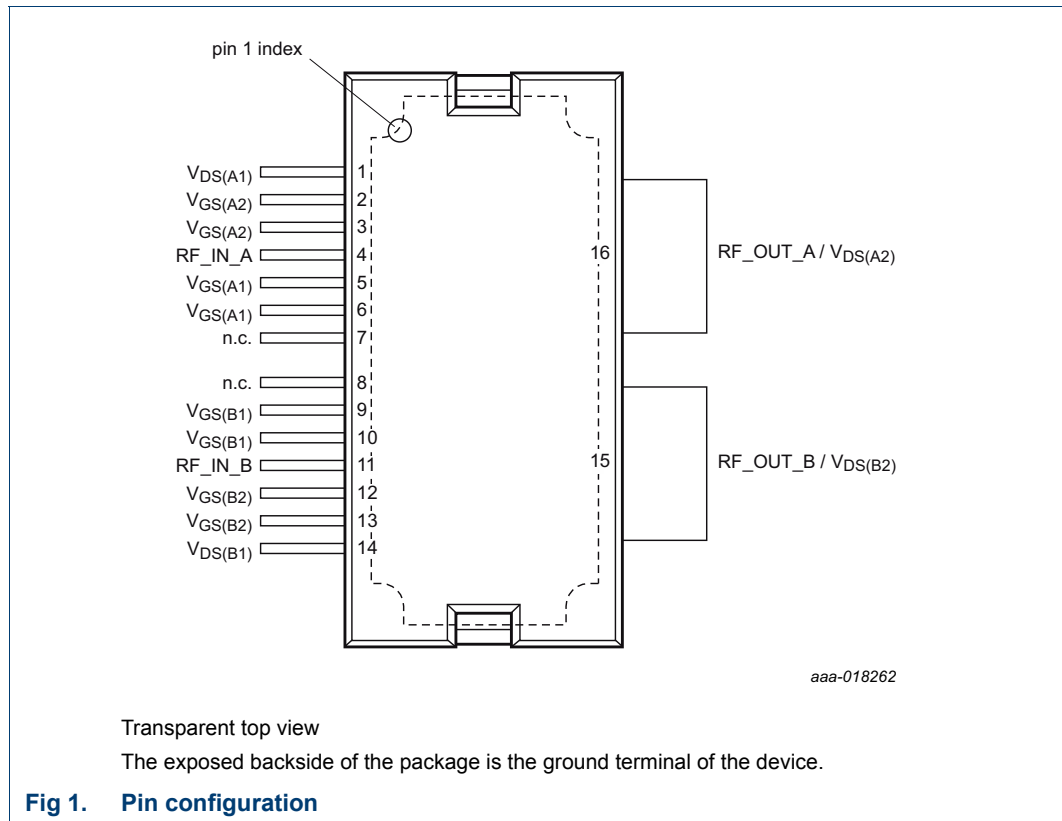
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Biasing of individual stages is externally accessible
- On-chip matching for ease of use
- Designed for broadband operation (frequency 2400 MHz to 2500 MHz)
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

Industrial, scientific and medical applications in the frequency range 2400 MHz to 2500 MHz.

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of stage A1
$V_{GS(A2)}$	2, 3	gate-source voltage of stage A2
RF_IN_A	4	RF input path A
$V_{GS(A1)}$	5, 6	gate-source voltage of stage A1
n.c.	7	not connected
n.c.	8	not connected
$V_{GS(B1)}$	9, 10	gate-source voltage of stage B1
RF_IN_B	11	RF input path of B
$V_{GS(B2)}$	12, 13	gate-source voltage of stage B2
$V_{DS(B1)}$	14	drain-source voltage of stage B1
RF_OUT_B/ $V_{DS(B2)}$	15	RF output path B / drain source voltage of stage B2
RF_OUT_A/ $V_{DS(A2)}$	16	RF output path A / drain source voltage of stage A2
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLM2425M7S60P	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-1

4. Block diagram

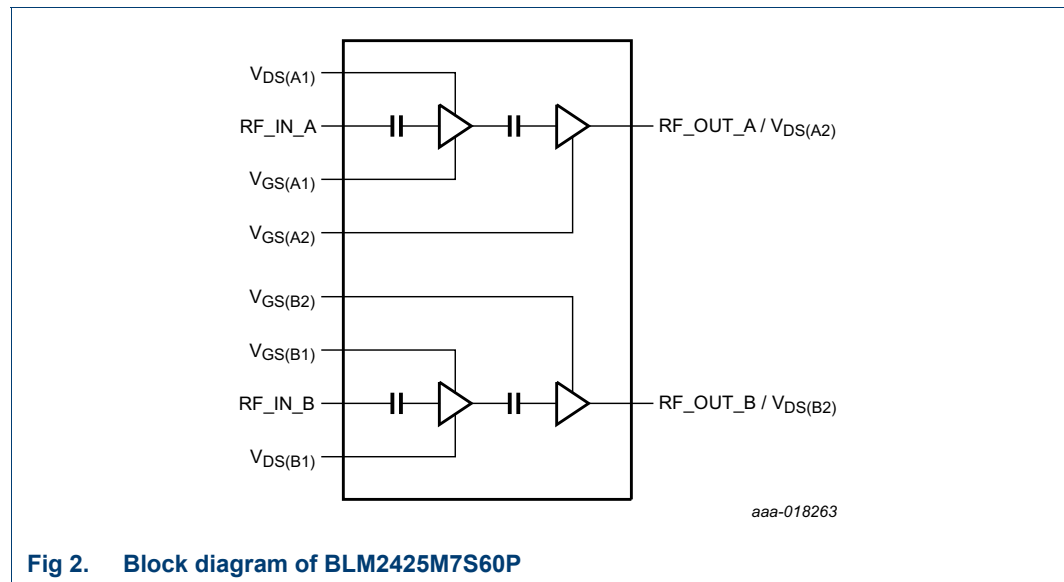


Fig 2. Block diagram of BLM2425M7S60P

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
$V_{GS(sense)}$	sense gate-source voltage		-0.5	+9	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; $T_{case} = 90\text{ °C}$; $P_L = 60\text{ W}$	[1]	0.91 K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics
 $T_{case} = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Final stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.422\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 42\text{ mA}$	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 253\text{ mA}$	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	7.8	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 1478\text{ mA}$	-	2.85	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 1.48\text{ A}$	-	350	-	$\text{m}\Omega$
I_{Dq}	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$; $V_{DS} = 28\text{ V}$	208	233	257	mA
Driver stage						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.116\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 11.6\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 69.6\text{ mA}$	1.7	2.1	2.5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	2.2	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 406\text{ mA}$	-	0.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 0.4\text{ A}$	-	2350	-	$\text{m}\Omega$
I_{Dq}	quiescent drain current	main transistor: $V_{DS} = 28\text{ V}$ sense transistor: $I_D = 7\text{ mA}$; $V_{DS} = 28\text{ V}$	67	75	83	mA

Table 7. RF Characteristics

Test signal: CW at $f = 2450$ MHz; RF performance at $V_{DS} = 32$ V; $I_{Dq1} = 25$ mA; $I_{Dq2} = 50$ mA; $T_{case} = 25$ °C; per section unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 30$ W	26	27.5	-	dB
η_D	drain efficiency	$P_L = 30$ W	41.5	45	-	%
RL_{in}	input return loss	$P_L = 30$ W	-	-18	-13.8	dB

8. Test information

8.1 Ruggedness

The BLM2425M7S60P is capable of withstanding a load mismatch corresponding to $VSWR = 15 : 1$ through all phases under the following conditions: $V_{DS} = 32$ V; $I_{Dq1} = 25$ mA; $I_{Dq2} = 50$ mA; $f = 2450$ MHz; per section unless otherwise specified.

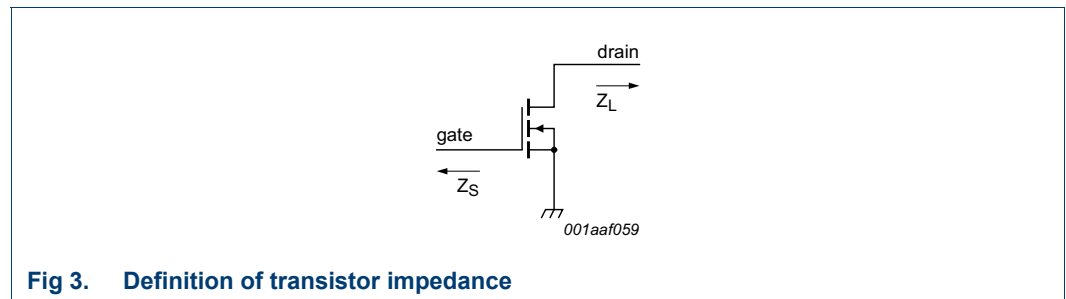
8.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values per section unless otherwise specified.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
2400	$19.1 + j43.2$	$5.3 - j2.4$
2450	$16.8 + j38.8$	$5.0 - j2.3$
2500	$14.4 + j33.0$	$4.4 - j2.4$

[1] Z_S and Z_L defined in [Figure 3](#)



8.3 Test circuit

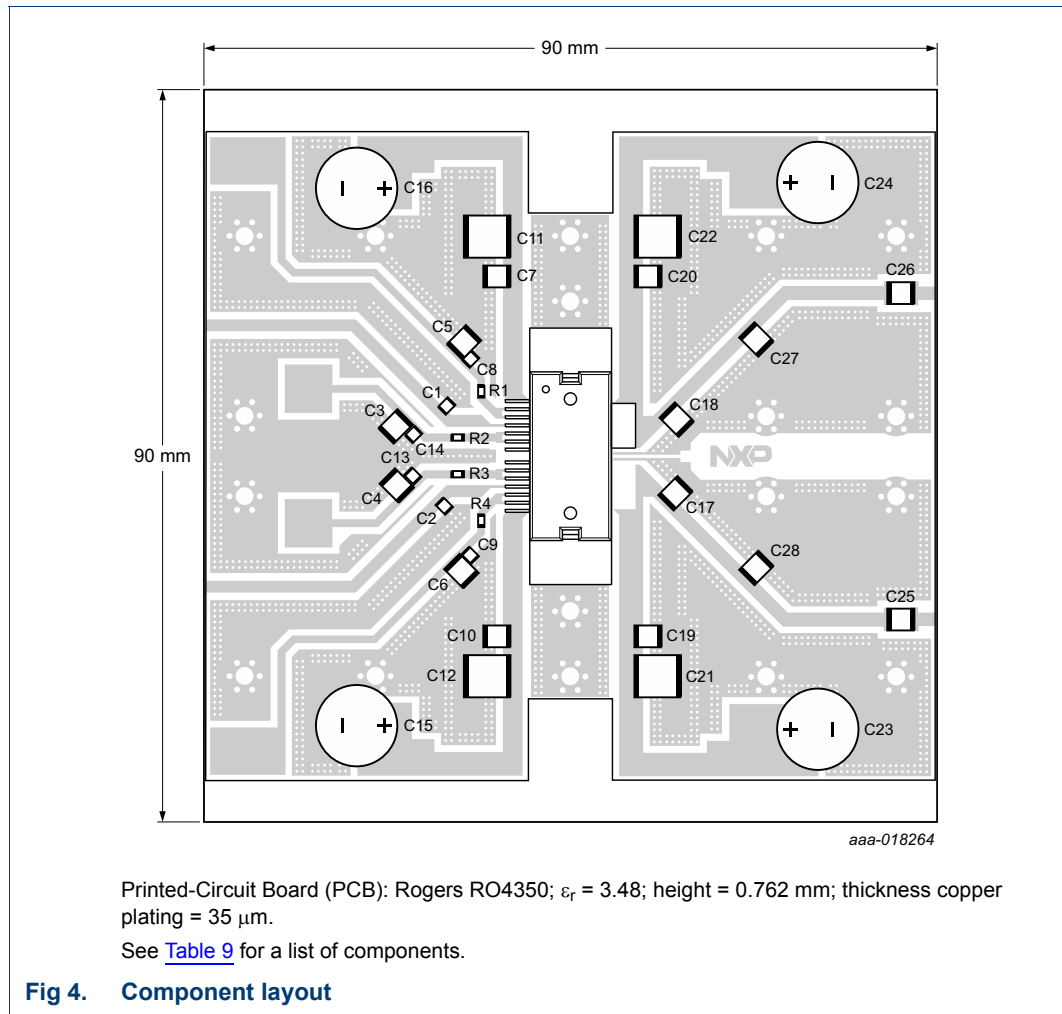


Table 9. List of components

See [Figure 4](#) for component layout.

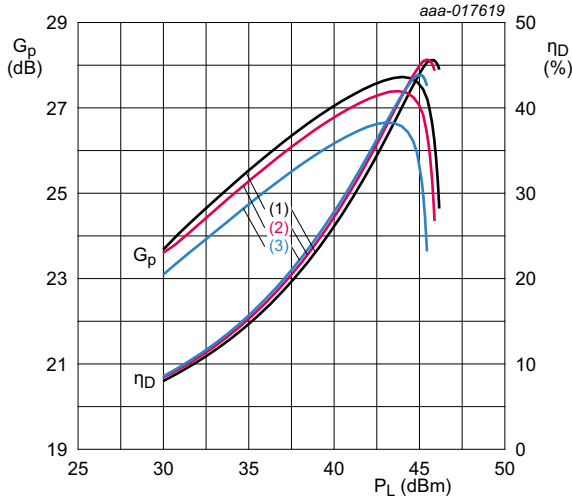
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1 pF [1]	
C3, C4, C5, C6	multilayer ceramic chip capacitor	1 μF , 50 V	Murata: GRM32RR71H105KA01L
C7, C10	multilayer ceramic chip capacitor	8.2 pF [2]	
C8, C9, C13, C14	multilayer ceramic chip capacitor	8.2 pF [1]	
C11, C12, C21, C22	multilayer ceramic chip capacitor	10 μF , 50 V	
C15, C16, C23, C24	electrolytic capacitor	220 μF , 63 V [2]	
C17, C18	multilayer ceramic chip capacitor	1.6 nF [2]	
C19, C20, C25, C26	multilayer ceramic chip capacitor	8.2 pF [2]	
C27, C28	multilayer ceramic chip capacitor	0.4 pF [2]	
R1, R2, R3, R4	SMD resistor	0 Ω	SMD 0805

[1] American Technical Ceramics type 100A or capacitor of same quality

[2] American Technical Ceramics type 100B or capacitor of same quality

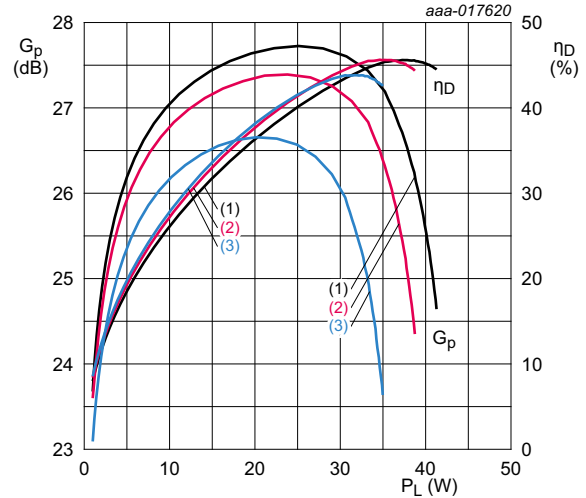
8.4 Graphical data

Performance curves are measured per section.



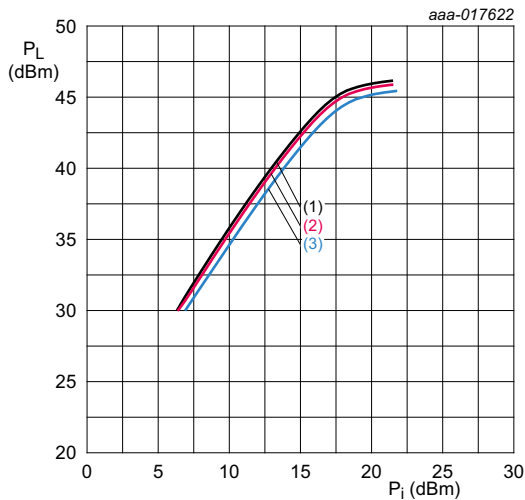
$V_{DS} = 32\text{ V}; I_{Dq1} = 25\text{ mA}; I_{Dq2} = 50\text{ mA}.$
 (1) $f = 2400\text{ MHz}$
 (2) $f = 2450\text{ MHz}$
 (3) $f = 2500\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



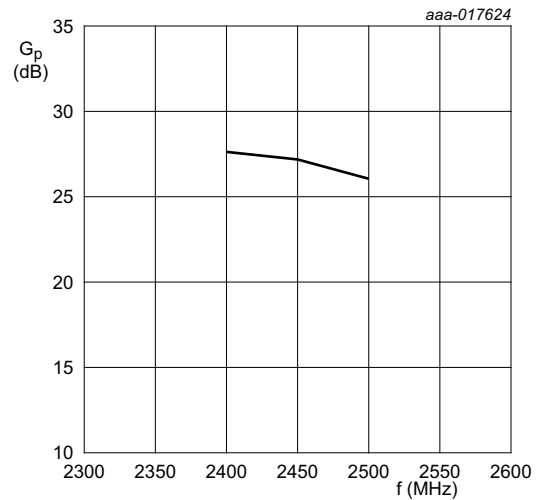
$V_{DS} = 32\text{ V}; I_{Dq1} = 25\text{ mA}; I_{Dq2} = 50\text{ mA}.$
 (1) $f = 2400\text{ MHz}$
 (2) $f = 2450\text{ MHz}$
 (3) $f = 2500\text{ MHz}$

Fig 6. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq1} = 25\text{ mA}; I_{Dq2} = 50\text{ mA}.$
 (1) $f = 2400\text{ MHz}$
 (2) $f = 2450\text{ MHz}$
 (3) $f = 2500\text{ MHz}$

Fig 7. Output power as a function of input power; typical values



$V_{DS} = 32\text{ V}; I_{Dq1} = 25\text{ mA}; I_{Dq2} = 50\text{ mA}; P_L = 30\text{ W}.$

Fig 8. Power gain as a function of frequency; typical values

9. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat)

SOT1211-1

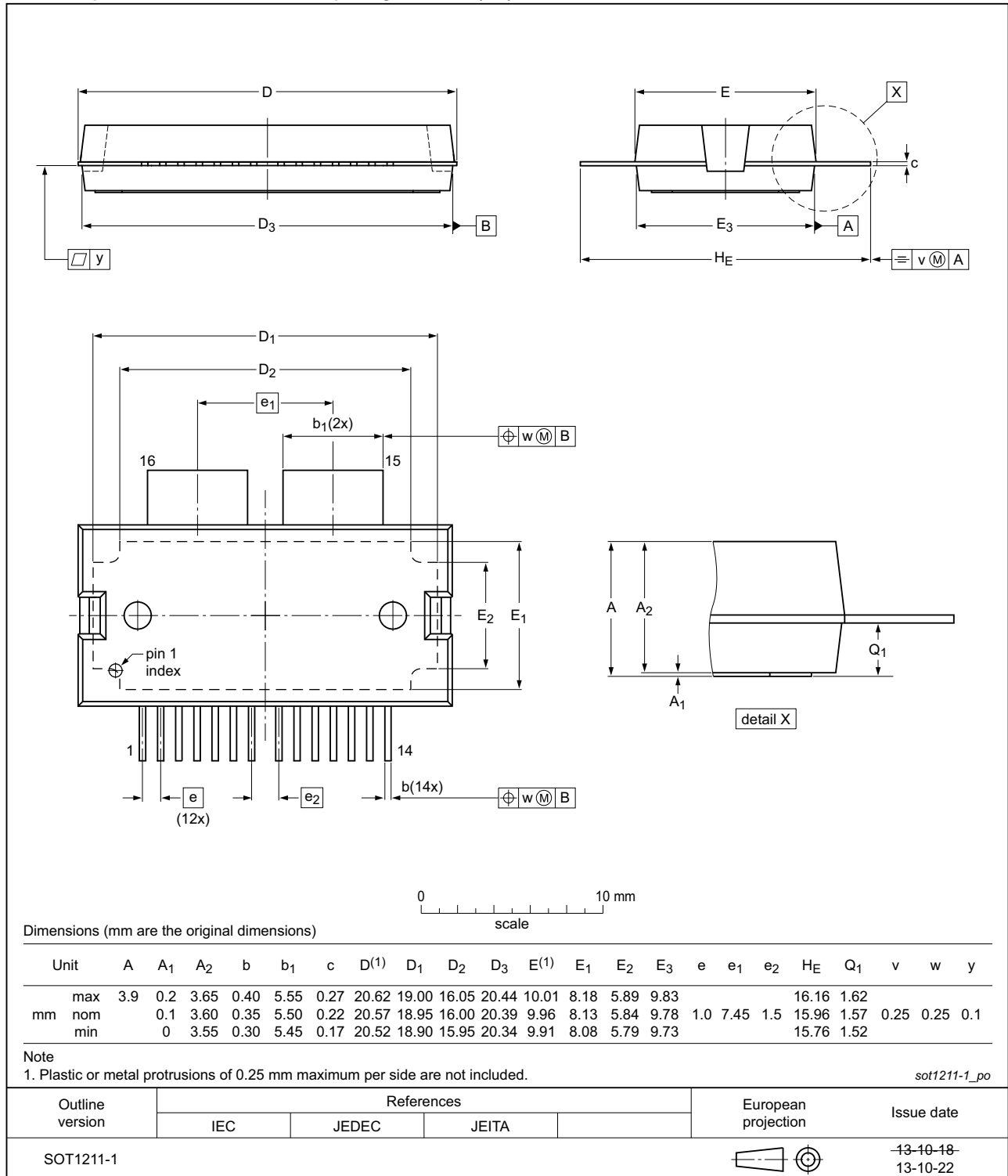


Fig 9. Package outline SOT1211-1 (HSOP16F)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM2425M7S60P v.3	20150909	Product data sheet	-	BLM2425M7S60P#2
Modifications:	<ul style="list-style-type: none"> Table 7 on page 5; table updated 			
BLM2425M7S60P#2	20150901	Objective	-	BLM2425M7S60P v.1
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon Legal texts have been adapted to the new company name where appropriate 			
BLM2425M7S60P v.1	20150518	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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