TDA5230
TDA5231

Universal Low Power ASK/FSK Single Conversion Multi-Channel Image-Reject Receiver with Digital Baseband Processing

Wireless Control Components

Never stop thinking.

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Page prev. version	Page current version	Subjects (changes since previous revision)
all	**all**	Rework of all chapters Product description enhanced by additional short form information Functional description, explanations added, full SFR information in each chapter Reference: some characteristics added, FSK demodulator BW changed to practical measurement method

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Page prev. version	Page current version	Subjects (changes since previous revision)
	4	IF MUX added in **Chapter 1 Product Description**, **Chapter 2.4.8.1 IF Filter**, and **Dual: AIF0 and BIF0: Conf. A IF Buffer Amplifier Enable**
51	**51**	Explanation for T_{ON} and T_{OFF} from **Chapter 2.4.6.2 Constant On/Off Time** to **Chapter 2.4.6.5 Permanent Wake Up Search** improved
125	**127**	Description Digital I/O pins corrected
134	**135**	Reset Value for register CMC0 corrected
	163	Minimum SPM cycletime (T_{ON} +T_{OFF}) specified
4	**4**	AEC Q100 added
	5	Order information added
all	**all**	Spelling corrections

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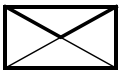


1 Product Description

1.1 Overview

The TDA523x is a family of universal, highly sensitive, low-power single-chip ASK/FSK superheterodyne image-reject-receivers for Manchester-coded data signals in the ISM bands between 302..320 MHz, 433..450 MHz and 865..870 MHz. The chips include fully-integrated digital baseband data processing and produce clean data output via SPI, thus significantly reducing the load on the host processor and standby power consumption.

The TDA523x family of chips offers a high level of integration and needs only few external components for application deployment.

The TDA523x is able to run in several autonomous self-polling and wake-up modes, scanning the received signal for usable data. Interrupts can be initiated based on various criteria, such as the received bit pattern to wake up the host processor. Received data can be scanned for certain message contents (IDs) and is stored in a FIFO data buffer, accessible via the SPI host interface.

The TDA523x is able to scan and receive from different sources with up to two different independent parameter configuration sets. Configurations can differ in modulation ASK/FSK, data rate, wake up criterion, protocol, etc. Additionally, multichannel applications are supported by scanning of up to 3 RF channels in the same band.

The TDA523x is fully programmable to facilitate quick time to market.

1.2 Key Features

- Fully integrated ASK/FSK RF Data Receiver with data FIFO and SPI host interface
- High input sensitivity: e.g. typically -108dBm at 2kbit data rate (see **Specifications**)
- Autonomous wake-up and Self-Polling features allow different modulation for wake-up and data
- Two parallel parameter sets for scanning and receiving from different sources
- Reduces significantly host processing power, system standby power consumption
- Fully integrated Multichannel PLL Synthesizer support up to 17 sub-channels
- Image Reject mixer prevents interferences on mirror frequency
- IF Filter Multiplexer allows IF bandwidth switching
- IF-Limiting Amplifier with RSSI-Output accessible via dedicated pin or register
- Data Framer with versatile Frame Synchronization capability
- Message Contents (ID) scanning
- Unique Serial-Number, accessible via SPI
- Crystal-Oscillator with on chip Fine-Tuning, Clock-Output with configurable Prescaler
- Supply Voltage Range 3.0 V to 3.6 V and 4.5 V to 5.5 V
- Package PG-TSSOP-28-1
- Operating Temperature Range -40 to +105°C
- Qualified according automotive AEC-Q100
- Evaluation boards, reference designs, and free PC configuration and evaluation tools available

1.3 Applications

- Tire Pressure Monitoring Systems
- Remote Keyless Entry Systems
- Remote Control Systems

1.4 Order Information

Type	Ordering Code	Package
TDA5230	Q62705K 791	PG-TSSOP28-1
TDA5231	SP000202847	PG-TSSOP28-1

1.5 Target Application Frequencies for TDA5230 and TDA5231

The TDA523x family of receivers cover a wide range of commonly used receive frequencies within the three major ISM-bands used in TPMS, RKE/PKE and remote control system applications.

The TDA5230 covers operation in the 433..450 MHz and 865..868 MHz ISM bands. The TDA5231 covers complementary operation in the 302..320 MHz ISM-band.

Figure 1 identifies the capabilities of the TDA5230 and TDA5231 within the three different frequency bands.

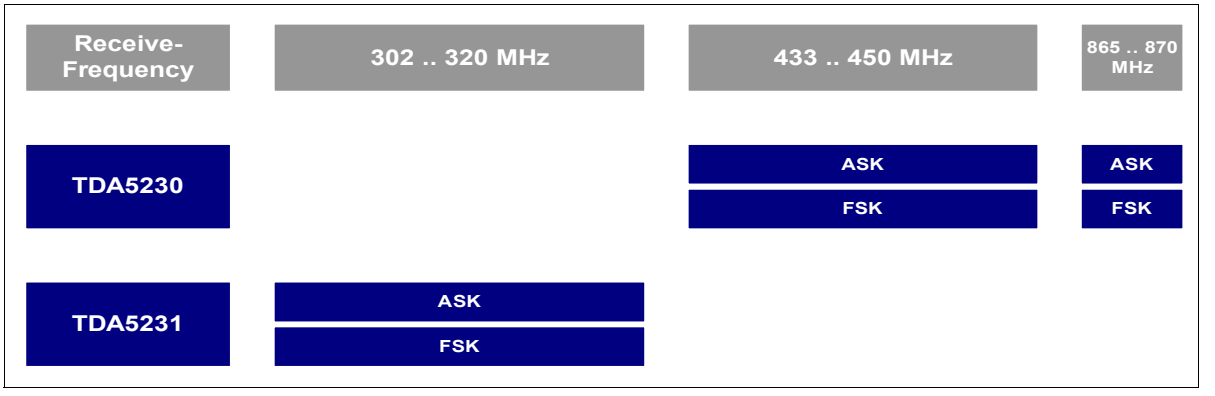


Figure 1 Application Frequencies for TDA5230 and TDA5231

Color underlayed text within this document highlights differences in the operation between the TDA5230 (Lo-Side LO-Injection) and TDA5231 (Hi-Side LO-Injection).

1.6 Major Key-Features of TDA5230 and TDA5231

1.6.1 Typical Application Circuit

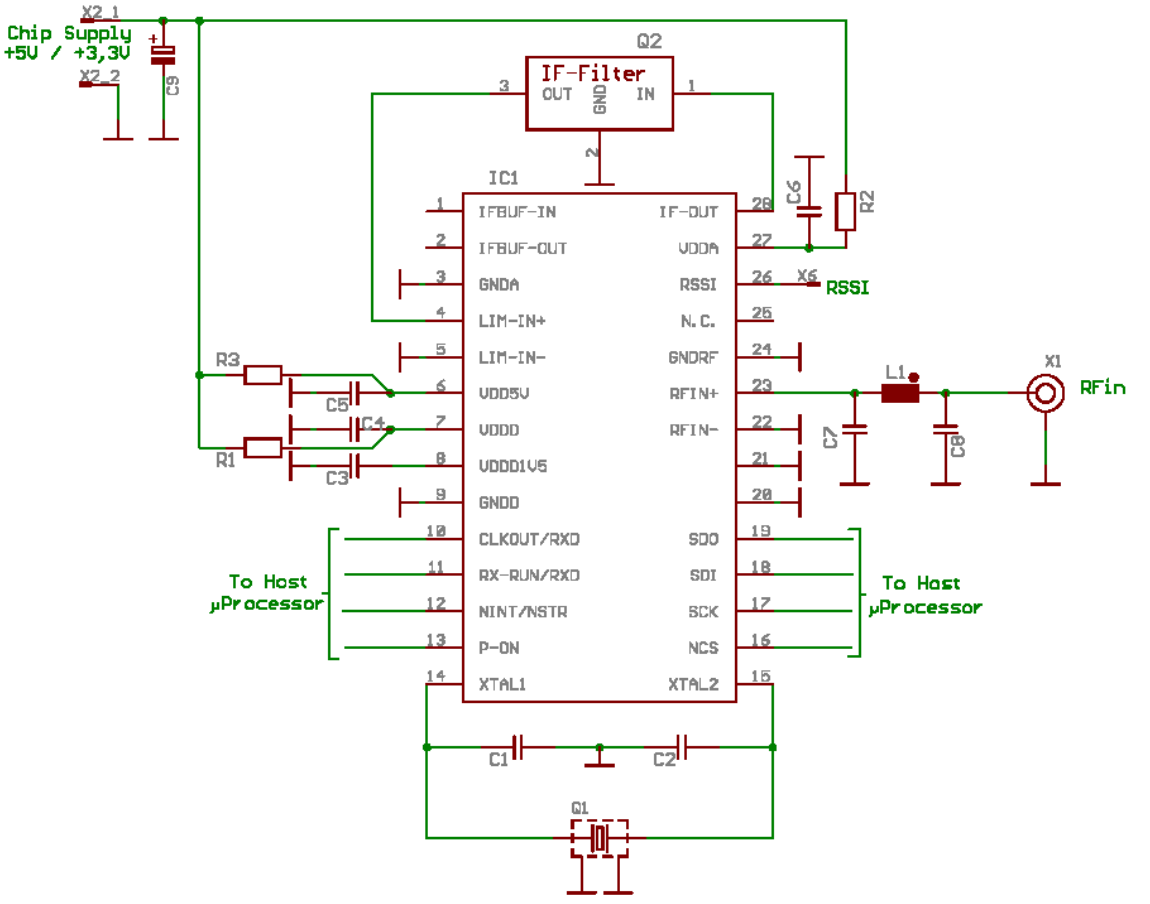


Figure 2 Typical Application Circuit

The TDA523x requires only view external components.

In noise and EMC sensitive applications usage of an input SAW filter plus additional matching circuitry is recommended.

1.6.2 Baseband Processing

TDA523x has integrated all means to process incoming ASK or FSK modulated Manchester-coded bit streams, and convert them into pure data, which can be read out via SPI by the host processor.

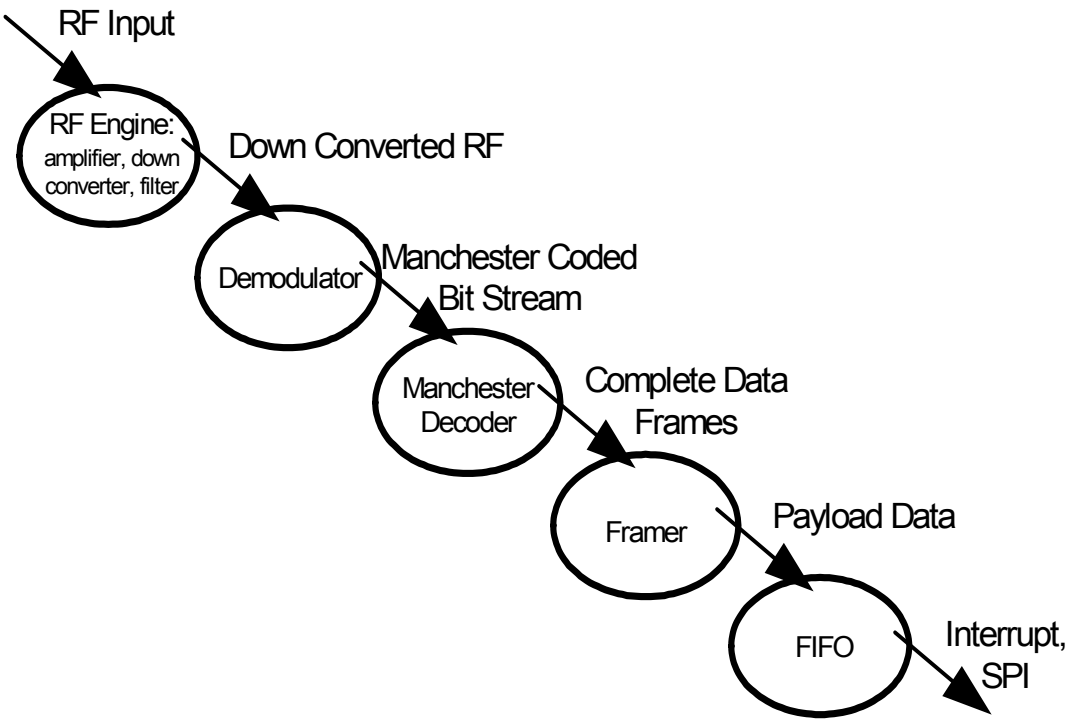


Figure 3 Internal Data Processing Flow

The Manchester-coded bit stream is decoded by the Manchester Decoder into a bit stream containing the wake-up pattern, the TSI (Telegram Start Identifier) and the payload. The Framer separates the payload and stores it in the FIFO. An interrupt is generated and data can be read from the FIFO by the host processor via SPI.

1.6.3 Autonomous Self Polling

The TDA523x offers a fully autonomous Self Polling Mode, in which the RF input signal is scanned for valid data signals base on programmable timing. The host processor is not burdened with this task, so its full processing power is available for other tasks, or the host processor may stay in a power save, or sleep mode. When valid data has been

received, the host processor is alerted by an interrupt, and the data payload is available from the FIFO. Invalid signals are ignored.

The TDA523x offers different programmable scanning modes, and criteria to identify valid wake up patterns, TSIs, and payloads.

Selectable Wake-Up Criteria include detection of a valid data rate, a random Manchester-coded pattern, a chain of equal Manchester-coded bits, or a specific pattern.

Before initiating an interrupt also the TSI must match up to a programmed pattern; optionally the data stream may be scanned for up to 16 bytes of a Message Identifier.

1.6.4 Two Independent Receiver Configuration Sets

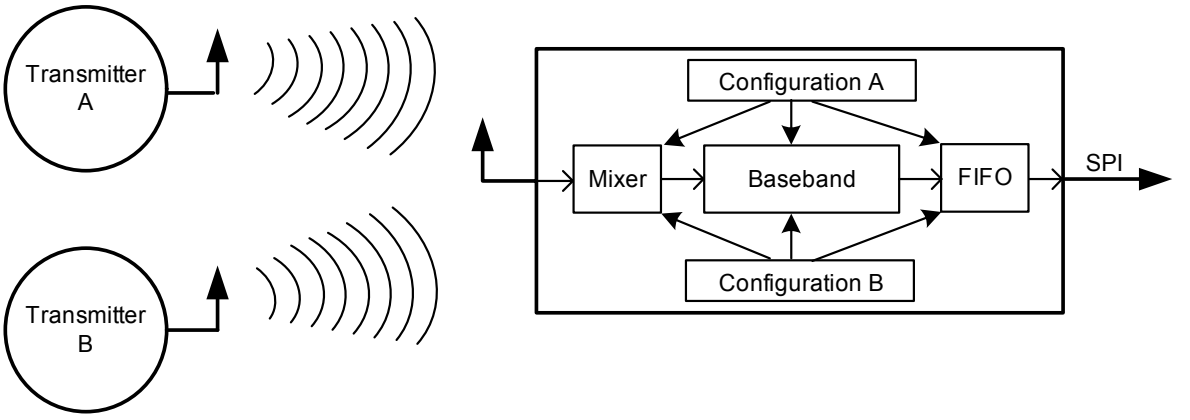


Figure 4 TDA523x Two Independent Receiver Configurations (simplified)

TDA523x has two switchable register sets, allowing scans based on up to two different configurations from different transmitters. Transmissions may differ in sub-channel, modulation, wake-up criterion, data rate, TSI, message identifier, packet length, etc.

In Self Polling Mode configurations are switched autonomously; in Slave Mode, configurations are switched by changing a single register bit.

1.6.5 Multi-Channel PLL Receiver Supports up to 17 Subchannels

TDA523x supports up to 17 subchannels: 1 center channel, 8 channels above, and 8 channels below the center channel frequency. The frequencies for the channels are fixed and depend on the system frequency and the selected band. Additional information is provided in chapter **“RF-PLL Synthesizer” on Page 28**.

In Self Polling Mode up to 3 Channels per Receiver Configuration may be scanned automatically.

1.6.6 Support Software and Evaluation Boards

The TDA523x includes free downloadable support software.

1.6.6.1 The IAF TDA523x Configuration Tool

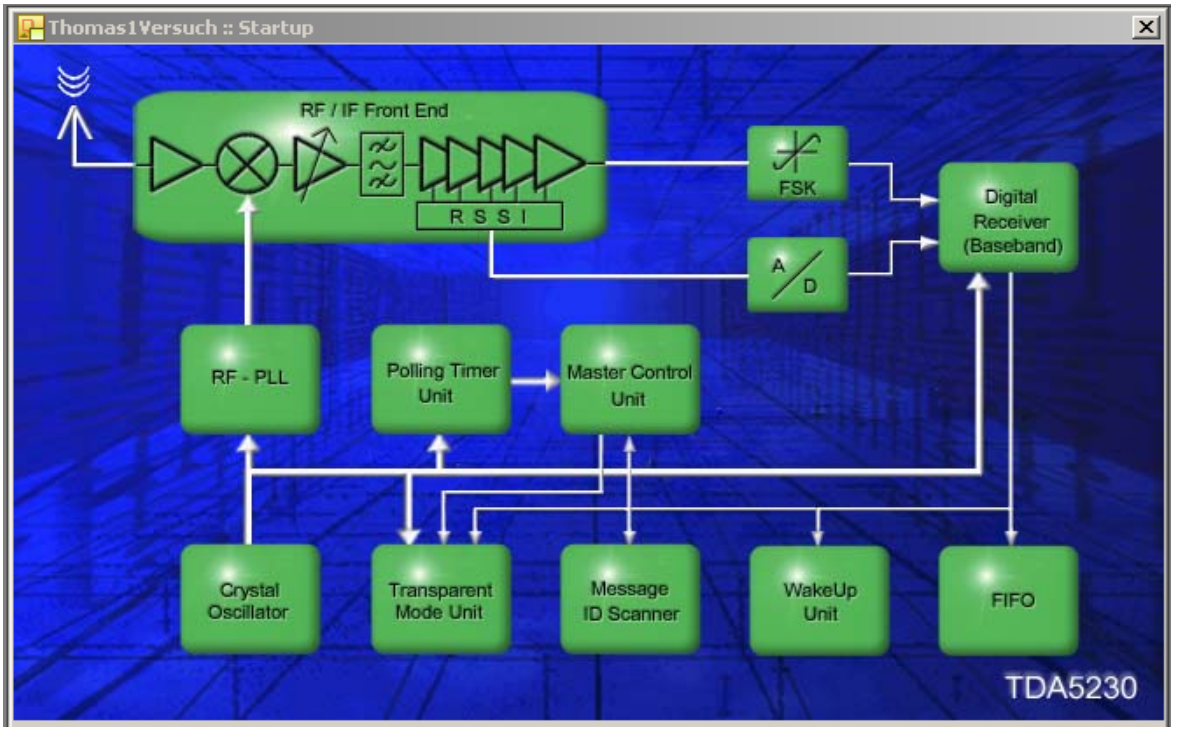


Figure 5 IAF TDA523x Configuration Tool

The IAF TDA523x Configuration Tool offers simple configuration of all register settings. The resulting configuration file may be directly used and downloaded with the TDA523x Explorer or the configuration content may be copied into the target application software.

1.6.6.2 The TDA523x Explorer

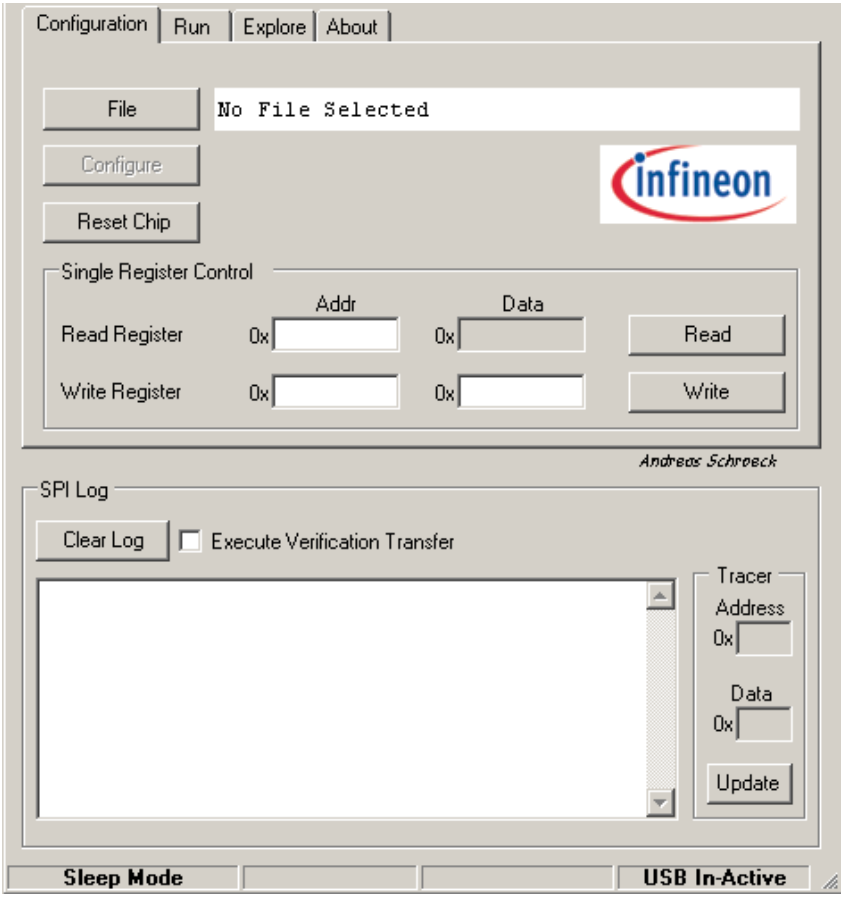


Figure 6 TDA523x Explorer

The TDA523x Explorer works with the TDA523x Evaluation Boards. It allows application solutions to be created and checked via a USB connection from a standard PC. The Explorer allows the user to write registers, read out the data FIFO and related registers.

1.6.6.3 Evaluation Boards

Various Evaluation Boards are available or in development.

All Evaluation Boards have a USB interface to connect to a standard PC and are supported by the TDA523x Explorer.

2 Functional Description

2.1 Pin Configuration

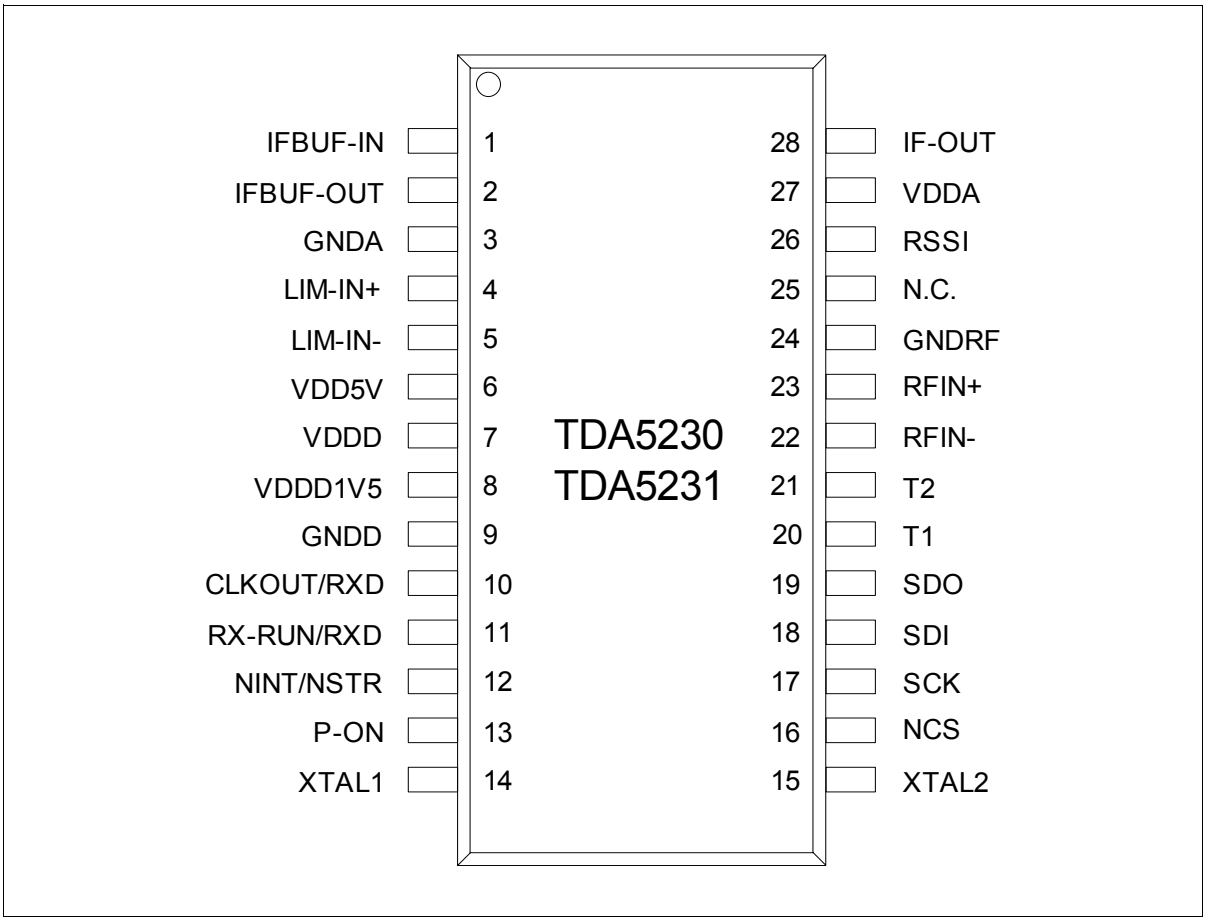
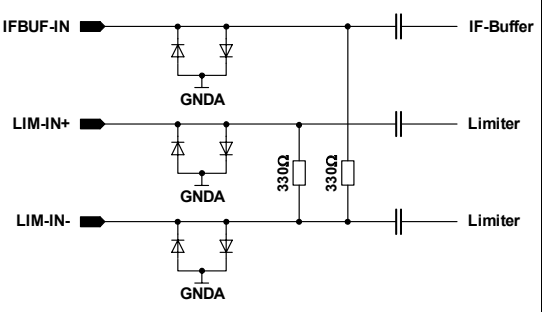
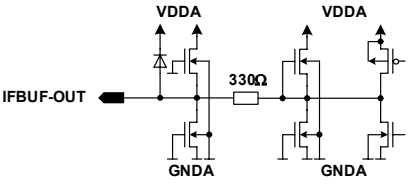
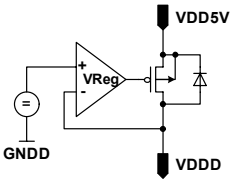
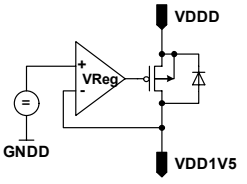
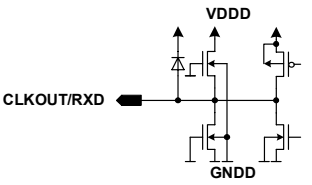
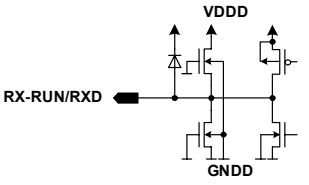
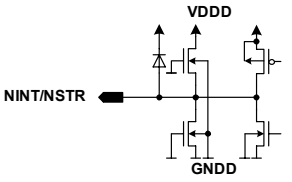
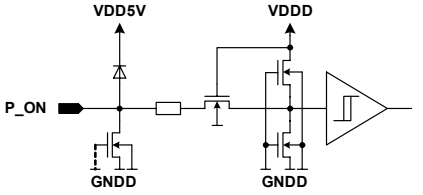
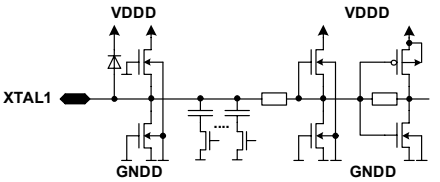
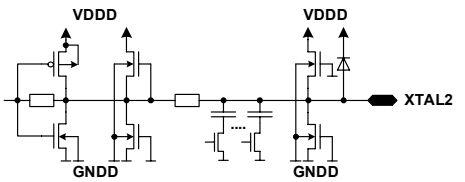


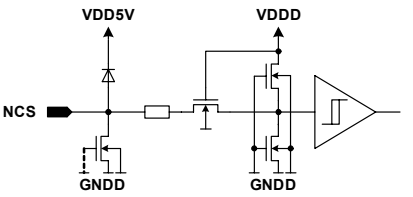
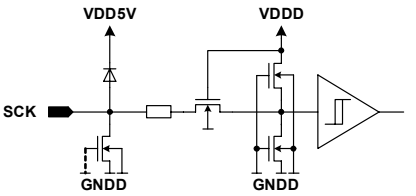
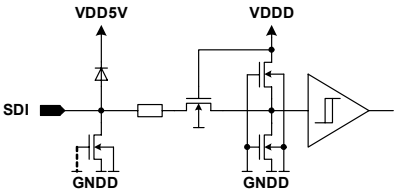
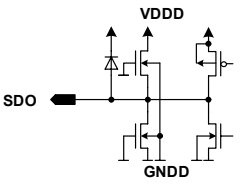
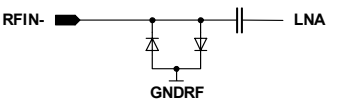
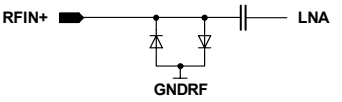
Figure 7 Pin Configuration

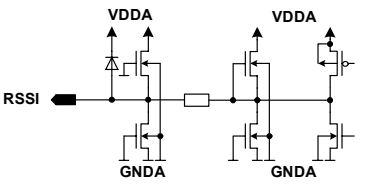
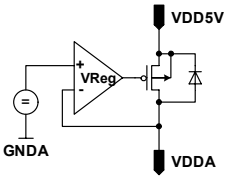
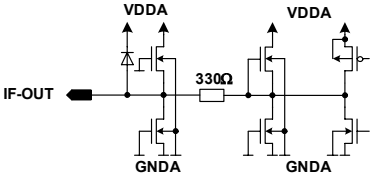
2.2 Pin Definition and Functions

Table 1 Pin Definition and Function

Pin No.	Symbol		Function
1	IFBUF-IN		Input of IF Buffer Amplifier
2	IFBUF-OUT		Output of IF Buffer Amplifier
3	GNDA		Analog Ground
4	LIM-IN+	see schematic of Pin 1	IF Limiter Input
5	LIM-IN-	see schematic of Pin 1	Complementary IF Limiter Input
6	VDD5V		Supply 5 V
7	VDDD		Digital Supply 3.3 V
8	VDDD1V5		Digital Supply 1.5 V
9	GNDD		Digital Ground

Pin No.	Symbol		Function
10	CLKOUT/RXD		Programmable Clock Output and alternative RX Data Output
11	RX-RUN/RXD		Run Mode Output signal and alternative RX Data Output
12	NINT/NSTR		Interrupt Output and alternative RX Data Strobe Output
13	P-ON		Power On
14	XTAL1		Crystal Oscillator
15	XTAL2		Crystal Oscillator

Pin No.	Symbol		Function
16	NCS		SPI Chip Select
17	SCK		SPI Clock
18	SDI		SPI Serial Data Input
19	SDO		SPI Serial Data Output
20	T1		Connect to Digital Ground
21	T2		Connect to RF Ground
22	RFIN-		Complementary LNA Input
23	RFIN+		LNA Input
24	GNDRF		RF Ground
25	N.C.		Do not connect

Pin No.	Symbol		Function
26	RSSI		RSSI Output
27	VDDA		Analog Supply 3.3 V
28	IF-OUT		Mixer IF Output

2.3 Functional Block Diagram

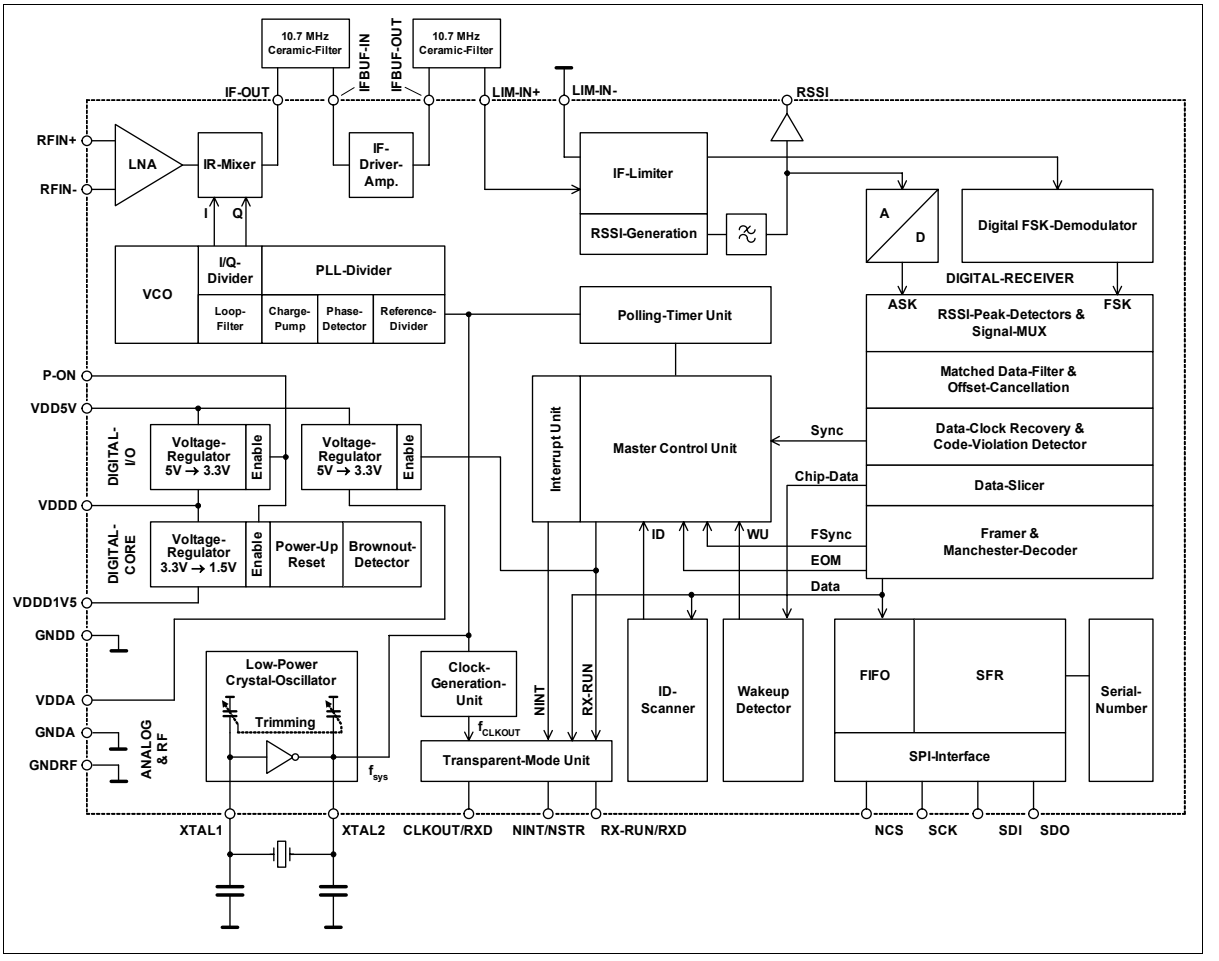


Figure 8 Functional Block Diagram

2.4 Functional Block Description

The RF frontend of the chip contains an LNA followed by an Image Reject Mixer that converts the incoming RF-signal down to IF with adjustable gain from RFIN to IF-OUT. Channel selection is achieved by up to two external ceramic IF filters, which narrow the channel bandwidth. The multistage amplifier performs the limitation of the IF signal and generation of the RSSI signal. The limited IF signal at its output drives the input of the digital FSK Demodulator. The gain and offset of the generated RSSI signal can be digitally adjusted. An A/D converter acts as an interface from the analog RSSI signal path to the Digital Receiver.

The Digital Receiver performs data filtering, offset cancellation and Manchester decoding of the received signals after they are demodulated. The chip also offers a

flexible and configurable frame synchronisation and Message ID scanning feature, supported by special function registers. Received data of an accepted message is stored in a FIFO and can be read out via the SPI interface.

A master control unit (MCU), implemented as a finite state machine and a Polling Timer Unit control all actions of the device and can be configured via Special Function Registers (SFRs). Various self-polling modes can be set up to achieve a maximum of autonomous receiver operation. The Transparent Mode Unit defines the functionality of the pins CLKOUT/RXD, NINT/NSTR and RX-RUN/RXD.

A fully integrated multi-channel PLLdrives the LO ports of the Image-Reject-Mixer. Within a selected operational frequency band multiple channels are accessible by utilizing the same reference crystal-frequency. The reference clock of the PLL and the digital section are provided by a pierce type crystal oscillator that offers on chip fine-tuning to trim out crystal tolerances. A programmable Clock Generation Unit divides the system clock by a programmable ratio and drives the CLKOUT/RXD pin.

On chip voltage regulators generate the required internal supply voltages and allow the IC to be operated at supply voltages between 3 V to 3.6 V and 4.5 V to 5.5 V. The digital supply of the chip is monitored by a brown out detector and is equipped with a built-in reset generator. Every device contains a unique serial number, which can be read out via the SPI Interface.

Special Function Register and Control Bit Symbols

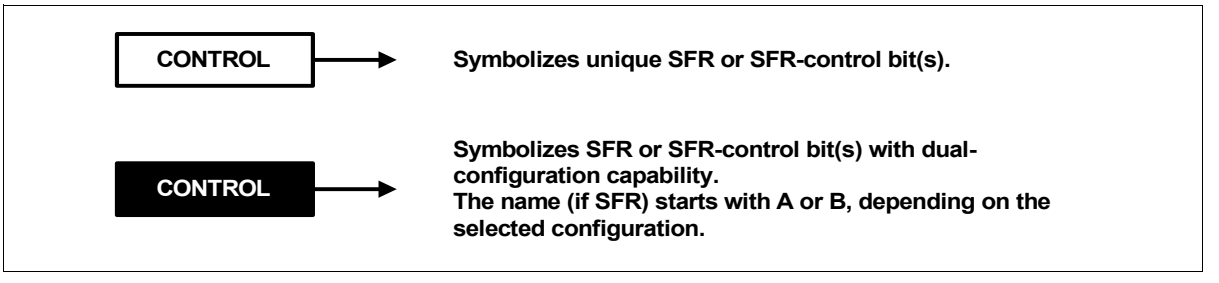


Figure 9 SFR Symbolism

The register names, addresses, and control bits for each function are listed in a table at the end of this section. Functional descriptions of all registers are provided in **Chapter 3 Register Descriptions**.

2.4.1 Power Supply

The chip may be operated within a 5 V or a 3.3 V environment.

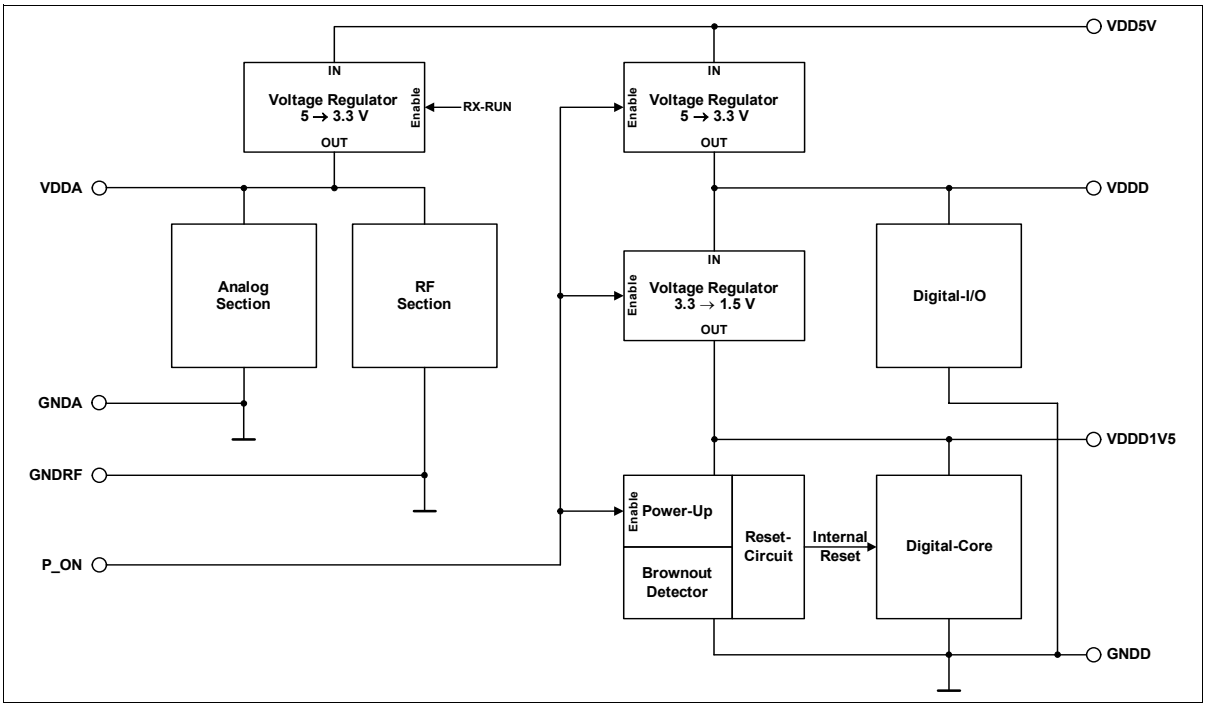


Figure 10 Power Supply

For operation within a 5 V environment, the chip is supplied via the pin VDD5V. In this configuration a 5 to 3.3 V voltage regulator supplies the analog/RF-section (only active in Run Modes) and a second 5 to 3.3 V voltage regulator supplies the digital I/O-pads.

When operating within a 3.3 V environment, the pins VDD5V, VDDA and VDDD must be supplied. The 5 to 3.3 V voltage regulators are inactive in this configuration.

The internal digital core is supplied by an additional 3.3 to 1.5 V regulator.

The regulators for the digital section are controlled by the signal at the P_ON (Power On). A low signal at P_ON disables all regulators and sets the IC into Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF-section is active (RX-RUN = high).

P_ON can be used to initiate a reset. The required negative pulse time t_{P_ON} is specified in **Chapter 4 Specifications**.

To provide data integrity within the digital units, a brown out detector monitors the digital supply and a detected voltage drop of VDDD below approximately 2.45 V initiates a reset.

Figure 11 illustrates a typical power supply application for a 3.3 V and a 5 V environment.

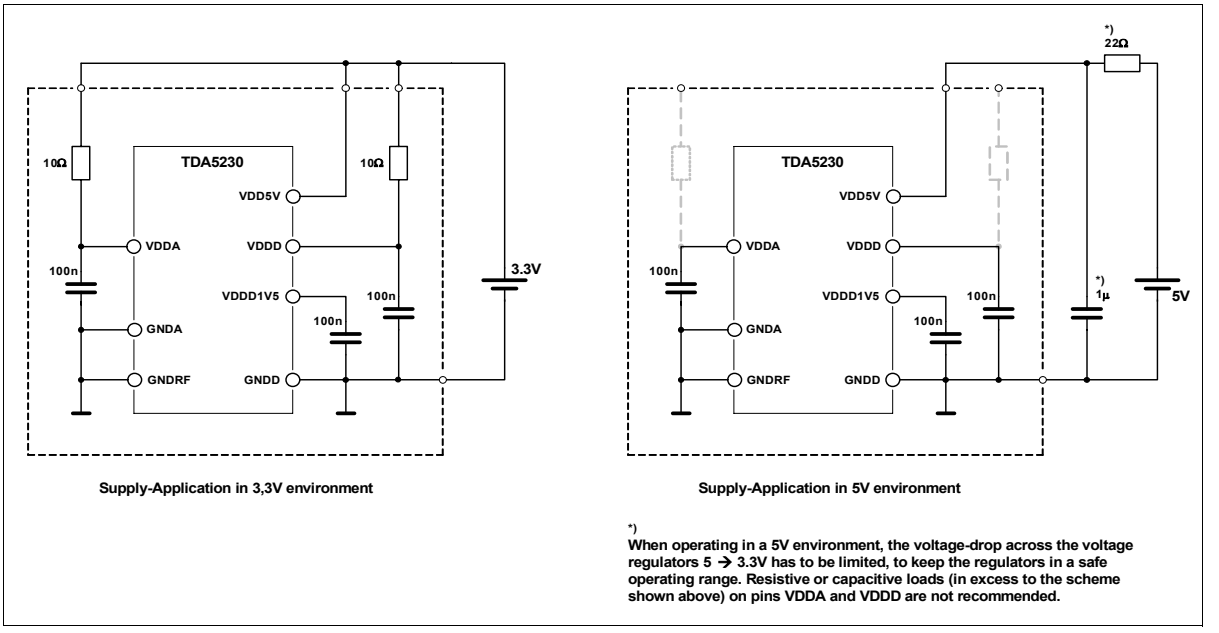


Figure 11 Supply Modes

2.4.1.1 Supply Current

In Sleep Mode, the Master Control Unit switches the crystal oscillator into Low Power Mode (all internal load capacitors are disconnected) to minimize power consumption.

Whenever the chip leaves the Sleep Mode (t_1), the crystal oscillator resumes operation in High Precision Mode and requires $t_{COSCsettle}$ to settle at the trimmed frequency. At t_2 the analog signal path (RF and IF section) and the RF-PLL are activated. At t_3 the chip is ready to receive data. The chip requires $t_{RXstartup}$ from leaving Sleep Mode and until the receiver is ready to receive data.

A transient supply current peak may occur at t_1, depending on the selected trimming capacitance. The average supply current drawn between during $t_{RFstartupdelay}$ is $I_{VDDsleep,high}$.

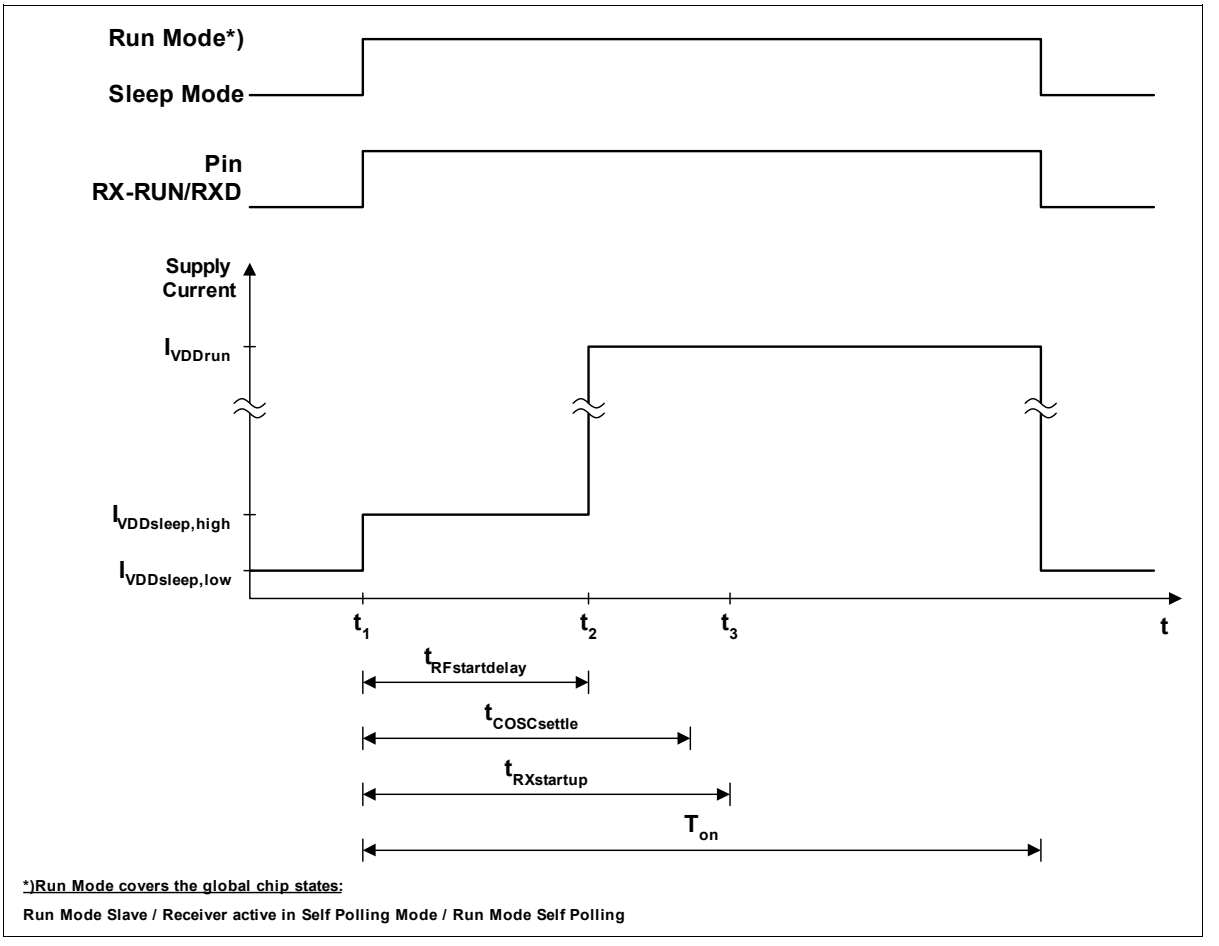


Figure 12 Supply Current Ramp Up/Down

If the IF buffer amplifier or the clock-generation feature (CLKOUT/RXD pin active) is activated, the respective currents must be added.

2.4.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A low at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high at the P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

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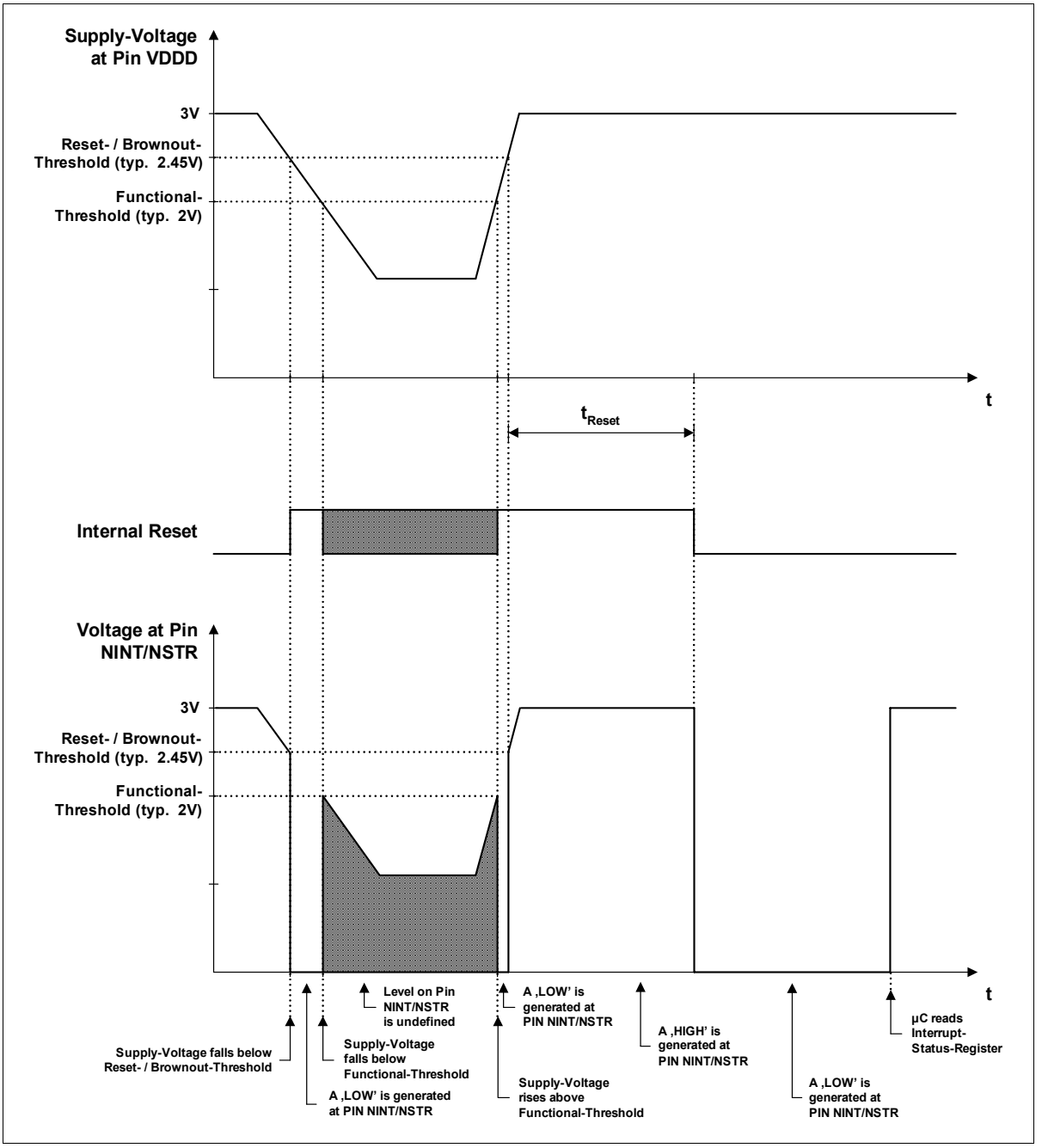

Figure 13 Reset Behavior

A second source that can trigger a reset is a brown out event. Whenever the integrated brown out detector measures a voltage drop below the brown-out threshold on the digital supply, the integrity of the stored data and configuration can no longer be guaranteed; thus, a reset is generated. While the supply voltage stays between the brown out and the functional threshold of the chip, the NINT/NSTR pin is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins (e.g. NINT/NSTR) are undefined.

When the supply voltage rises above the brown out threshold, the IC generates a high pulse at NINT/NSTR and remains in the reset state for the duration of t_{Reset}. When the IC leaves the reset state, the Interrupt Status register (IS) is set to FF_{hex} and the NINT/NSTR pin is forced to low. Now, the IC starts operation in the Sleep Mode, ready to receive commands via the SPI interface. The NINT/NSTR pin will go high, when the Interrupt Status register is read the first time.

2.4.3 System Clock

2.4.3.1 Crystal Oscillator

The reference clock for the Digital and the RF Section is generated by a pierce-type crystal oscillator. Adjustable internal load capacitors are provided that allow the tolerances of the crystal, external load capacitors and the IC itself to be trimmed out. These capacitors are built of binary weighted C-banks and are connected in parallel to the external load capacitors. The internal capacitors are controlled by the crystal oscillator calibration data register (XTALCAL). An automatic amplitude regulation allows the oscillator to operate with minimal current consumption.

All trim capacitors are disconnected in Sleep Mode (this minimizes current consumption). Whenever the TDA523x switches from Sleep Mode to Run Modes, the Master Control Unit reads out the XTALCAL0 and XTALCAL1 registers and connects the selected trim capacitors to the crystal. A modification of XTALCAL0 or XTALCAL1 registers in Run Modes does not immediately alter the setting of the activated trim capacitors unless the SFR control bit XTALTREN, is set.

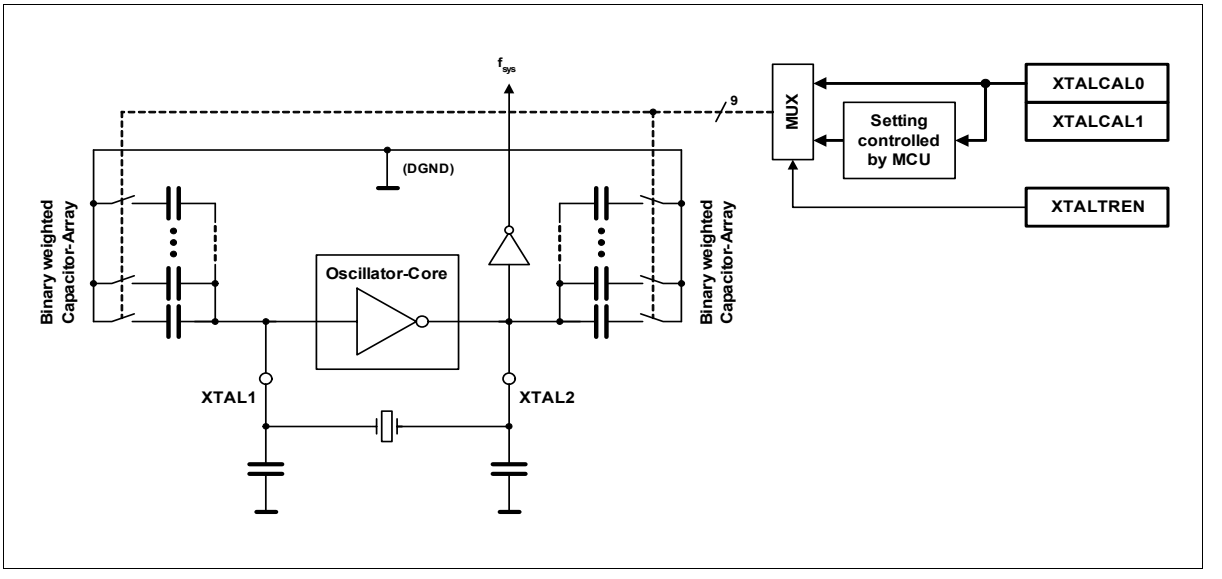

Figure 14 Crystal Oscillator

Crystal Selection:

The recommended crystal type and manufacturer is listed in the **Bill of Materials** in the Evaluation Board section of this Data Sheet. This crystal has been released by Infineon as well by the crystal manufacturer for optimal operation with TDA523x.

If additional crystal types are released, this information will be published on the related TDA523x product page at www.infineon.com.

The crystal frequency is calculated:

For TDA5230 (Lo Side LO Injection)

$$f_{sys}=A*(f_{RF}-10.7MHz)/64$$

For TDA5231 (Hi Side LO Injection

$$f_{sys}=A*(f_{RF}+10.7MHz)/64$$

Values for A depend on the frequency band: 302...320MHz...A=3 (TDA5231), 433...450MHz...A=2, 865...870MHz...A=1 (TDA5230)

The crystal frequency is automatically calculated by the IAF TDA523x Configuration Tool.

Recommended Trimming Procedure

- Set the TDA523x to SLEEP mode
- Set the registers XTCAL0 and XTCAL1 to the expected nominal values
- Set the TDA523x to Slave Mode Run
- Set the register bit XTALTREN in register CMC1
- Wait for 0.5ms minimum
- Trim the oscillator by increasing and decreasing the values of XTALCAL0/1
- Never change the trim capacitor size by more than 1 pF!
- When the Oscillator is trimmed, reset the XALTREN bit
- Set the TDA523x to SLEEP mode
- Add the settings of XTCAL0/1 to the configuration. It must be set after every power up or brown out!

Using the High Precision Mode

As discussed earlier, the TDA523x allows to the crystal oscillator to be trimmed by the use of internal trim capacitors. It is also possible to use the trim functionality to compensate temperature drift of crystals.

During Run Mode (always when the receiver is active) the capacitors are automatically connected and the oscillator is used in the High Precision Mode.

On entering Sleep Mode, the capacitors are automatically disconnected to save power.

If the High Precision Mode is also required for Sleep Mode, the automatic disconnection of trim capacitors can be avoided by setting XALTREN to 1 (enable XTAL trim).

Setting of XALTREN has to be changed only in Run-Mode!

CMC1: Chip Mode Control Register 1

ADDR: 0x03		*Reset Value: 0x00*
Bit	**R/W**	**Description**
4	W	XTALTREN: XTAL Trim Enable 0: Trimming is disabled 1: Trimming is enabled

XTALCAL0: Trim XTAL frequency, coarse

ADDR: 0x61		*Reset Value: 0x10*
Bit	**R/W**	**Description**
4	W	XTAL_SW_COARSE_4: Connect trim capacitor: 16 pF
3	W	XTAL_SW_COARSE_3: Connect trim capacitor: 8 pF
2	W	XTAL_SW_COARSE_2: Connect trim capacitor: 4 pF
1	W	XTAL_SW_COARSE_1: Connect trim capacitor: 2 pF
0	W	XTAL_SW_COARSE_0: Connect trim capacitor: 1 pF

XTALCAL1: Trim XTAL frequency, fine

ADDR: 0x62		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3	W	XTAL_SW_FINE_3: Connect trim capacitor: 500 fF
2	W	XTAL_SW_FINE_2: Connect trim capacitor: 250 fF
1	W	XTAL_SW_FINE_1: Connect trim capacitor: 125 fF
0	W	XTAL_SW_FINE_0: Connect trim capacitor: 62.5 fF

2.4.3.2 External Clock Generation Unit

The chip provides a programmable clock signal at the CLKOUT/RXD pin that is derived from the internal system clock. To save power, this unit can be disabled by the SFR CLKOUTEN bit. The Clock Generation Unit divides the internal clock by an adjustable factor down to the desired CLKOUT frequency. The 20-bit wide division factor, stored in the CLOCKOUT0, CLOCKOUT1 and CLOCKOUT2 registers, allows a CLKOUT-frequency to be generated down to approximately 10 Hz. The 1:2 divider following the 20-bit counter creates the final CLKOUT signal with 50% duty cycle.

The resulting CLKOUT frequency can be calculated by:

$$f_{CLKOUT} = \frac{f_{sys}}{2 \cdot \text{division factor}}$$

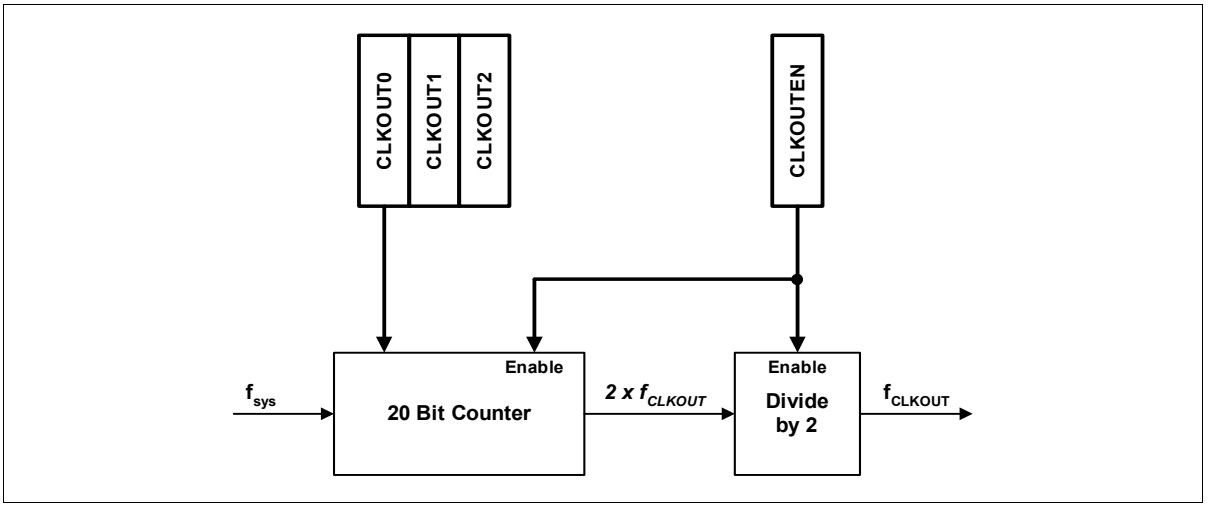

Figure 15 External Clock Generation Unit

The maximum CLKOUT frequency is limited by the driver capability of the CLKOUT/RXD pin and depends on the external load connected to this pin. Please be aware that large loads and/or high clock frequencies at this pin may interfere with the receiver and reduce performance.

After Reset the CLKOUT/RXD pin is activated and the division factor initialized to 7 (equals 1 MHz for f_{sys} of 14 MHz).

A higher clock output frequency than 1 MHz is not recommended.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		*Reset Value: 0x40*
Bit	**R/W**	**Description**
6	W	CLKOUTEN: CLKOUT enable 0: Disable 1: Enable programmable clock output

CLKOUT0: Clock Divider Register 0

ADDR: 0x13			*Reset Value: 0x07*
Bit	**R/W**	**Description**	
7:0	W	CLKOUT0: Clock Out Divider: Bit 7...Bit 0 (LSB) Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2	

CLKOUT1: Clock Divider Register 1

ADDR: 0x14			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	CLKOUT1: Clock Out Divider: Bit 15...Bit 8 Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2	

CLKOUT2: Clock Divider Register 2

ADDR: 0x15			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
3:0	W	CLKOUT2: Clock Out Divider: Bit 19 (MSB)...Bit 16 Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2	

2.4.4 RF-PLL Synthesizer

The Phase Locked Loop RF synthesizer consists of a VCO, programmable divider chains, a phase detector, a charge pump and a loop filter. The on chip VCO includes a spiral-inductor and varactors. The loop filter is also fully integrated on chip. The VCO signal is fed to both the programmable synthesizer divider chain and to a programmable RF divider. This RF divider allows selection between three operational frequency bands and drives a fixed divider by four, which generates the quadrature LO signals for the Image Reject Mixer.

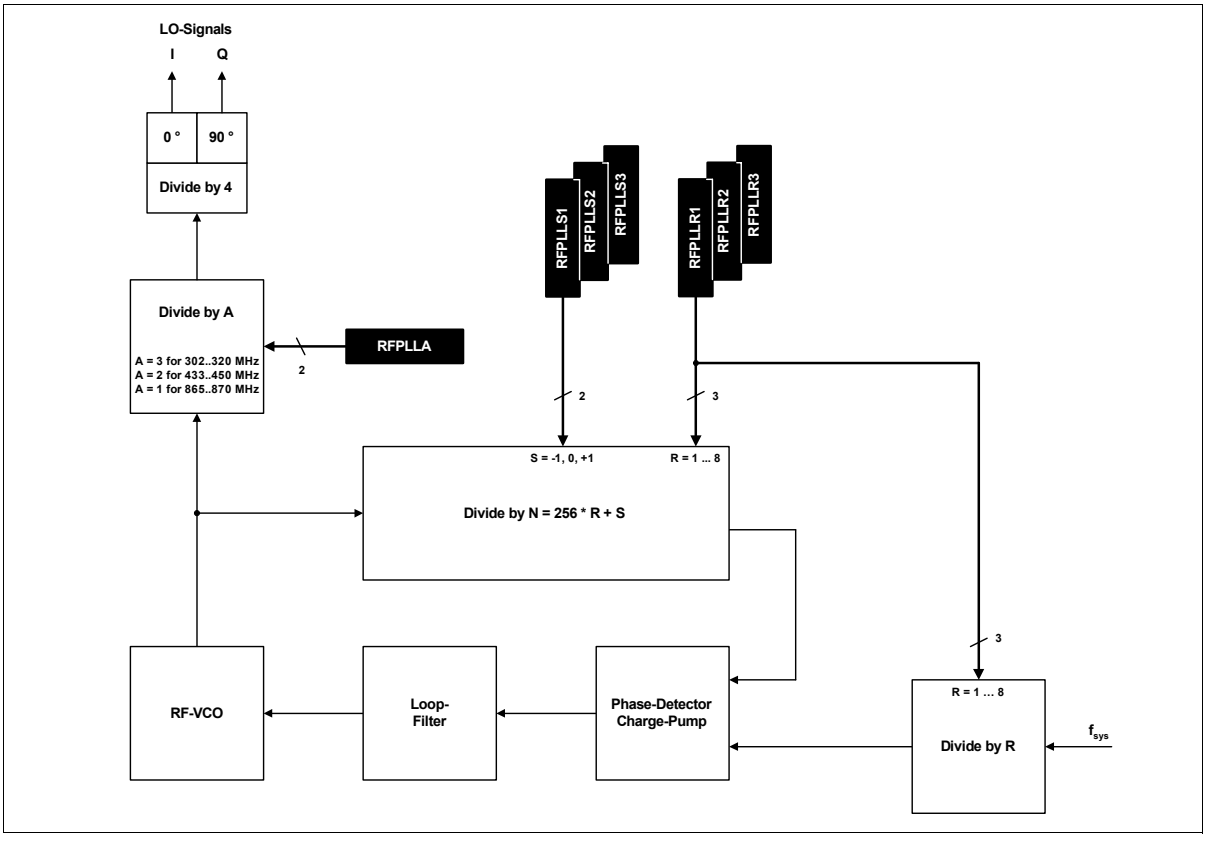

Figure 16 RF PLL

Selection of a distinct operational frequency band is done via the SFR control bits RFPLLA. The overall division factor of the PLL-loop is determined by the content of the SFR control bits RFPLLRx and RFPLLSx, which control a programmable tri-modulus divider and a reference frequency divider. Depending on the configuration of the multi-channel feature, the effective source of the control bits RFPLLRx can either be RFPLLR1, RFPLLR2 or RFPLLR3 and the source of the control bits RFPLLSx can be either RFPLLS1, RFPLLS2 or RFPLLS3.

Based on the tri-modulus divider concept, up to 17 distinct channels[1)] are accessible within the selected operational frequency band by utilizing the same reference crystal frequency. The selected LO-frequency is described by the formula:

$$f_{LO} = \frac{f_{sys}}{R} \cdot (256 \cdot R + S) \cdot \frac{1}{4 \cdot A} = \frac{f_{sys}}{4 \cdot A} \cdot \left(256 + \frac{S}{R}\right)$$

Values for A depend on the frequency band: 302...320MHz...A=3 (TDA5231), 433...450MHz...A=2, 865...870MHz...A=1 (TDA5230)

Values for S are +1, 0, -1

Values for R are 1,2,3,4,5,6,7,8

Example:

A system for 433.92 MHz, having an f_{sys}=13.225625MHz has following available sub-channels:

S	R	f_{RF} [MHz]
1	1	435.573
1	2	434.747
1	3	434.471
1	4	434.333
1	5	434.251
1	6	434.196
1	7	434.156
1	8	434.127
0	2	433.92
-1	8	433.713
-1	7	433.684
-1	6	433.644
-1	5	433.589
-1	4	433.507
-1	3	433.369

1) Channels with receive frequencies close to the harmonics of the reference crystal frequency should not be used in applications.

S	R	f_{RF} [MHz]
-1	2	433.093
-1	1	432.267

Calculation of sub-channels is automatically performed by the IAF TDA523x Configuration Tool.

When defining a multichannel system, the correct selection of channel spacing is extremely important. A general rule is not possible, but following must be considered:

- If an additional SAW filter is used, all channels including their tolerances have to be inside the SAW filter bandwidth.
- The distance between channels has to be high enough, that no overlapping can happen. Strong input signals may still appear as recognizable input signal in the neighboring channel because of the limited suppression of IF Filters. Example: a typical 280kHz IF filter has at 10.3 MHz (10.7 Mhz-0.4 MHz) only 30 dB suppression. A -70 dBm input signal appears like a -100 dBm signal, which is inside the receiver sensitivity. In critical cases the use of two IF filters must be considered. See also **Chapter 2.4.8 Functionality of the IF Path**

For Lo Side LO Injection mode operation: $f_{RF} = f_{LO} + 10.7$ MHz

For Hi Side LO Injection mode operation: $f_{RF} = f_{LO} - 10.7$ MHz

Dual: ARFPLL1 and BRFPLL1:Conf.A RF PLL setting, channel 1 (Slave Mode & Self Polling Mode)

ADDR: 0x22 and 0x43		*Reset Value: 0x29*
Bit	**R/W**	**Description**
6:5	W	RFPLLA: band selection 00 : select 315 MHz band, A=3 01 : select 434 MHz band, A=2 10 : select 868 MHz band, A=1
4:2	W	RFPLLR1: channel 1, PLL divider factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS1: channel 1, PLL divider factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

1) Channels with receive frequencies close to the harmonics of the reference crystal frequency should not be used in applications.

Dual: ARFPLL2 and BRFPLL2:Conf. ARF PLL setting, channel 2 (Self Polling Mode)

ADDR: 0x23 and 0x44		*Reset Value: 0x08*
Bit	**R/W**	**Description**
4:2	W	RFPLLR2: channel 2, PLL divider factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS2: channel 2, PLL divider factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

Dual: ARFPLL3 and BRFPLL3:Conf.A RF PLL setting, channel 3 (Self Polling Mode)

ADDR: 0x24 and 0x45		*Reset Value: 0x0A*
Bit	**R/W**	**Description**
4:2	W	RFPLLR3: channel 3, PLL divider factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS3: channel 3, PLL divider factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

1) Channels with receive frequencies close to the harmonics of the reference crystal frequency should not be used in applications.

2.4.5 Master Control Unit

2.4.5.1 Overview

The Master Control Unit controls the operation modes, the global states, and is generally responsible for automating data reception, verification, identification, extraction, and storage into the FIFO. The data without RUNIN and TSI are read via SPI from the FIFO by the external microcontroller.

The following operational modes and the behavior of the Master Control Unit are fully automatic and influenced only by SFR settings and by incoming RF streams.

The TDA523x has two major operational modes. Modes are switched by the SFR bit MSEL0

In **Slave Mode** the device is controlled via SPI by the external microcontroller. This mode supports:

- Run Mode Slave, where the receiver is continuously active
- Sleep Mode, where the receiver is switched off for power saving. This mode can also be used to change register settings
- Hold Mode, allows to register settings to be changed. The change to Hold Mode and back is faster than changing to Sleep Mode.

Switching between configurations and channels, as well as in between Run and Sleep mode must be initiated by the microcontroller.

In **Self Polling Mode** TDA523x autonomously polls for incoming RF signals. The receiver switches automatically between the two configurations (Configuration A and Configuration B) and up to 3 channels per configuration (Further information is located in **Chapter 2.4.6 Polling Timer Unit**).

Between scans, the receiver is automatically switched off to save power. If an incoming signal fulfills the selected wake-up criteria, matches the TSI pattern, and passes the optional message ID screening, the payload is loaded into the FIFO, and, if not masked, an interrupt is generated. Then, the payload data can be read via SPI.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		Reset Value: 0x40
Bit	**R/W**	**Description**
1	W	SLRXEN: Slave Receiver enable This Bit is used only in Operating Modes Run Mode Slave, Sleep Mode 0: Receiver is in Sleep Mode 1: Receiver is in Run Mode Slave
0	W	MSEL: Operating Mode 0: Run Mode Slave, Sleep Mode 1: Self Polling Mode

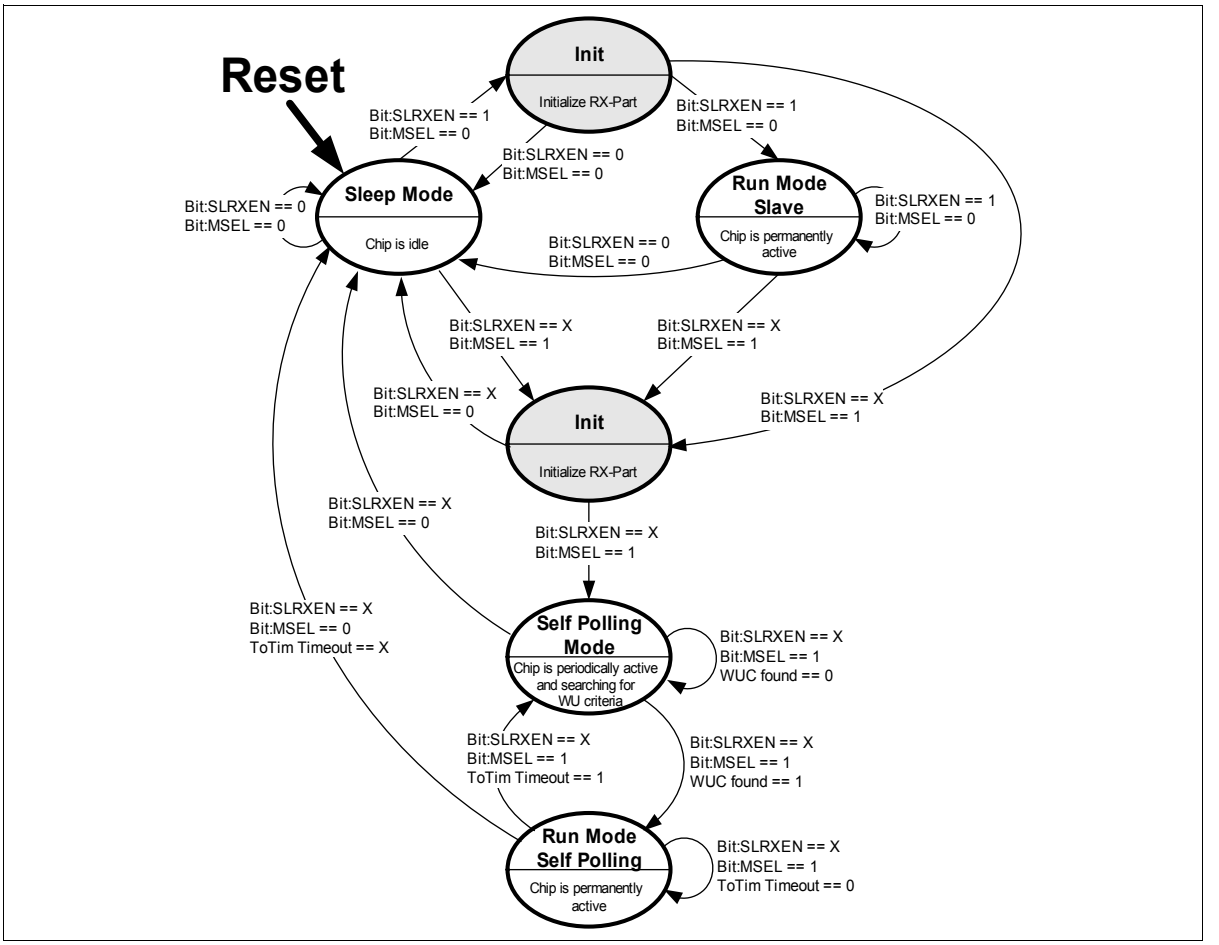

Figure 17 Global State Diagram

2.4.5.2 Run Mode Slave

In Run Mode Slave, the receiver is able to continuously scan for incoming data streams. Detection and validation of a wake up pattern are not done, but correct RUNIN and TSI are required.

Recognition of TSI and validation of the optional MID (Message IDentification) are done automatically. The data payload is extracted from the data stream, and moved to the FIFO.

The various recognition steps are communicated by interrupts. Interrupts are generated at Framestart (when a valid TSI has been detected), when a valid MID has been found, and at EOM (End of Message).

Run Mode Slave is entered by setting SFR CMC0 bits MSEL to 0 and SLRXEN to 1.

Configurations are switched via SFR bit RMSL in the CMC0 register. The channel in use is always defined in the ARFPPLL and BRFPLL SFRs, depending on the selected configuration.

The configuration may be changed only in Sleep Mode or in Hold Mode. This is necessary to restart the state machine with defined settings at a defined state. Otherwise the state machine may hang up. Re-configurations using Hold Mode is faster, because there is no Start Up sequence.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		*Reset Value: 0x40*
Bit	**R/W**	**Description**
3	W	RMSL: Run Mode Slave Configuration This Bit is relevant only in Slave Mode, to select the used configuration 0: Config A 1: Config B

Figure 18 illustrates the **internal behavior** of the FSM (Finite State Machine) in Run Mode Slave.

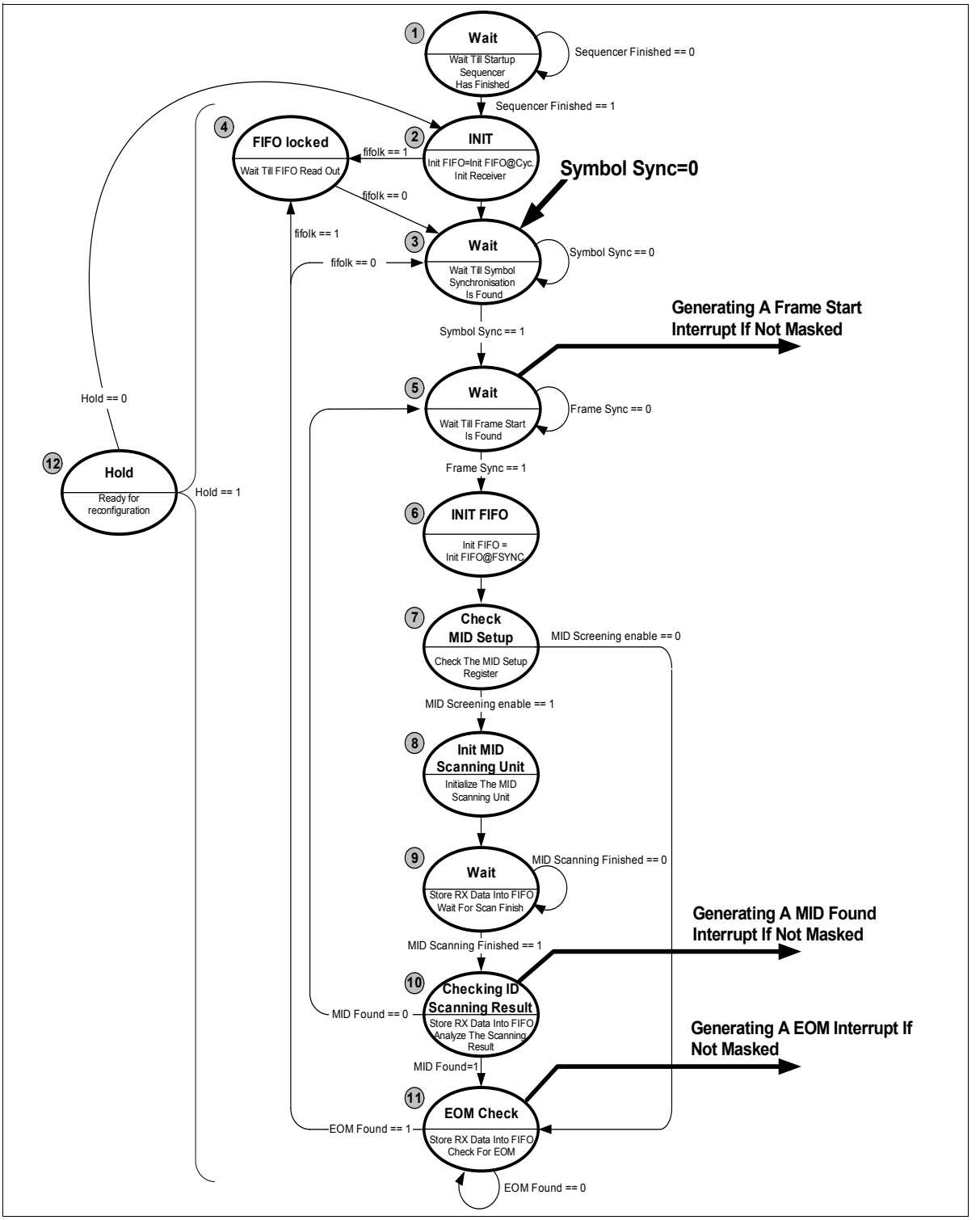

Figure 18 Run Mode Slave

Notes to State Diagram Run Mode Slave:

1.) **Wait:** Waiting until start up sequencer has completed the power up procedure.

2.) **Init:** The Receiver will be initialized and the FIFO will be initialized when the SFR control bit INITFIFO is set. Read out the Modulation Type Configuration (ASK or FSK), which is defined in the SFR control bits AMT/BMT and set the device to the configured mode. Set the channel to the correct value, which is defined in the ARFPLL1/BRFPLL1 register.

3.) **FIFO locked**: When the signal **fifolk** is set, the chip enters this state and remains there until the signal **fifolk** is reset. In this state, no further data reception is possible and therefore, no **SYNC** or **FSYNC** will be generated, even if a data-packet is present in the received data stream. (More information on the FIFO behavior can be found in chapter **Chapter 2.4.15 Data FIFO**).

4.) **Wait:** Wait until symbol synchronization is complete. A loss of symbol synchronization always leads into this state, whatever the current state is. This state is left only, if symbol-synchronization can be established on the received data stream. (More information on the synchronization behavior can be found in **Chapter 2.4.13 Frame Synchronization**).

5. **Wait:** Wait until a start of a data packet (frame) is detected. All bits received from **FSYNC** until the detection of **EOM** will be transferred to the FIFO.

6.) **INIT FIFO:** The FIFO will be initialized, if the SFR control bit FSINITFIFO is set

7.) **Check MID Setup**: Check the configuration of the Message ID Unit. Depending on the SFR control bit MIDSEN a Message ID scanning is started or not. If no Message ID scanning is selected, the next state is the state **EOM check**. Otherwise the Message ID scanning unit is activated to search for a valid Message ID.

8.) **Init MID Scanning Unit:** Initialize the Message ID scanning unit.

9.) **Wait:** Wait until the Message ID scanning unit has finished the search for a valid message ID. All incoming data is stored in the FIFO.

10.)**Checking ID Scanning Result:** The result of a search for a Message ID is checked. If no valid MessageID was found, a search for a new frame is started. Be aware that all received bits after **FSYNC** were stored in the FIFO, even if no Message ID was found. After a successful search for a Message ID , the next state will be **EOM check**.

11.)**EOM Check:** Incoming data bits are transferred to the FIFO until an **EOM** is detected. The criteria for **EOM** are defined in the AEOMC/BEOMC register. If the SFR control bit FIFOLK is set, the signal **fifolk** will be asserted at **EOM**. Depending on the state of **fifolk**, the next chip state will be **FIFO locked** or **Wait for Symbol Synchronization**.

2.4.5.3 HOLD Mode

This state (item 12 in the state diagram **Figure 17**) is used for fast reconfiguration of the chip in Slave-Mode. This state can be reached after the Startup Sequencer and Initialization of the chip has been finished from any state from 3 to 11. To reconfigure the chip the SFR control bit HOLD must be set. After reconfiguration in this state the SFR control bit HOLD has to be cleared again. After leaving the HOLD state, the INIT state is entered and the receiver loads the new settings. Be aware that the time between changing the configuration and reinitialization of the chip must be at least 40 µs. Take note that one SPI command for clearing the SFR control bit needs 24 bits or 20 µs at the highest SPI data rate. The remaining 20 µs must be guaranteed by the application.

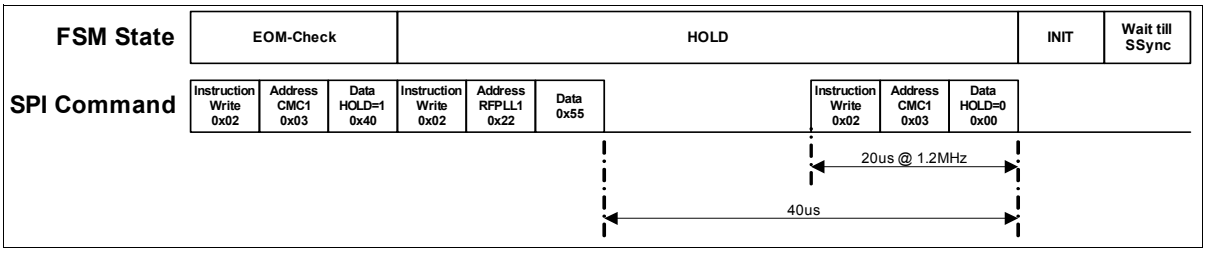

Figure 19 Hold State Behavior

HOLD Mode should only be entered from Run Mode Slave. Configuration changes in Self Polling Mode should be done by switching to SLEEP Mode and returning to Self Polling Mode after reconfiguration

CMC1: Chip Mode Control Register 1

ADDR: 0x03			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
6	W	HOLD: Holds the chip in the config state (only in Run Mode Slave) 0: Normal Operation 1: Jump into the config state Hold	

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2.4.5.4 SLEEP Mode

The SLEEP Mode is a power save mode. The complete RF part is switched off and the oscillator is in Low Precision Mode. Like in HOLD mode, the chip can be reconfigured. When switching from SLEEP to Run Mode Slave, the state machine starts with the internal Start Up Sequence.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		Reset Value: 0x40
Bit	**R/W**	**Description**
1	W	SLRXEN: Slave Receiver enable This Bit is only used in Operating Mode Run Mode Slave / SLEEP Mode 0: Receiver is in SLEEP Mode 1: Receiver is in Run Mode Slave
0	W	MSEL: Operating Mode 0: Run Mode Slave / SLEEP Mode 1: Self Polling Mode

2.4.5.5 Self Polling Mode

In Self Polling Mode TDA523x autonomously polls for incoming RF wake up data streams. There is no processing load on the host microcontroller. When a wake up criterion has been found, the mode is changed to Run Mode Self Polling for automatic verification of TSI, MIDs and transfer of data to the FIFO.

Self Polling Mode is entered by setting the register bit MSEL to 1.

Configuration changes are allowed only by switching to SLEEP mode, and returning after reconfiguration.

The **Polling Timer Unit** controls the timing for scanning (On Time) and sleeping (Off Time). Two independent configuration sets (A and B) are automatically switched, thus enabling scanning from different transmit sources. Additionally, within each configuration as many as 3 different frequency channels may be scanned to allow multi-channel applications.

See also **Chapter 2.4.6 Polling Timer Unit**.

The **Wake Up Generation Unit** identifies whether an incoming data pattern matches with the configurable wake up criterion.

After receiving the wake up pattern, modulation can be switched.

See also **Chapter 2.4.5.6 Automatic Modulation Switching** and **Chapter 2.4.12 Wake Up Generation Unit**.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		*Reset Value: 0x40*
Bit	**R/W**	**Description**
2	W	DCE: Dual Configuration Enable This Bit is relevant only in Self Polling Mode. It defines whether both configurations are used. 0: Only Config A is used 1: First Config A is used; then Config B is used

RFPLLAC: RF PLL Actual Channel Register

ADDR: 0x06		*Reset Value: 0x00*
Bit	**R/W**	**Description**
1:0	R	RFPLLACS: Actual Channel This register is set after a Wake Up found in the Self Polling Mode 00b: No channel was actually found 01b: Channel 1 according to RFPLL1 setting was found 10b: Channel 2 according to RFPLL2 setting was found 11b: Channel 3 according to RFPLL3 setting was found

Dual: AMT and BMT: Conf.A Modulation Type Register

ADDR: 0x21 and 0x42		*Reset Value: 0x04*
Bit	**R/W**	**Description**
3:2	W	NOC: Number of channels Only used in the Self Polling Mode to define how many channels have to be scanned. In the Slave Mode there is only 1 channel used, whatever here is configured. Min: 01b = 1 channel Max: 11b= 3 channels

The following state diagrams and explanations help to illustrate the behavior during Self Polling Mode. First, there is a wake up search for a wake up pattern according configuration A on up to three different channels. Then, there is an optional search for a wake up pattern according configuration B, again including up to 3 channels.

In applications using only a single configuration, settings are always taken from Configuration A

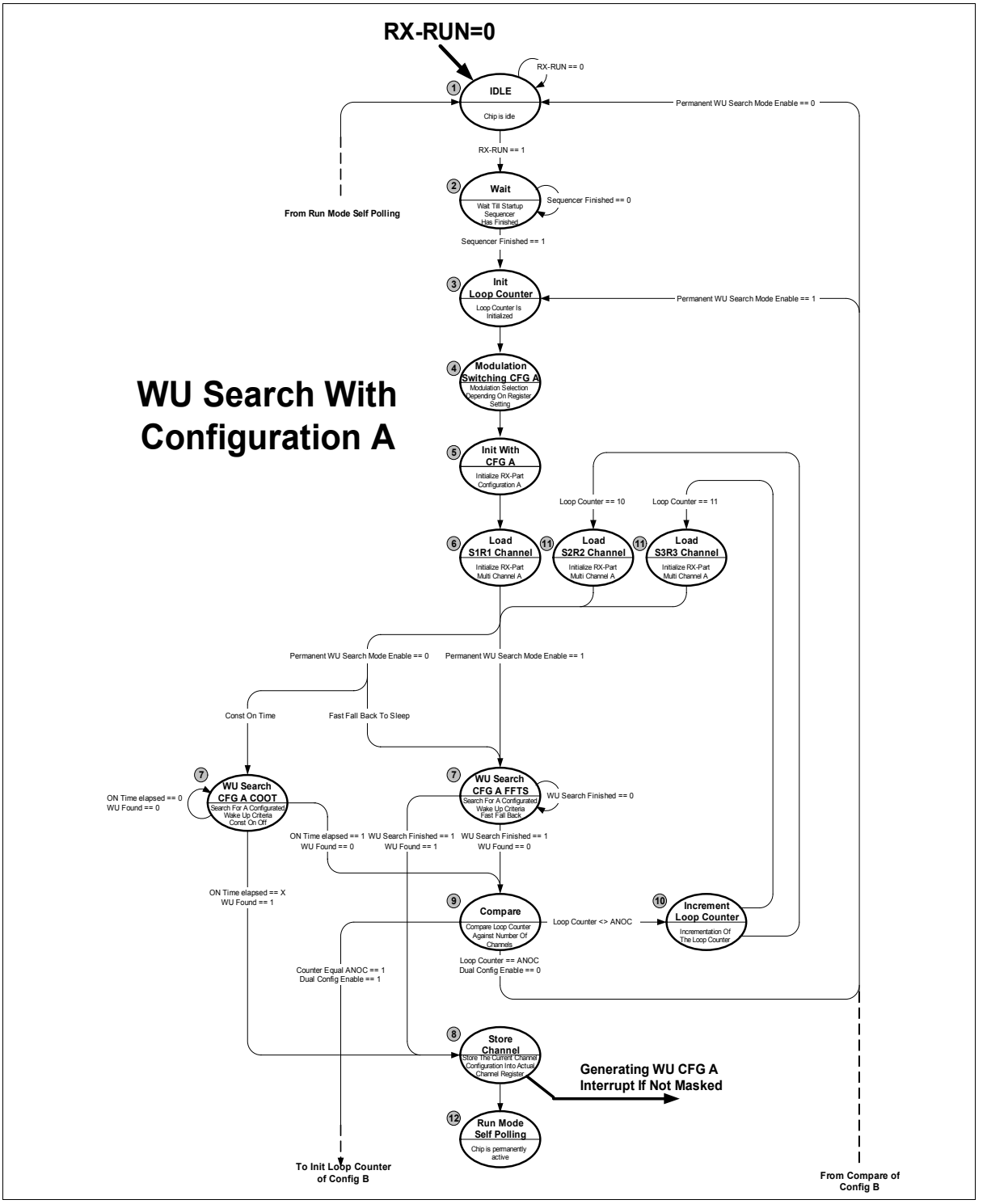

Figure 20 Wake up Search with Configuration A

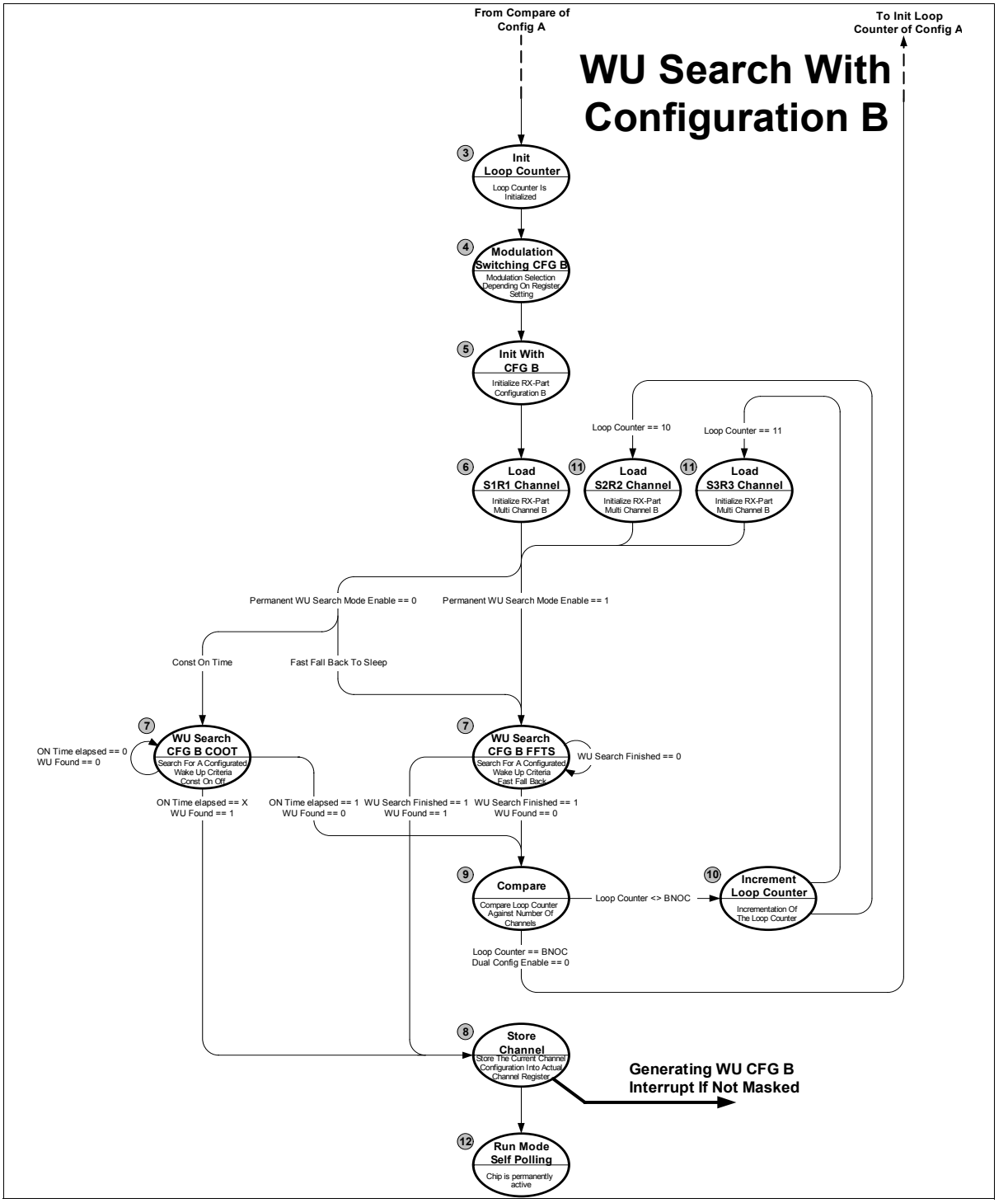

Figure 21 Wake up Search with Configuration B

Notes to Self Polling Modes State diagrams

1.) **Idle:** The state **Idle** is left, when the signal **RX-RUN**, which enables the receiver unit, is set by the Polling Timer Unit. T

2. **Wait:** Wait until the start up sequencer has finished powering up the receiver unit.

3.) **Init Loop Counter:** The loop counter is reset to Channel 1 of configuration A. The state of the loop counter determines the selected channel.

4. **Modulation Switching CFG A:** The receiver unit is set to the modulation type defined in the SFR control bit MT.

5.) **Init with CFG A**: The receiver unit is initialized with the settings given in Configuration A.

6.) **Load S1R1 channel:** The receive channel is set according to the PLL settings given in register ARFPLL1 and waits for about 40µs ($9*64/f_{sys}$).

7. **WU Search CFG A:** As determined by the selected **Self Polling Mode** scheme defined by the SFR control bits SPMSEL and PERMWUSEN, the corresponding WU search scheme is activated.
   If the search for the fulfillment of a **wake up** criterion complicated successfully, the current receive channel is stored by entering the state **Store Channel**. Otherwise, the next state is **Compare**.

8.) **Store Channel:** In this state, the currently selected receive channel (e.g. S1/R1) is stored as the actual channel in the register RFPLLAC. The chip resumes operation in **Run Mode Self Polling** afterwards.

9.) **Compare:** If the loop counter equals the number of channels selected by the SFR control bit ANOC, the next state of the chip will be the **Idle state**, unless dual configuration is enabled by the SFR control bit DCE. In this case, the next state will be **Init Loop Counter** in **Figure 21** . In all other cases, the chip resumes operation in the **Increment Loop Counter** state.

10.)**Increment Loop Counter:** In this state, the loop counter is incremented.

11.)**Load S2R2/S3R3 Channel:** The receive channel is set to the PLL settings given by the register ARFPLL2 and ARFPLL3 respectively and waits for about 40µs(9*64/fsys).

2.4.5.6 Automatic Modulation Switching

In **Self Polling Mode**, the chip is able to automatically change the type of modulation once a **wake up** criterion has been satisfied in a received data stream. The type of modulation used in the different operational modes is selected by the SFR control bits MT, the types are shown in the following register table.

Dual: AMT and BMT: Conf.A Modulation Type Register

ADDR: 0x21 and 0x42		*Reset Value: 0x04*
Bit	**R/W**	**Description**
3:2	W	NOC: Number of channels Used only in the Self Polling Mode to define how many channels must be scanned. In the Slave Mode only one channel is used, regardless of the configuration. Min: 01b = 1 channel Max: 11b= 3 channels
1:0	W	MT: Modulation Type

	Run Mode Slave	Self Polling Mode	Run Mode Self Polling
00b	ASK	ASK	ASK
01b	FSK	FSK	FSK
10b	ASK	FSK	ASK
11b	FSK	ASK	FSK

2.4.5.7 Multi-channel in Self Polling Mode

Previously mentioned, in Self Polling Mode TDA523x allows up to three channels per configuration to be scanned. Channels are defined in registers ARFPLL1-3 and BRFPLL1-3. The channel number at which a wake up has been found is available in register RFPLLACS. See also **Chapter 2.4.4 RF-PLL Synthesizer**.

Dual: AMT and BMT: Conf.A Modulation Type Register

ADDR: 0x21 and 0x42		*Reset Value: 0x04*
Bit	**R/W**	**Description**
3:2	W	NOC: Number of channels Used only in the Self Polling Mode to define how many channels must be scanned. In the Slave Mode, only one channel is scanned, regardless of the configuration. Min: 01b = 1 channel Max: 11b= 3 channels

Dual: ARFPLL1 and BRFPLL1:Conf.A RF PLL setting, channel 1 (Slave Mode & Self Polling Mode)

ADDR: 0x22 and 0x43		*Reset Value: 0x29*
Bit	**R/W**	**Description**
4:2	W	RFPLLR1: Channel 1, PLL divider factor R[1)]
1:0	W	RFPLLS1: Channel 1, PLL divider factor S[1)]

1)

Dual: ARFPLL2 and BRFPLL2:Conf. ARF PLL setting, channel 2 (Self Polling Mode)

ADDR: 0x23 and 0x44		*Reset Value: 0x08*
Bit	**R/W**	**Description**
4:2	W	RFPLLR2: Channel 2, PLL divider factor R[1)]
1:0	W	RFPLLS2: Channel 2, PLL divider factor S[1)]

Dual: ARFPLL3 and BRFPLL3:Conf.A RF PLL setting, channel 3 (Self Polling Mode)

ADDR: 0x24 and 0x45		*Reset Value: 0x0A*
Bit	**R/W**	**Description**
4:2	W	RFPLLR3: Channel 3, PLL divider factor R[1)]
1:0	W	RFPLLS3: Channel 3, PLL divider factor S[1)]

1) Channels with receive frequencies close to harmonics of the reference crystal-frequency should not be used in applications.

RFPLLAC: RF PLL Actual Channel Register

ADDR: 0x06		*Reset Value: 0x00*
Bit	**R/W**	**Description**
1:0	R	RFPLLACS: Actual Channel This Register is set after a Wake Up found in the Self Polling Mode 00b: No Channel was actually found 01b: Channel 1 Wake Up according to RFPLL1 setting was found 10b: Channel 2 Wake Up according to RFPLL2 setting was found 11b: Channel 3 Wake Up according to RFPLL3 setting was found

2.4.5.8 Run Mode Self Polling

The chip enters **Run Mode Self Polling** after a successful fulfillment of a **wake up** criterion in Self Polling Mode.

The following steps are performed automatically, depending on register settings

- Modulation switching (see **Chapter 2.4.5.6 Automatic Modulation Switching**)
- Wait for valid TSI (see **Chapter 2.4.13 Frame Synchronization**)
- Initialize FIFO (see **Chapter 2.4.15 Data FIFO**) and write data to FIFO
- Scan for MID's (see **Chapter 2.4.14 Message-ID Scanning**)

Depending on the interrupt masking, the host micro controller is alerted when

- a data frame has started,
- an MID has been found, (if enabled) or
- EOM (End of Message) has been detected.

See also **Chapter 2.4.17 Interrupt Generation Unit**

Run Mode Self Polling is left, when synchronization is lost and the Time Out Timer (TOTIM) has elapsed, and when the mode is switched to SLEEP or Run Mode Slave by the host microcontroller.

As long as the chip is in Run Mode Self Polling, incoming data frames, even without additional wake up patterns, can be received and stored.

The data FIFO can be either initialized and cleared at

- Cycle Start, that means whenever Run Mode Self Polling is entered or
- Frame Start, when a TSI has been successfully identified.

Further information about the data FIFO is found in the **Chapter 2.4.15 Data FIFO**.

CMC0: Chip Mode Control Register 0

ADDR: 0x02		*Reset Value: 0x40*
Bit	**R/W**	**Description**
7	W	INITFIFO: Init FIFO at Cycle Start Initialization of the FIFO can be configured in both Slave Mode and Self Polling Mode. In Slave Mode, this occurs at the beginning of the Slave Run Mode. In Self Polling Mode, initialization is done after a Wake up is found (switching from Self Polling Mode to Run Mode Self Polling). 0: No Init 1: Init FIFO
5	W	TOTIMEN: ToTim Timer enable Time Out Timer is used to return from Run Mode Self Polling to Self Polling Mode whenever there is no Sync for a specific time. 0: Disable 1: Enable ToTim Timer
4	W	FIFOLK: Lock Data FIFO at EOM 0: FIFO lock is disabled 1: FIFO lock is enabled at EOM (see also **Chapter 2.4.15 Data FIFO**)

CMC1: Chip Mode Control Register 1

ADDR: 0x03		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3	W	FSINITFIFO: Init FIFO at Frame Start 0: No Init 1: Init

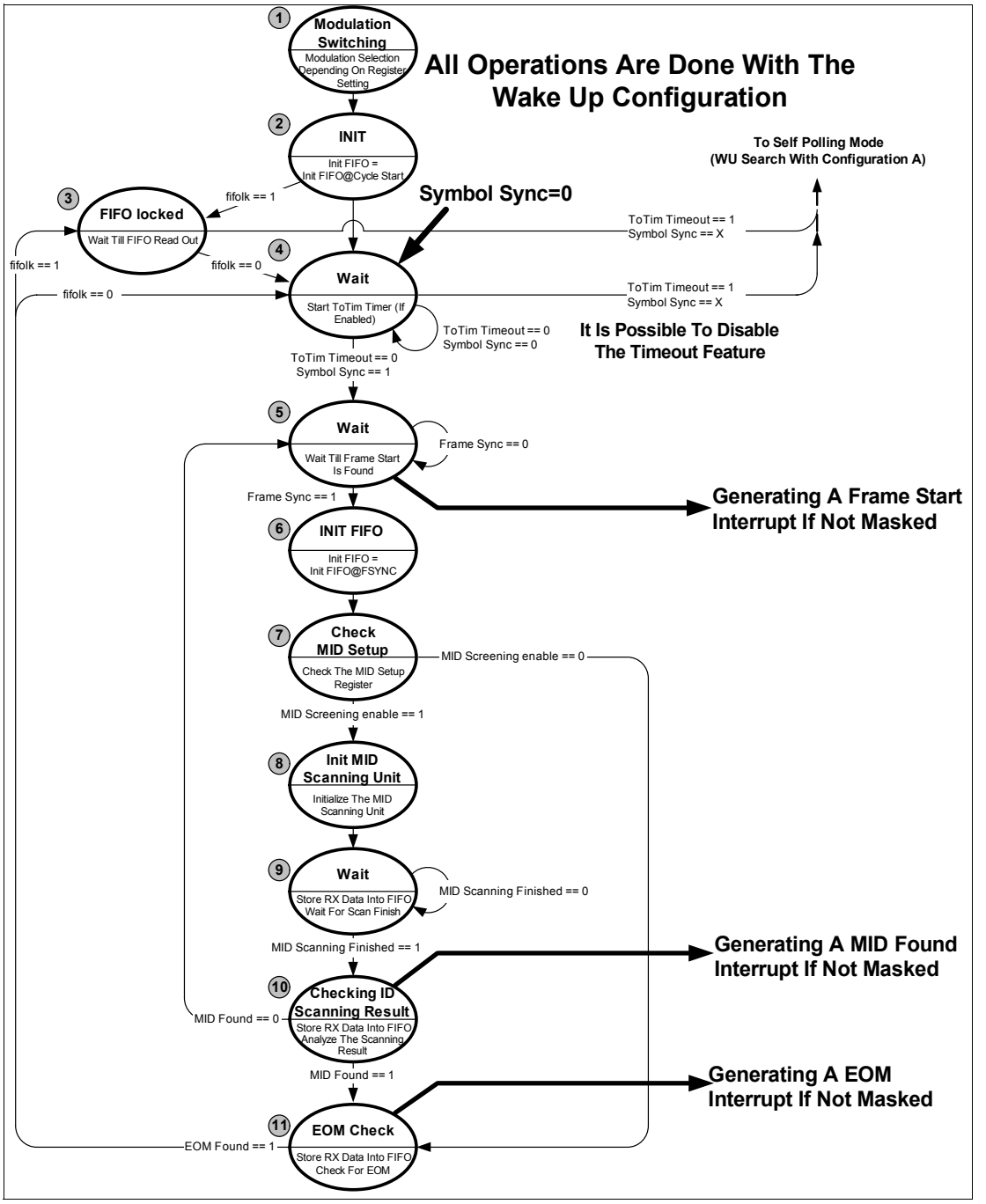

Figure 22 Run Mode Self Polling

Notes to State Diagram Run Mode Self Polling:

1. Modulation Switching: Modulation is set according registers AMT and BMT bits MT.
2. Init: The Receiver will be initialized and the FIFO will be initialized and cleared when the SFR control bit INITFIFO is set. Read out the Modulation Type Configuration (ASK or FSK), which is defined in the SFR control bits AMT/BMT, and set the device to the configured mode. Set the channel to the correct value, which is defined in the ARFPLL1/BRFPLL1 register.
3. **FIFO locked**: When the signal **fifolk** is set, the chip enters this state and remains there until the signal **fifolk** is deasserted. In this state, no further data reception is possible and therefore no **SYNC** or **FSYNC** will be generated, even if a data packet is present in the received data-stream. (More information on the FIFO behavior can be found in **Chapter 2.4.15 Data FIFO**).
4. **Wait:** Wait until symbol synchronization has finished. A loss of symbol synchronization always leads into this state, whatever the current state was. This state is only left, if symbol synchronization could be established on the received data stream. (More information on the synchronization behavior can be found in **Chapter 2.4.13 Frame Synchronization**).
5. **Wait:** Wait until a start of a data packet (TSI) is detected. All bits received from **FSYNC** until the detection of **EOM** will be transferred to the FIFO.
6. **INIT FIFO:** The FIFO will be initialized, if the SFR control bit FSINITFIFO is set
7. **Check MID Setup**: Check the configuration of the Message ID Unit. Depending on the SFR control bit MIDSEN, a Message ID scanning is started or not. If no Message-ID scanning is selected, the next state is the **EOM check** state. Otherwise, the Message ID scanning unit is activated to search for a valid Message-ID.
8. **Init MID Scanning Unit:** Initialize the Message-ID scanning unit.
9. **Wait:** Wait until the Message-ID scanning unit has finished the search for a valid message ID. All incoming data is stored in the FIFO.
10. **Checking ID Scanning Result:** The result of a search for a Message ID is checked. If no valid Message ID was found, a search for a new frame is started. Be aware that all received bits after **FSYNC** were stored in the FIFO, even if no Message ID was found. After a successful search for a Message ID , the next state will be **EOM check**.
11. **EOM Check:** The reception of the data frame is completed with EOM. Dependent on register AEOMC and BEOMC, EOM can be either Sync lost, code violation or number of received bits.

2.4.6 Polling Timer Unit

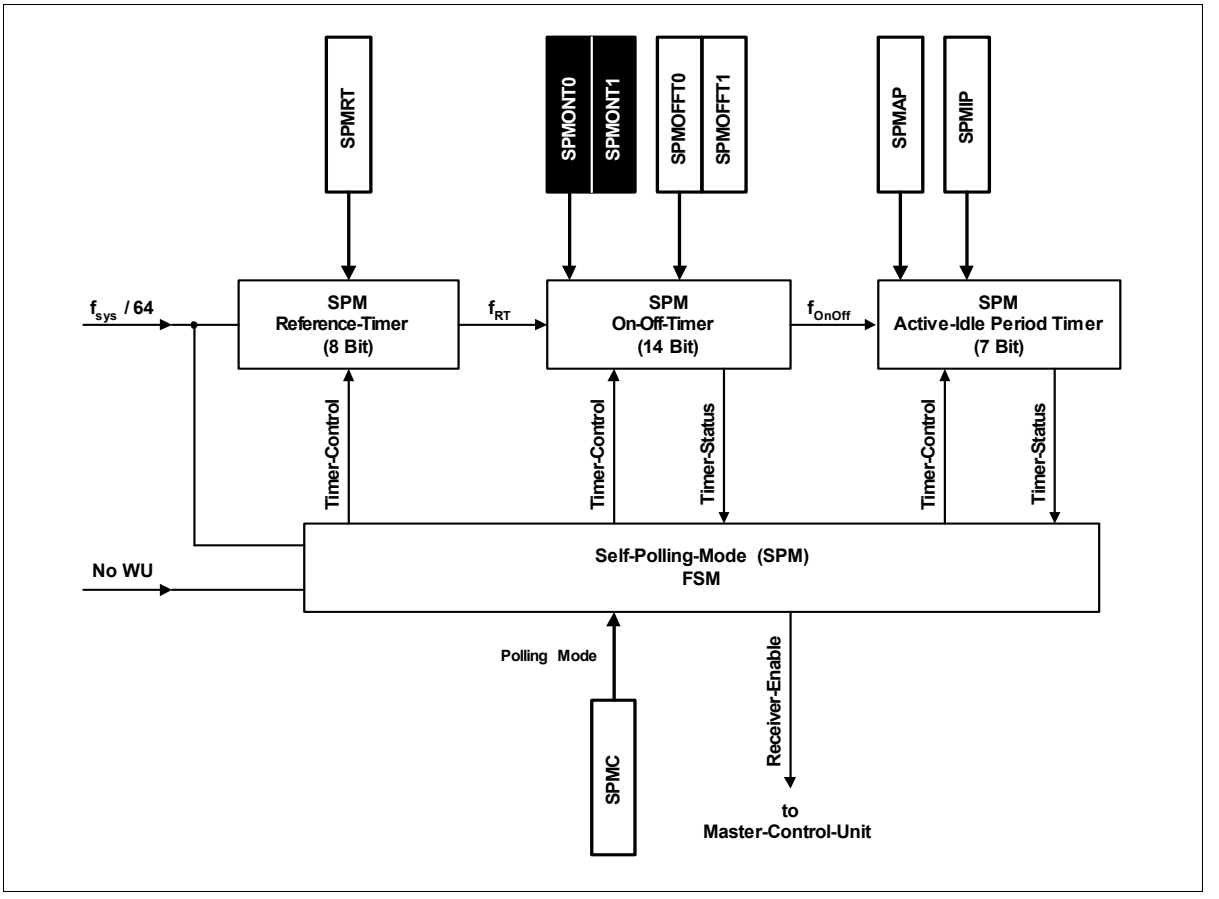

Figure 23 Polling Timer Unit

The Polling Timer Unit consists of a Counter Stage and a Control FSM (Finite State Machine).

The Counter Stage is divided into three sub-modules.

The **Reference Timer** is used to divide the state machine clock (fsys/64) into the slower clock required for the SPM timers.

The **On/Off Timer** and the **Active Idle Period Timer** are used to generate the polling signal. The whole unit is controlled by the SPM FSM.

2.4.6.1 Self Polling Modes

Three polling modes are available to fit the polling behavior to the expected wake up patterns and to optimize power consumption in Self Polling Mode.

The Polling Modes are selected via the Self Polling Mode Control (SPMC) register.

The following four modes are available:

- Constant On/Off
- Fast Fall Back to Sleep
- Mixed Mode(Cfg.A: Constant On/Off; Cfg.B: Fast Fall Back to Sleep)
- Permanent Wake Up Search

A detected wake up forces the chip into Run Mode Self Polling.

In all modes, the timing resolution is defined by the Reference Timer, which scales the incoming frequency (fsys/64) corresponding to the value which is defined in the Self Polling Mode Reference Timer (SPMRT) register. Changing values of SPRMT help to fit the final on/off timing to the calculated ideal timing. Use the TDA523x IAF Configuration Tool for optimization.

2.4.6.2 Constant On/Off Time

In this mode, there is a constant on and a constant off time. Therefore, the resulting master period time is constant. The on and off time are set in the ASPMONT0, ASPMONT1, BSPMONT0, BSPMONT1, SPMOFFT0 and SPMOFFT1 registers. The On Time configuration is done separately for configuration A and B. The selection for single or dual configuration is done in the CMC0 register. When single configuration is selected only configuration A is used. The number of channels is defined in the AMT/BMT register. In the case of multi-channel or combination of multi-channel and dual configuration mode, the configured On Time is used for each channel in each configuration. The following figure shows all possible scenarios.

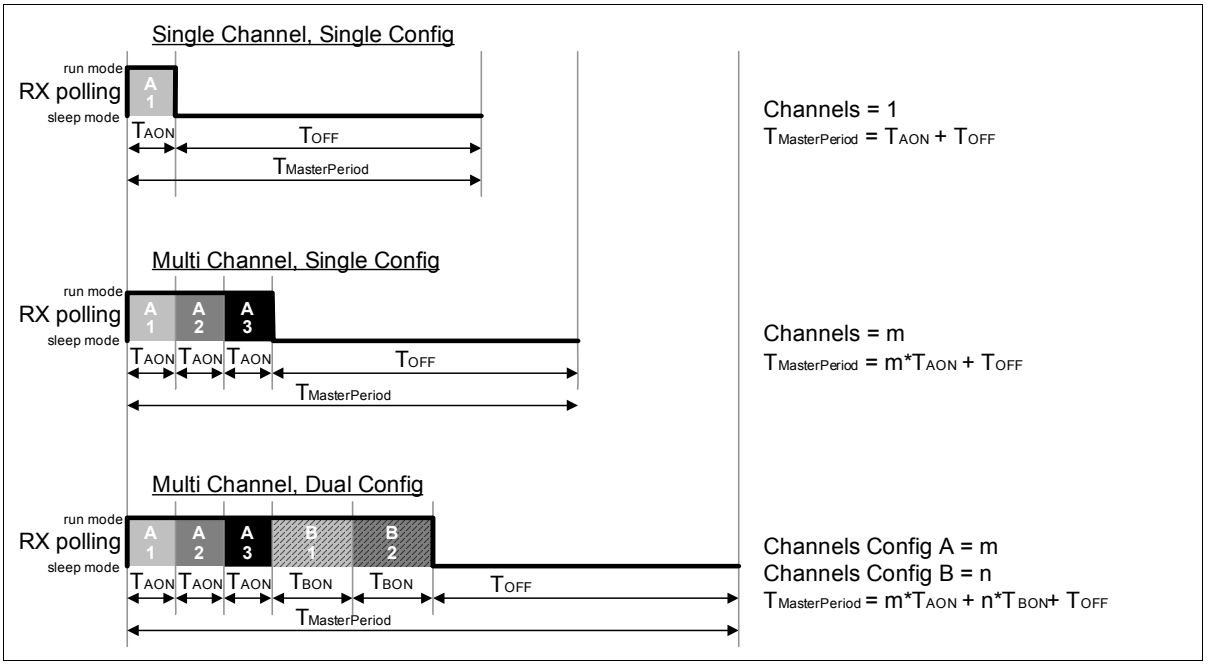

Figure 24 Constant On/Off Time

Calculation Example

For all calculation examples for On and Off Time we will use following example data:

- Configuration A and B used
- Three channels to be scanned in Configuration A, two channels in Configuration B
- Configuration A Data Rate 10 kb/s, +/-10%, Configuration B Data Rate 5 kb/s, +/-10%
- Length of usable Wake Up Pattern is 2000 bits (for both Data Rates)
- Wake Up Criterion requires 10 bits equal to 20 chips
- f_{sys} is 13.225625 MHz (used for 433.92 MHz RF), this means Receiver Start Up Time is 0.576 ms, Channel Hop Latency is 0.06 ms

Calculation of the Master Period Time ($T_{MasterPeriod}$).

$T_{MasterPeriod}$ depends on:

- Length/duration of transmitted Wake Up Pattern
- Data Rate and tolerance
- Length/duration of Wake Up criterion (**Chapter 2.4.12 Wake Up Generation Unit**)

Imagine, the transmission of the Wake Up Pattern starts very little time after the receiver starts polling on this channel. Using our example data, the receiver recognizes only 19 chips out of the required 20, but then the State Machine switches to the next channel. Therefore, the Master Period Time has to be short enough that inside of the (shorter) transmitted Wake Up Pattern, this channel can be successfully polled again.

1) Calculation of Wake Up Times for Each Configuration and Channel:

The Wake Up Time includes Receiver Start Up Time for the first channel scanned, or Channel Hop Latency for the following channels plus 7.625 bits (The 7.625 bits are required for synchronisation and Data Framer Latency) and Wake Up Criterion length at minimal Data Rate.

$T_{WakeUp\_ConfigAChannel1}$=0.576 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.55 ms

$T_{WakeUp\_ConfigAChannel2}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigAChannel3}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigBChannel1}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

$T_{WakeUp\_ConfigBChannel2}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

2) Calculation of usable Wake Up Pattern Time:

The Wake Up Pattern time is the minimal duration of wake up patterns.

$T_{Wakeup\_PatternA}$=Wake Up Pattern/(Data Rate*tolerance)=2000/(10 kb/s*1.1)=181.81 ms

$T_{Wakeup\_PatternB}$=2000/(10 kb/s*1.1)=363.62ms

Note: In many transmit frame descriptions the Wake Up Pattern is terminated by a single bit for synchronisation. In this case, the Wake Up Pattern has to be reduced by the number of bits (or chips) used for TSI (See **Chapter 2.4.13 Frame Synchronization**).

The usable Wake Up Pattern Time is the Wake Up Pattern Time reduced by the longest Wake Up Time of a channel in the related configuration. This is $T_{WakeUp\_ConfigAChannel1}$ for Configuration A, and for Configuration B the scanning of both channels requires the same time.

$T_{usable\_Wakeup\_PatternA}=T_{Wakeup\_PatternA}-T_{WakeUp\_ConfigAChannel1}$=181.81ms-2.55ms=179.26ms

$T_{usable\_Wakeup\_PatternB}=T_{Wakeup\_PatternB}-T_{WakeUp\_ConfigBChannel1}$=363.62ms-3.98ms=359.64ms

3) Calculation of the Master Period Time

$T_{MasterPeriod}$ is smaller then $T_{usable\_Wakeup\_PatternA}$ or $T_{usable\_Wakeup\_PatternB}$ whichever is shorter. In our example:

$T_{MasterPeriod}<T_{usable\_Wakeup\_PatternA}$=179.26ms

Calculation of the On Time

In Constant On/Off Time Wake Up Mode, the On Time limits the search for a Wake Up Criterion for each channel in both configurations. There is an independent On Time for Configuration A channels, and a ON Time for Configuration B channels. The On Time in each configuration has to be longer than the longest Wake Up Time in this configuration.

$T_{ON\_ConfigA}>T_{WakeUp\_ConfigAChannel1}$=2.55ms

$T_{ON\_ConfigB}>T_{WakeUp\_ConfigBChannel1}$=3.98ms

Calculation of the Off Time

The Off Time is the Master Period minus the sum of all On Times.

$T_{OFF}=T_{MasterPeriod}-3*T_{ON\_ConfigA}-2*T_{ON\_ConfigB}=179.26ms-3*2.55ms-2*3.98ms=163.65ms$

Note: Use the TDA523x IAF Configuration Tool to translate the calculated values into register settings. Enter On Times and Off Time as calculated. Watch the Master Period and vary Off Time till the resulting Master Period is shorter than the result of the calculation. Take care that T_{ON} must be always longer and $T_{MasterPeriod}$ always shorter than the calculated values!

2.4.6.3 Fast Fall Back To Sleep

This mode is used to switch off the receiver as quickly as possible to reduce power consumption.

During the search for a wake up pattern, a check is performed in parallel to determine, if there is a bit stream, to which it can be synchronized. If within the limits of the Sync Search Time Out there is no synchronization to a bit stream, the wake up search for this channel is stopped. If synchronization to a bit stream is possible (and not lost again), the chip waits if the wake up criterion is fulfilled. If the Wake Up Criterion is not fulfilled, if in worst case, the last bit of an expected wake up pattern is wrong, the wake up procedure for this channel is stopped, and the chip tries to synchronize on the next channel, or falls back to sleep. That means, that the effective search time and, consequently, the receiver active time are significantly shorter, and power consumption is reduced when no input signal is present. Calculation of Sync Search Time Out is found in **Chapter 2.4.9.1 Synchronization Search Time and Inter-Frame Time**.

The On and Off Time settings are different from the Constant On/Off Time Mode. The BSPMONT register is not used because the whole On time is defined in the ASPMONT register. Regardless of the numbers of channels and whether dual or single configuration is used, the on time is defined with the Config A On Timer. The deactivation of the receiver can happen at different times, but this event does not influence the timer stage because the On time is still the same. So the master period is constant. The following scenarios are the same as before, but with Fast Fall Back to Sleep.

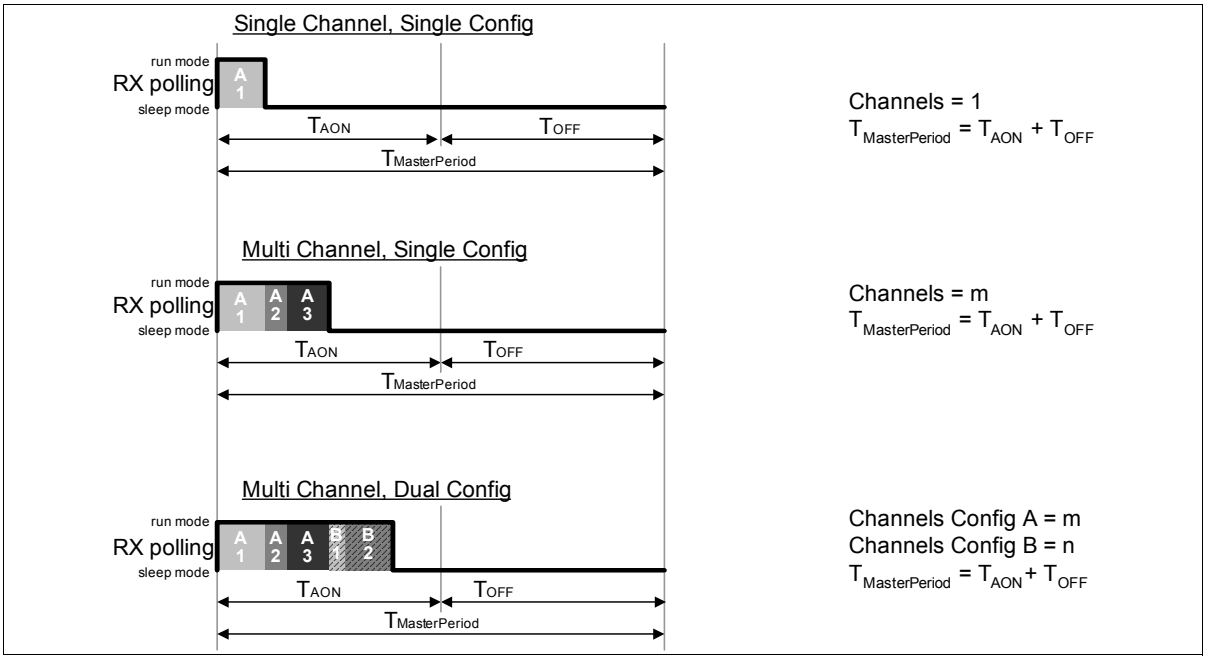

Figure 25 Fast Fall Back to Sleep

Calculation Example

The same example data is used as for Constant On/Off Time:

- Configuration A and B used
- Three channels to be scanned in Configuration A, two channels in Configuration B
- Configuration A Data Rate 10 kb/s, +/-10%, Configuration B Data Rate 5 kb/s, +/-10%
- Length of usable Wake Up Pattern is 2000 bits (for both Data Rates)
- Wake Up Criterion requires 10 bits equal to 20 chips
- f_{sys} is 13.225625 MHz (used for 433.92 MHz RF), this means Receiver Start Up Time is 0.576 ms, Channel Hop Latency is 0.06 ms

Calculation of the Master Period Time ($T_{MasterPeriod}$)

The Master Period Time has to be short enough that inside of the (shorter) transmitted Wake Up Pattern, the channel with the longest Wake Up sequence can be polled twice.

This calculation is equal to the calculation in Constant On/Off Time.

1) Calculation of Wake Up Times for Each Configuration and Channel:

$T_{WakeUp\_ConfigAChannel1}$=0.576 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.55 ms

$T_{WakeUp\_ConfigAChannel2}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigAChannel3}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigBChannel1}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

$T_{WakeUp\_ConfigBChannel2}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

2) Calculation of usable Wake Up Pattern Time:

The Wake Up Pattern time is the minimal duration of wake up patterns.

$T_{Wakeup\_PatternA}$=Wake Up Pattern/(Data Rate*tolerance)=2000/(10 kb/s*1.1)=181.81 ms

$T_{Wakeup\_PatternB}$=2000/(10 kb/s*1.1)=363.62ms

$T_{usable\_Wakeup\_PatternA}$=$T_{Wakeup\_PatternA}$-$T_{WakeUp\_ConfigAChannel1}$=181.81ms-2.55ms=179.26 ms

$T_{usable\_Wakeup\_PatternB}$=$T_{Wakeup\_PatternB}$-$T_{WakeUp\_ConfigBChannel1}$=363.62ms-3.98ms=359.64 ms

3) Calculation of the Master Period

$T_{MasterPeriod}$ is smaller then $T_{usable\_Wakeup\_PatternA}$ or $T_{usable\_Wakeup\_PatternB}$ whichever is shorter. In our example:

$T_{MasterPeriod}$<$T_{usable\_Wakeup\_PatternA}$=179.26 ms

Calculation of the On Time

In Fast Fall Back to Sleep Wake Up Mode, the On Time limits the search for a Wake Up Criteria for all used channels in both configurations. Therefore the On Time is the sum of On Time for all used channels and configurations.

$T_{ON\_}$>$T_{WakeUp\_ConfigAChannel1..3}$+$T_{WakeUp\_ConfigBChannel1..2}$=2.55 ms+2.02 ms+2.02 ms+ +3.98 ms +3.98 ms =14.55 ms

Note: Different to Constant On/Off Time, a longer On Time as calculated will typically not increase power consumption.

Calculation of the Off Time

The Off Time is the Master Period minus the On Time.

T_{OFF}=$T_{MasterPeriod}$-T_{ON}=179.26 ms-14.55 ms=164.71 ms

Note: Use the TDA523x IAF Configuration Tool to translate the calculated values into register settings. Enter On and Off Time as calculated. Watch the Master Period and vary Off Time till the resulting Master Period is shorter than the result of the calculation. Take care that T_{ON} must be always longer and $T_{MasterPeriod}$ always shorter than the calculated values!

2.4.6.4 Mixed Mode (Constant On/Off Time & Fast Fall Back to Sleep)

This mode combines Constant On/Off Time for Configuration A and Fast Fall Back to Sleep for Configuration B. The next figure shows the same scenarios as seen earlier, but now for Mixed Mode.

T_{ON} for Configuration A is calculated according Const On/Off rules, T_{ON} for Configuration B is calculated according Fast Fall Back to Sleep rules.

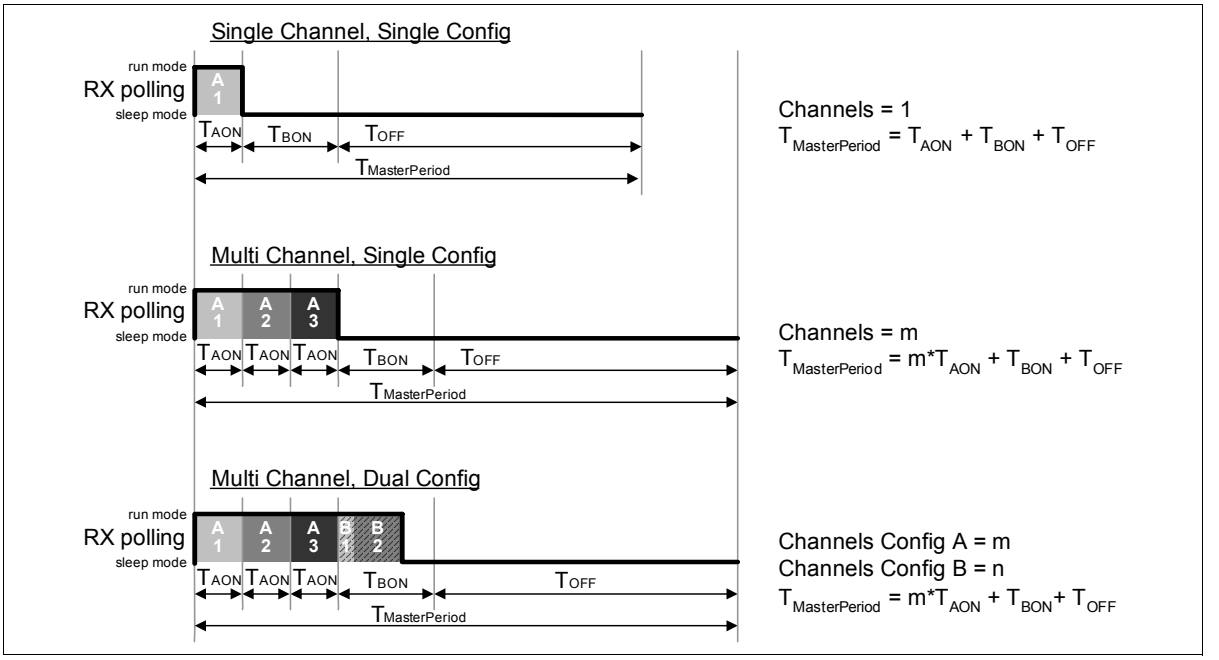

Figure 26 Mixed Mode

Calculation Example

The same example data is used as for Constant On/Off Time:

- Configuration A and B used
- Three channels to be scanned in Configuration A, two channels in Configuration B
- Configuration A Data Rate 10 kb/s, +/-10%, Configuration B Data Rate 5 kb/s, +/-10%
- Length of usable Wake Up Pattern is 2000 bits (for both Data Rates)
- Wake Up Criterion requires 10 bits equal to 20 chips
- f_{sys} is 13.225625 MHz (used for 433.92 MHz RF), this means Receiver Start Up Time is 0.576 ms, Channel Hop Latency is 0.06 ms

Calculation of the Master Period Time ($T_{MasterPeriod}$)

The Master Period Time has to be short enough that inside of the (shorter) transmitted Wake Up Pattern, the channel with the longest Wake Up sequence can be polled twice.

This calculation is equal to the calculation in Constant On/Off Time.

1) Calculation of Wake Up Times for Each Configuration and Channel:

$T_{WakeUp\_ConfigAChannel1}$=0.576 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.55 ms

$T_{WakeUp\_ConfigAChannel2}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigAChannel3}$=0.06 ms+(7.625 bits+10 bits)/(10kb/s*0.9)=2.02 ms

$T_{WakeUp\_ConfigBChannel1}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

$T_{WakeUp\_ConfigBChannel2}$=0.06 ms+(7.625 bits+10 bits)/(5kb/s*0.9)=3.98 ms

2) Calculation of usable Wake Up Pattern Time:

The Wake Up Pattern time is the minimal duration of wake up patterns.

$T_{Wakeup\_PatternA}$=Wake Up Pattern/(Data Rate*tolerance)=2000/(10 kb/s*1.1)=181.81 ms

$T_{Wakeup\_PatternB}$=2000/(10 kb/s*1.1)=363.62ms

$T_{usable\_Wakeup\_PatternA}$=$T_{Wakeup\_PatternA}$-$T_{WakeUp\_ConfigAChannel1}$=181.81ms-2.55ms=179.26 ms

$T_{usable\_Wakeup\_PatternB}$=$T_{Wakeup\_PatternB}$-$T_{WakeUp\_ConfigBChannel1}$=363.62ms-3.98ms=359.64 ms

3) Calculation of the Master Period

$T_{MasterPeriod}$ is smaller then $T_{usable\_Wakeup\_PatternA}$ or $T_{usable\_Wakeup\_PatternB}$ whichever is shorter. In our example:

$T_{MasterPeriod}$<$T_{usable\_Wakeup\_PatternA}$=179.26 ms

Calculation of the On Time

In Mixed Wake Up Mode, the On Time for Configuration A limits the search for a Wake Up Criteria for each used channel in Configuration A. The On Time for Configuration B limits the Wake Up search for all used channels in Configuration B. Therefore the On Time is the sum of On Time for all used channels and configurations.

$T_{ON\_ConfigA}$>$T_{WakeUp\_ConfigAChannel1}$=2.55ms

$T_{ON\_ConfigB}$>$T_{WakeUp\_ConfigBChannel1..2}$=3.98 ms +3.98 ms =7.96 ms

Calculation of the Off Time

The Off Time is the Master Period minus the sum of On Times for Configuration A and the On Time for Configuration B.

T_{OFF}=$T_{MasterPeriod}$-3*$T_{ON\_ConfigA}$-$T_{ON\_ConfigB}$=179.26 ms-3*2.55 ms-7.96 ms=163.65 ms

Note: Use the TDA523x IAF Configuration Tool to translate the calculated values into register settings. Enter On and Off Time as calculated. Watch the Master Period and vary Off Time till the resulting Master Period is shorter than the result of the calculation. Take care that T_{ON} must be always longer and $T_{MasterPeriod}$ always shorter than the calculated values!

2.4.6.5 Permanent Wake Up Search

When the SFR control bit PERMWUSEN is set and the Self Polling Mode is set to Constant On/Off, the receiver will work in Fast Fall Back Mode but it will not go back to the sleep state after the last channel has been searched. Instead, it will start again from

the beginning (Config A, Channel 1) until the on time has elapsed. The timing calculation can be seen in the next figure. Note that Permanent Wake Up Search makes sense only in the Const On/Off Mode.

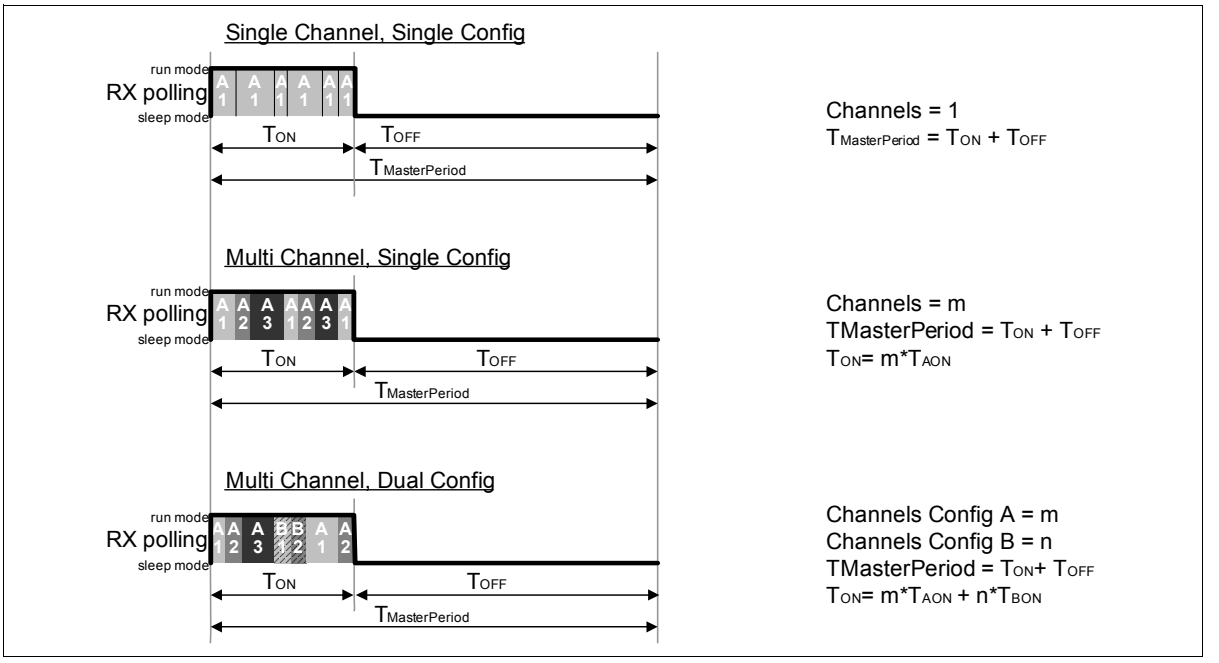

Figure 27 Permanent Wake Up Search

Note: Calculation of On/Off Time and Master Period is equal to Fast Fall Back to Sleep Wake Up Mode.

2.4.6.6 Active Idle Period Selection

This is used to deactivate some polling periods. Normally, the polling starts again after the $T_{MasterPeriod}$. With this Active-Idle Period selection, some of the polling periods can be deactivated independently from the polling mode. The active and idle sequences are set with the SPMAP and the SPMIP registers. The values of these registers determine the factors M and N.

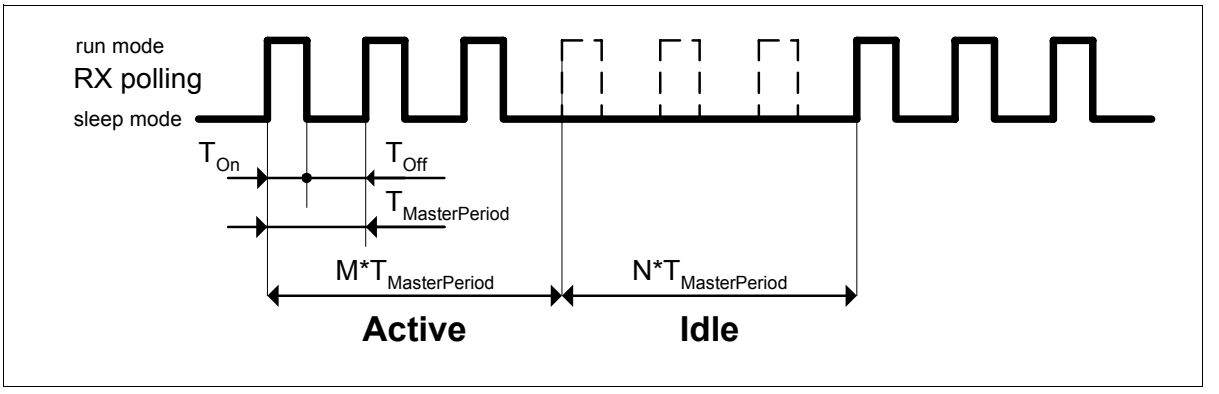

Figure 28 Active Idle Period Including Fast Fall Back To Sleep

SPMC: Self Polling Mode Control Register

ADDR: 0x07			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
3	W	PERMWUSEN: Permanent Wake Up Search enable during On Time 0: Disabled 1: Enabled	
2	W	SPMAIEN: Self Polling Mode Active Idle Enable 0: Disabled 1: Enabled	
1:0	W	SPMSEL: Self Polling Mode Selection 00b: Constant On/Off Time 01b: Fast Fall Back to Sleep 10b: Mixed Mode(Conf.A: Const On/Off, Conf.B: Fast Fall Back to Sleep)	

SPMRT: Self Polling Mode Reference Timer

ADDR: 0x08			*Reset Value: 0x01*
Bit	**R/W**	**Description**	
7:0	W	SPMRT: Set Value Self Polling Mode Reference Timer The output of this timer is used as input for the On/Off Timer Incoming Periodic Time = 64/fsys Output Periodic Time= T_{RT} = (64 * SPMRT) /fsys Min: 01h = (64*1)/fsys Max: 00h = (64 * 256)/fsys	

SPMOFFT0: Self Polling Mode Off Time Register0

ADDR: 0x09		Reset Value: 0x01
Bit	**R/W**	**Description**
7:0	W	SPMOFFT: Set Value Self Polling Mode Off Time: Bit 7...Bit 0(LSB) Off Time = T_{RT} *SPMOFFT Min: 0001h = 1*T_{RT} Reg.Value 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}

SPMOFFT1: Self Polling Mode Off Time Register1

ADDR: 0x0A		Reset Value: 0x00
Bit	**R/W**	**Description**
5:0	W	SPMOFFT: Set Value Self Polling Mode Off Time: Bit 13(MSB)...Bit 8 Off Time = T_{RT} *SPMOFFT Min: 0001h = 1*T_{RT} Reg.Value 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}

SPMAP: Self Polling Mode Active Periods Reg.

ADDR: 0x0B		Reset Value: 0x01
Bit	**R/W**	**Description**
4:0	W	SPMAP: Set Value Self Polling Mode Active Periods. Min: 01h = 1 (Master) Period Max: 1Fh = 31 (Master) Periods Reg.Value 00h = 256 (Master) Periods

SPMIP: Self Polling Mode Idle Periods Register

ADDR: 0x0C		Reset Value: 0x01
Bit	**R/W**	**Description**
7:0	W	SPMIP: Set Value Self Polling Mode Idle Periods. Min: 01h = 1 (Master) Period Max: 00h = 256 (Master) Periods

2.4.7 RF Path

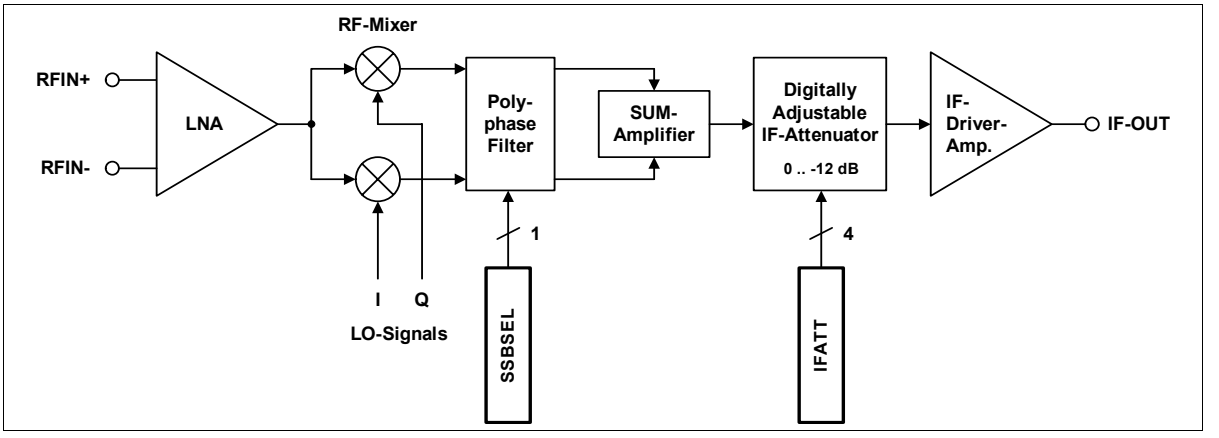

Figure 29 RF Path

RFIN+ and RFIN- are inputs to the on chip LNA.

RF is usually connected to RFIN+, and RFIN- is grounded. If a filter with differential outputs is used, such as a SAW filter, the differential inputs may be used accordingly.

The LNA directly drives the two in quadrature driven RF Mixers. The outputs of the two mixers are fed to a polyphase filter that provides active suppression of input signals at the image frequency of the desired input signal. The center frequency of the polyphase filter and the following blocks at the IF frequency is 10.7 MHz.

The RF mixer and poly phase filter are capable to support a Hi-Side and a Lo-Side LO Injection mode. Selection of the LO Injection mode is controlled via the SFR-control bit SSBSEL.

The polyphase filter is followed by a digitally adjustable IF attenuator. This allows the production spread of the on chip signal strip, of external LNA and matching circuitry and RF SAW and ceramic IF filters to be trimmed out. The attenuator offers a programmable attenuation range of 12 dB, programmable in 16 Steps and is controlled via the SFR control bits IFATT. An IF driver amplifier with a characteristic output impedance of 330 Ω allows simple interfacing to external ceramic IF filters.

For adjustment of the RSSI offset the complete RF path can be switched off via the SFR control bit RFOFF.

Selection of IF Attenuation

Use always minimum IF Attenuation (0dB). Only if there is an external LNA used, IF Attenuation should be set to the gain of the external LNA. If there is one or more SAW filters, the insertion loss should be reduced from the external LNA gain.

If strong out of band disturbers are expected, an increase of IF Attenuation may increase large signal immunity, at the cost of slight reduction in sensitivity.

RFC: RF Control Register

ADDR: 0x12			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
4	W	RFOFF: Switch off RF path (for RSSI trimming) 0: RF path enabled 1: RF path off	
3:0	W	IFATT: Adjust IF attenuation in 16 steps to trim the gain RFIN --> IF-OUT 0000: 0 dB attenuation 1111: 12 dB attenuation	

LOC: Local Oscillator Control Register

ADDR: 0x16			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:5	W	Always set to 0	
4	W	SSBSEL: Local Oscillator Injection Mode Selection 0: Lo-Side LO Injection .. use for TDA5230 1: Hi-Side LO Injection .. use for TDA5231	
3:0	W	Always set to 0	

2.4.7.1 RX-RUN/RXD Pin

The receiver enable signal is offered at the dedicated RX-RUN/RXD Pin to control external components such as an external LNA. Whenever the receiver is active, the RX-RUN output is high.

Note that the same output pin may be also configured to provide the received data in Transparent Mode.

CMC1: Chip Mode Control Register 1

ADDR: 0x03		*Reset Value: 0x00*
Bit	**R/W**	**Description**
0	W	RXRUNRXDSEL: RX-RUN/RXD Pin Function 0: RX-Run Signal out at Pin RX-RUN/RXD 1: RX-Data out at Pin RX-RUN/RXD

2.4.8 Functionality of the IF Path

2.4.8.1 IF Filter

The output of the image reject mixer is buffered by the IF driver amplifier. The signal is then filtered by one or (alternatively) two external 10.7 MHz IF filters.

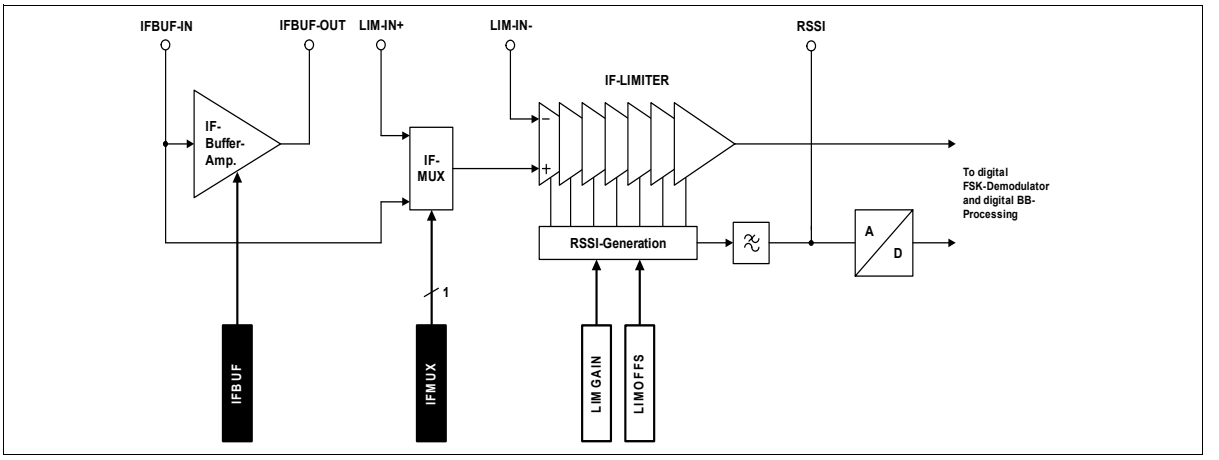

Figure 30 IF Path

For operation with one IF filter, this filter must be connected to the pins IF-OUT and LIM-IN+.

For the two filter option, the first IF filter must be connected to the pins IF-OUT and IFBUF-IN and the second filter to the pins IFBUF-OUT and LIM-IN+. The IF buffer amplifier is enabled by the bit IFBUF to drive the second IF filter.

The IF MUX allows to bypass the second IF Filter, and therefore to switch in between two different IF Filter bandwidths. The IF MUX is switched by using the bit IFMUX.

All input and output impedances seen by the IF filters (IF driver amplifier, IF buffer amplifier and IF limiter input) are designed to 330 Ω.

Selection of the IF Filter

The construction of the TDA523x allows the use low-cost standard ceramic IF filters with a center frequency of 10.7 MHz, and an input and output impedance of 330 Ω.

The recommended IF filter bandwidth is 280 kHz. See also (bill of material of the evaluation board). Wider IF Filter bandwidth is required if transmitters with high tolerance are used. Narrower IF Filter bandwidth will increase immunity to noise and improve channel separation in multichannel systems.

If bandwidth switching is required, the first IF Filter is wideband, and is used if the IF MUX is switched to IFBUF-IN. The second IF Filter is narrowband, if the IF MUX is switched to LIM-IN+, the narrow characteristic of this filter overrides the wide first IF Filter.

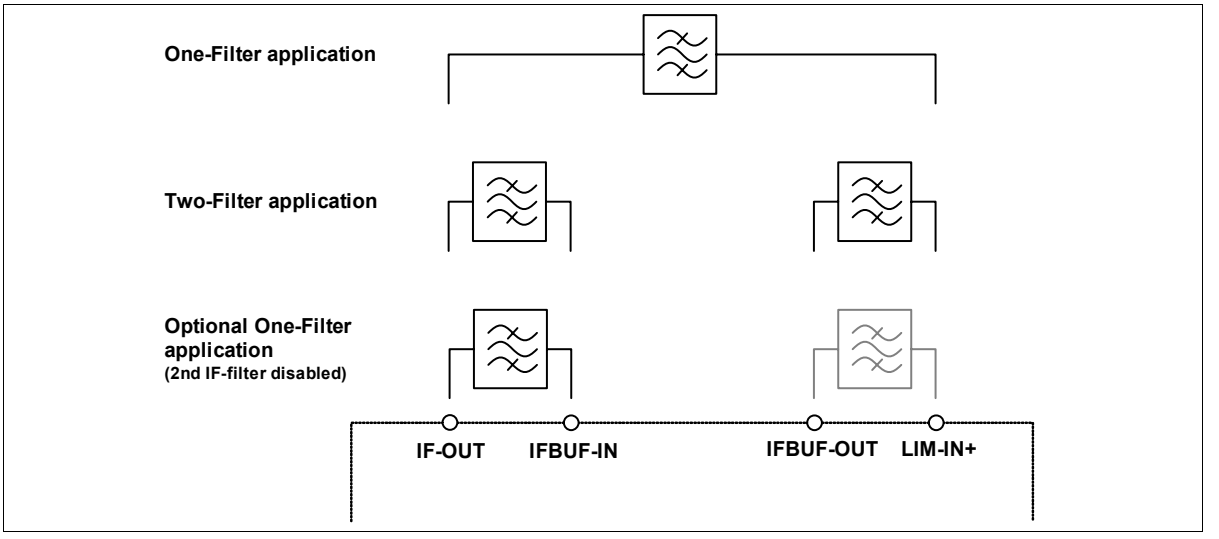

Figure 31 External IF Filter Configurations

Dual: AIF0 and BIF0: Conf.A IF Buffer Amplifier Enable

ADDR: 0x3F and 0x60		*Reset Value: 0x00*
Bit	**R/W**	**Description**
1	W	IFBUF: Enable IF Buffer amplifier 0: Buffer disabled, used for single IF filter 1: Buffer enabled, used for dual IF filter configuration
0	W	IFMUX: select IF-limiter input 0: use pin LIM-IN+ as input 1: use pin IFBUF-IN as input

2.4.8.2 Limiter, RSSI

The limiter is an AC coupled multistage amplifier with a wide bandpass characteristic centered around 10.7 MHz. The limited IF signal is fed to the digital FSK Demodulator. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator that produces a voltage signal proportional to the logarithm of the input signal level.

The RSSI signal is used to determine the relative RF input signal power of a received signal or data transmission, and for example, to estimate the transmitter distance.

RSSI can be read either from the analog output as described below, or digitally via the peak detector registers, which are described in **Chapter 2.4.8.3 RSSI Peak Detector**.

To achieve a well-defined RSSI response, the offset and the gain of the RSSI generation unit can be trimmed via the SFR control bits LIMGAIN and LIMOFFS as described later.

The bandwidth of the RSSI signal can be adapted to the data rate. It is controlled by the SFR control bits AAFILT.

This RSSI Signal can be fed to the pin RSSI via a buffer amplifier. To enable this buffer the SFR control bit RSSIMONE must be set.

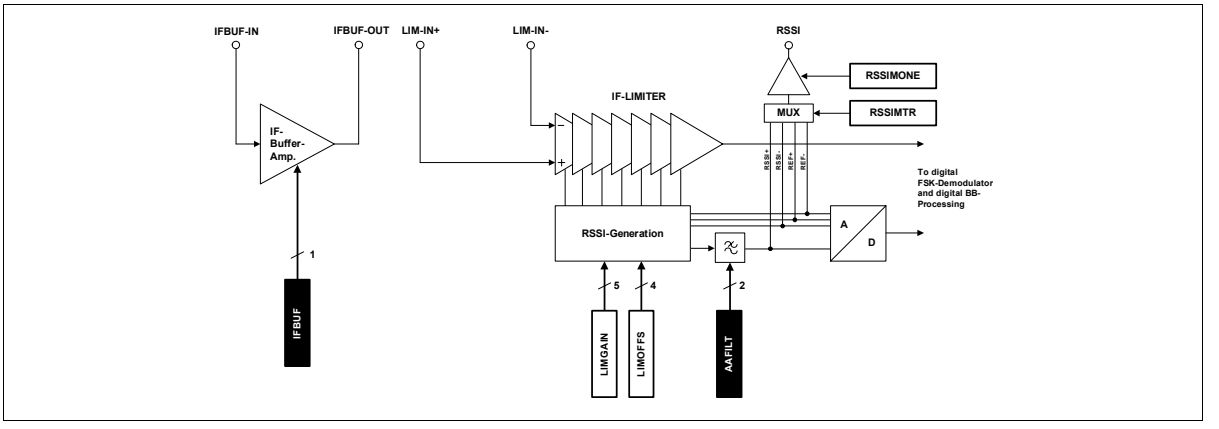

Figure 32 IF Path, RSSI

RSSI is derived from four signals. Any of these four signals (RSSI+, RSSI-, REF+ and REF-) may be routed to the pin RSSI. RSSI+ is the real RSSI signal derived from the input signal voltage, while RSSI- is an internal offset, and REF+/- is the internal voltage reference. The selection of the signal routed to pin RSSI is done by the SFR control bits RSSIMTR.

Typical values are:

RSSI-...1.55 V, REF+...1.8 V, REF-...1.3 V; these values are not influenced by trimming.

The following figure shows the behavior of RSSI+ over an input signal power sweep. The four curves show the trimming range in between minimum offset/maximum gain and maximum offset/minimum gain, the typical RSSI+ using recommended default setting of minimum offset / minimum gain (if RSSI trimming is not used), and the fourth curve represents a typical trimmed RSSI+

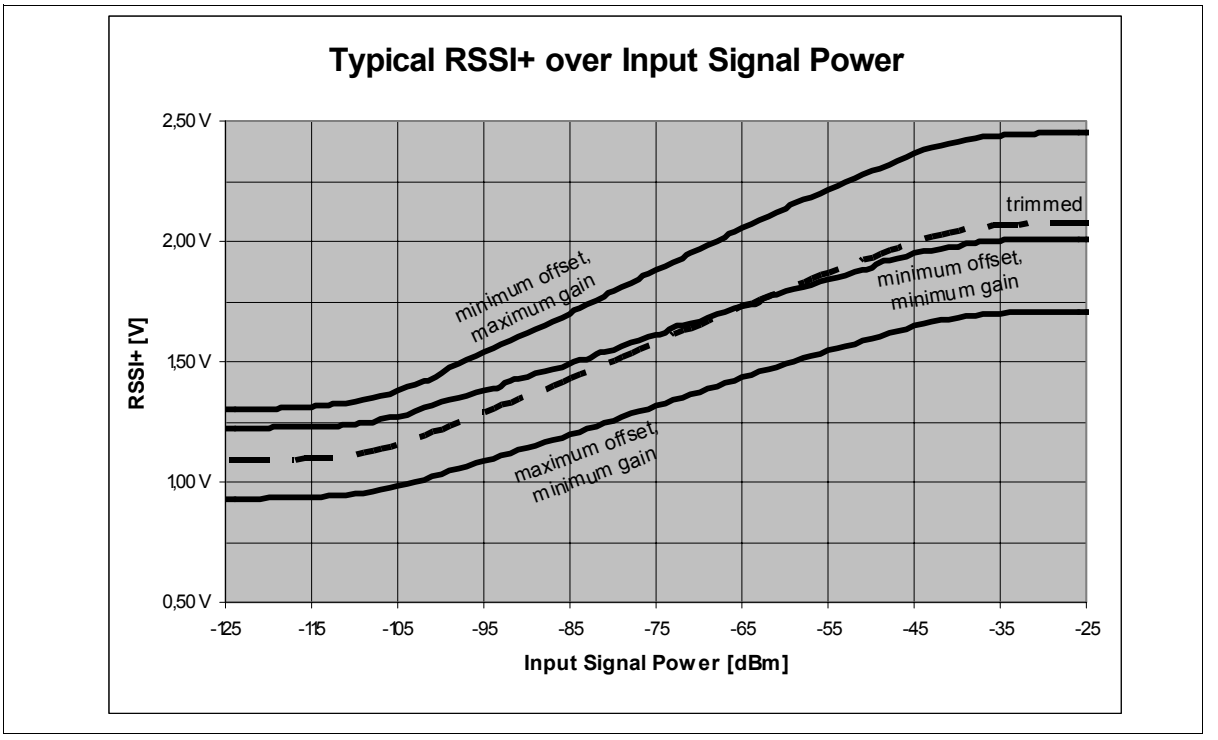

Figure 33 Typical RSSI+ over Input Signal Power

The true RSSI signal is calculated by the following rule:

$$RSSI = \left(\frac{RSSI+ \; - \; RSSI-}{REF+ \; - \; REF-}\right)$$

The result of this calculation is about -1 for no input signal (=noise), and about +1 for large input signals (e.g. -10 dBm).

The RSSI Signals are also sampled by an AD converter, with four differential input signals for the RSSI and the RSSI voltage reference. The true RSSI is automatically calculated, using the following formula and the result stretched to values from 0 to 255.

$$RSSI = \left(\left(\frac{RSSI+ \; - \; RSSI-}{REF+ \; - \; REF-}\right) + 1\right) \times \frac{1}{2} \times 255$$

The digital output of the ADC is used for processing ASK modulated data, and for two peak detectors, which are accessible via SFRs and are described in **Chapter 2.4.8.3 RSSI Peak Detector**. The range of the ADC is smaller than the range of real RSSI. It is important that the true RSSI level at noise is >-0.92, which means it is clearly inside the ADC range. Otherwise, small input signals are not recognized and sensitivity is decreased.

Accuracy is optimized by trimming true RSSI at noise level (no input signal) to a calculated value of -0.92 to 0.90 and at strong input signals (about -10 dBm) to +1.

It is recommended either to use RSSI with the default settings (minimum offset, minimum gain) or to use the following trim procedure. This guarantees optimal ASK sensitivity. It is not recommended to use trimming to increase RSSI resolution or slope.

Recommended Analog Trimming Procedure:

- Download configuration file
- Send 0x35 to the register LIMC1; this enables the RSSI buffer, selects RSSI-, and sets the RSSI offset to a middle value
- Measure RSSI- voltage at RSSI pin (26)
- Send 0x55 to the register LIMC1, REF+ is selected
- Measure REF+ voltage at RSSI pin (26)
- Send 0x75 to the register LIMC1, REF- is selected
- Measure REF- voltage at RSSI pin (26)
- Send 0x15 to the register LIMC1, RSSI+ is selected
- Measure a RSSI voltage curve at RSSI pin (26) from noise or (no input signal) to a high signal (about -10 dBm) using a continuous wave input signal.
- Normalize the curve using the formula for true RSSI earlier in this chapter
- Change LIMOFFS (LIMC1, bit 0..3) until true RSSI without input signal is between -0.92 and -0.9
- Change LIMGAIN (LIMC0, bit 0..4) until true RSSI at -10 dBm is smaller but next to +1
- The new values for LIMGAIN and LIMOFFS must be added to the configuration!

See also the Recommended Digital Trimming Procedure in **Chapter 2.4.8.3 RSSI Peak Detector**. If trimming is required it is only necessary to do either analog or digital trimming, but results of the two trimming procedures are slightly different.

Usually, it is recommended to use the digital RSSI.

Recommended applications for the analog RSSI are:

- Debugging and watching RF traffic
- External ASK demodulation
- Relative signal power measurements

If optimal accuracy is required and to reduce thermal drift, it is recommended to read all four RSSI signals (RSSI+, RSSI-, REF+ and REF-) within a few seconds.

LIMC0: Trim RSSI Gain

ADDR: 0x1B		*Reset Value: 0x0C*
Bit	**R/W**	**Description**
4:0	W	LIMGAIN: Trim the RSSI Gain (Slope) Min: 00h = Minimum gain Max: 1Fh = Maximum gain IAF TDA523x Config Tool sets this value to 00h by default

LIMC1: Trim RSSI Offset, enable RSSI pin

ADDR: 0x1C		*Reset Value: 0x15*
Bit	**R/W**	**Description**
6:5	W	RSSIMTR: Select signal for RSSI pin 00b: RSSI+ 01b: RSSI- (reference) 10b: REF+ (reference) 11b: REF- (reference)
4	W	RSSIMONE: Enable buffer for RSSI pin 0: buffer off 1: buffer on
3:0	W	LIMOFFS: Trim the RSSI Offset Min: 0h = Minimum offset Max: Fh= Maximum offset IAF TDA523x Config Tool sets this value to 0h by default

Dual: ADIGRXC and BDIGRXC: Global Settings

ADDR: 0x6C and 0x8C		*Reset Value: 0x00*
Bit	**R/W**	**Description**
2:1	W	AAFILT: Anti Aliasing Filter 00b: 40 kHz use for data rates >9.6 kb/s 01b: 13.6 kHz use for data rates >3 kb/s 10b: 5 kHz use for data rates >2 kb/s 11b: 3.6 kHz use for data rates <=2 kb/s The anti aliasing filter corner frequency can be changed to achieve better performance. Note that the corner frequency and the data rate must be set together. This value is automatically created by the IAF TDA523x Config Tool
0	W	DATINV ... Used by Data Filter

2.4.8.3 RSSI Peak Detector

As mentioned earlier, RSSI is also sampled by an ADC, delivering an 8-bit resolution. All four RSSI signals are connected to the differential inputs, and True RSSI with optimal temperature compensation is automatically generated.

The Chip possesses two digital RSSI peak level detectors. The RSSI level from the ADC is averaged over four samples before it is sent to the two Peak Detectors. This reduces the influence of single noise peaks.

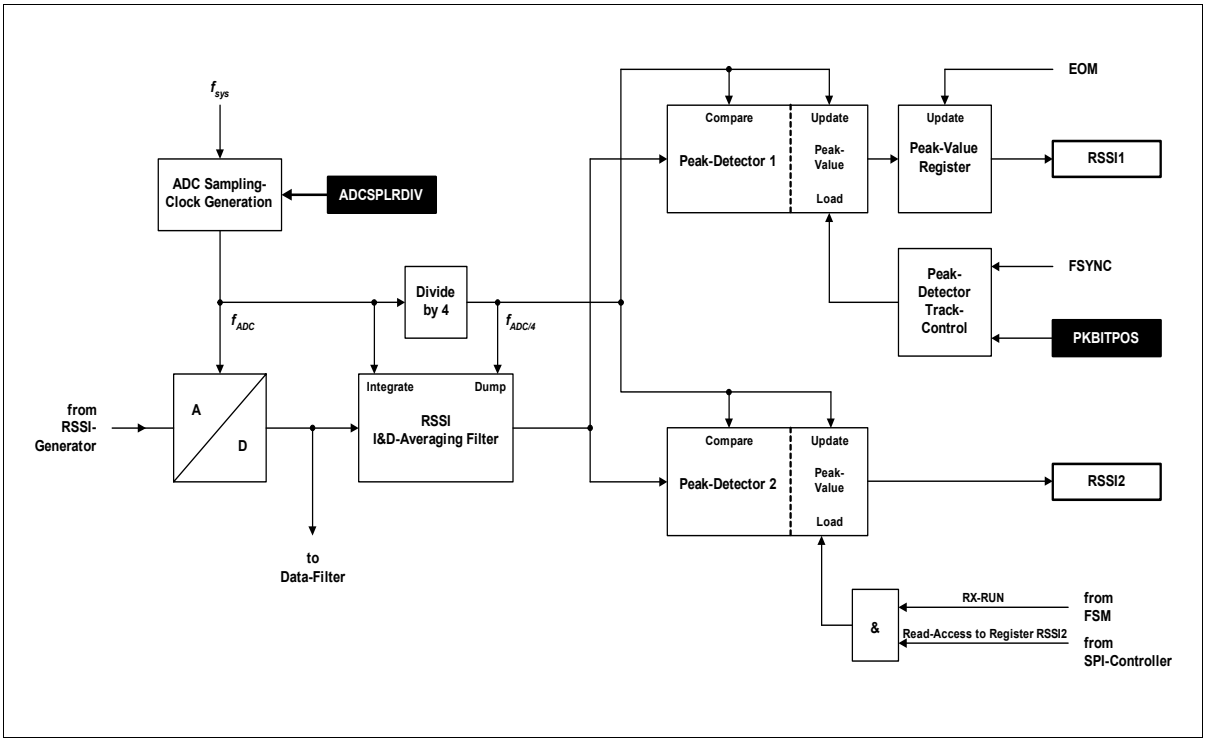

Figure 34 Peak Detector Unit

Peak Detector 1 is used to measure the input signal power of a received and accepted data telegram. It is read via SFR RSSI1.

Observation of the RSSI signal starts at the detection of a TSI (FSYNC) and ends with the detection of EOM. The internal RSSI1 value is cleared after FSYNC. The evaluated RSSI peak level RSSI1 is transferred to the RSSI1 register at EOM. Starting the observation of the RSSI level can be delayed by a selectable number of data bits and is controlled by the register PKBITPOS. A latency in the generation of FSYNC and EOM of approx. 2..3 bits in relation to the contents of the Peak Detector must be considered. Within the boundaries described, the register RSSI1 always contains the peak value of the last completely received data telegram. The register RSSI1 is reset to 0 at power up reset only.

Peak Detector 2 is used to measure RSSI independent of a data transfer and to digitally trim RSSI. It is read via SFR RSSI2.

Observation of the RSSI signal is active whenever the RX-RUN signal is high. The RSSI2 register is refreshed and Peak Detector 2 is reset after every read access to RSSI2.

It may be required to read RSSI2 twice to obtain the required result. This is because, for example, during a trim procedure input signal power is reduced, after reading RSSI2, the peak detector will still hold the higher RSSI level. After reading RSSI2 the lower RSSI level is loaded into the Peak Detector, and can be read by reading RSSI2 again.

When the RX-RUN signal is inactive, a read access has no influence to the peak detector value. The register RSSI2 is reset to 0 at power up reset.

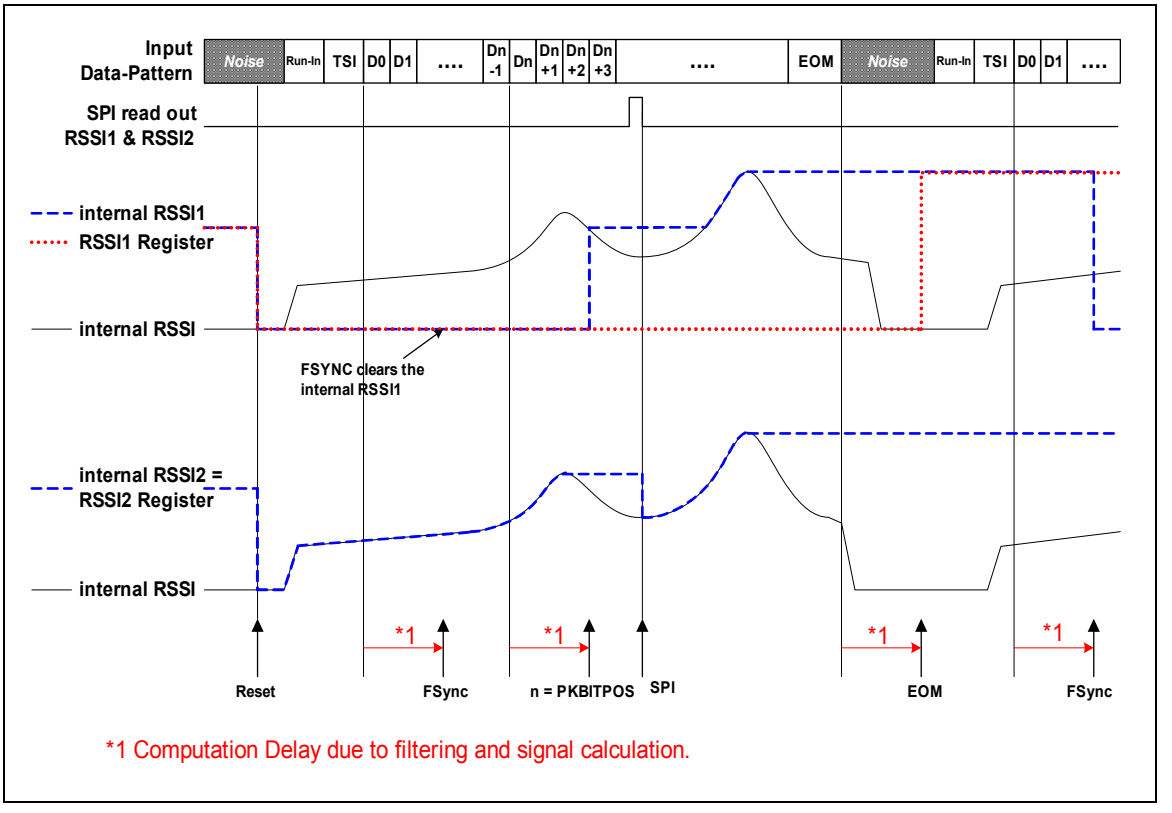

Figure 35 Peak Detector Behavior

The following figure shows the typical behavior of the digital RSSI. Three curves show the typical trimming range, the typical default RSSI, and the fourth curve shows a typically trimmed RSSI.

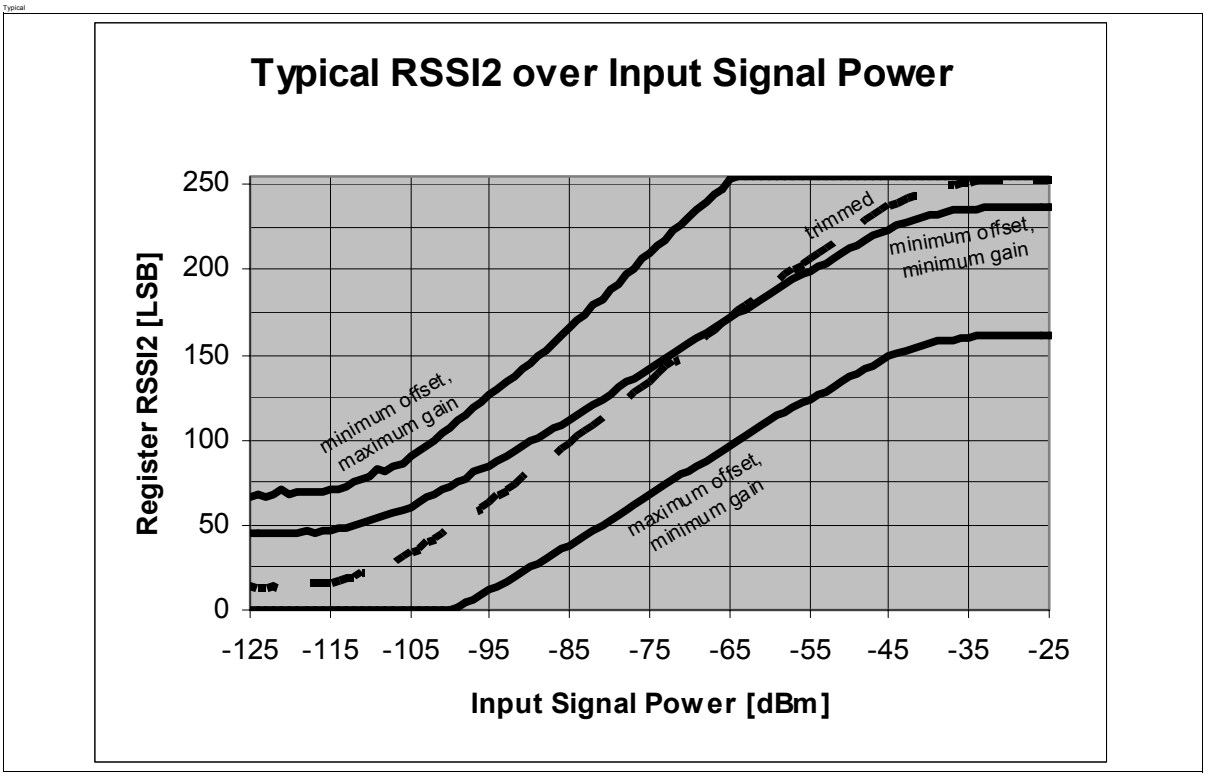

Figure 36 Typical Digital RSSI over Input Signal Power

Recommended Digital Trimming Procedure:

- Download configuration file (Run Mode Slave, LIMGAIN, LIMOFFS set to minimum)
- Switch off RF Path by setting register RFC to 0x1F.
- Read RSSI2 eleven times (minimum 10 ms in between readings), use average of last ten readings (always)
- Change LIMOFFS till RSSI2 readings with no input signal are between 0x02 and 0x05 or closest to the upper value
- Set register RFC to 0x0**z** to switch on RF-Path (**z** stands for the selected value for IF Attenuation. See **Chapter 2.4.7 RF Path**. If IF Attenuation is trimmed, this has to be done before trimming of RSSI.).
- Change LIMGAIN till RSSI2 readings at -10 dBm are between 0xFC and 0xFE or closest to the lower value.
- The new values for LIMGAIN and LIMOFFS have to be added to the configuration!

It is only necessary to use either analog or digital trimming. The results between analog and digital trimming may differ. Therefore the same procedure should always be used.

RSSI1: Peak Detector 1 read register

ADDR: 0xAC		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	R	RSSI1: peak level during payload Tracking started after FSYNC + PKBITPOS Set at EOM Cleared at Reset and FSYNC

RSSI2: Peak Detector 2 read register

ADDR: 0xAD		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	C	RSSI2: peak level. Tracking is active when Digital Receiver is enabled Set at higher peak levels than stored Cleared at Reset and SPI read out

2.4.9 Digital Receiver

The functionality of the Digital Receiver (DigRX) is divided into three consecutive data processing stages: the Data Filter, the Clock and Data Recovery and the Framer Synchronization Unit. The architecture of the Digital Receiver is optimized for processing Manchester-coded data streams. The figure below shows all the symbol combinations. Digital 0 and 1 are coded with the change of the amplitude in the middle of the symbol period. The Code Violations (CV) M (mark) and S (space), are coded as low/high signal levels. Generally, the Digital Receiver can handle one single CV following four valid Manchester-coded data bits

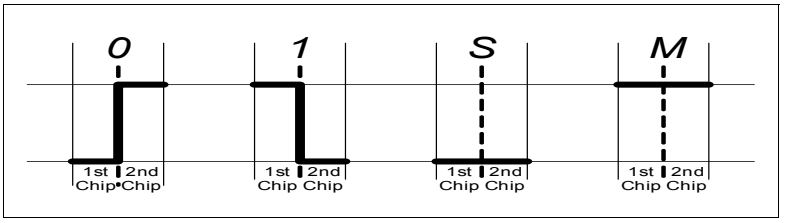

Figure 37 Manchester Code

The basic structure of a telegram frame is shown in the figure below. The protocol starts with RUNIN. The RUNIN with the minimum length of four manchester coded symbols is used for internal filter setting and frequency adjustment. The TSI (Telegram Start Identifier), which is used as framing word, follows the RUNIN sequence. The payload contains the effective data. The length of the valid payload data is defined as the length itself or additional criteria (e.g. loss of Sync).

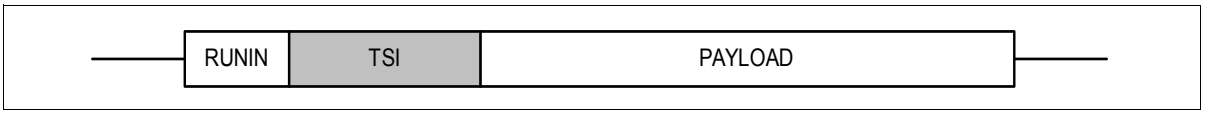

Figure 38 Frame

2.4.9.1 Synchronization Search Time and Inter-Frame Time

Two important system parameters will be described in this chapter: the Synchronization Search Time Out (SYSRCT0) and the Inter-Frame Time. The processing sequence of a telegram is shown below.

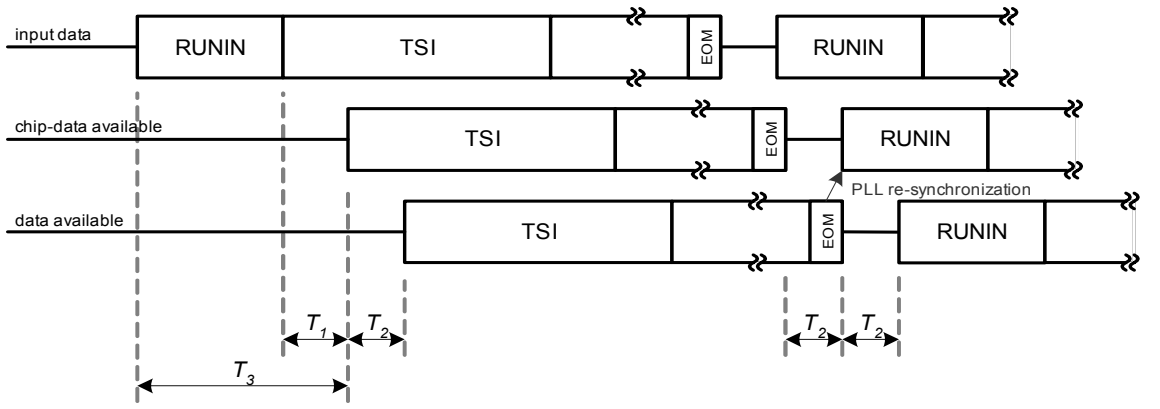

Figure 39 Data Latency

The synchronization search time T_3 is the time the receiver requires for a search for a pattern in an incoming data stream. The minimum value of the search time out length is the consequence of the system latency time T_1 and RUNIN length.

The overall system latency time is calculated in two steps: T_1 is the delay between ADC input and the filter output (chip data available), and T_2 is the time between the Slicer input and the Framer output (decoded data available).

T_1 latency time include: (T_1 = 2 2/16 T + 0.5 T)[1)]

- matched filter computation time
- signal detector delay

T_2 latency time include: (T_2 = 1.5 T to 2.0 T)

- Data Slicer computation time
- Framer computation time. The 0.5 T spread is caused by the internal Framer circuit quantization behavior.

This means, that for the minimum length of the SYSRCT0, the value 2 2/16 bits plus 0.5 bits, plus the RUNIN length, which is set in the CDR2 register, plus 1.5 bits (to consider worst case RUNIN patterns) have to be used. To reach all data rate and duty cycle errors 10% of the overall sum must be added.

$$SYSRCT0 = roundup(((RUNIN + 2{,}125 + 2) \cdot 16) \cdot 1{,}1)$$

1) T..nominal duration of one data bit

Based on the recommended value of 3.5 bits for the RUNIN, the recommended setting for SYSRTC0 = 0x87. **This value is automatically used by the IAF TDA523x Configuration Tool!**

Dual: ASYSRCT0 & BSYSRCT0: Synchronization search time out

ADDR: 0x76 & 0x96			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	SYNCTO: Synchronization search time out[1)] FFh: 15 15/16 bit 00h: 0 bit	

1) the value should be set in T/16 steps

A Second important system parameter which must be considered, is the minimal Inter-Frame Time (time in between two data frames). This time is equal to the T_2 time and has a length of 2 bits. The EOM to PLL re-synchronization time is negligible (this time is T/16 bit), and the system delay T_1 is irrelevant, because of the EOM signal is used for PLL re-synchronization only.

Note that the described Inter-Frame Time is based on the input pattern with equal signal power in the following telegram, in other cases the Inter-Frame Time can vary from the calculated value.

2.4.9.2 Data Filter and Signal Detection

The Digital Receiver processes input signals from the digital FSK Demodulator as well as from the A/D-converted output signal of the RSSI generator used for ASK modulated data signals. Input selection of the Digital Receiver is done by a multiplexer, which is controlled by the Master Control Unit via the control signal Modulation Type. An optional Pre-Slicer Unit may be activated in certain ASK applications to further increase the jammer performance of the receiver.

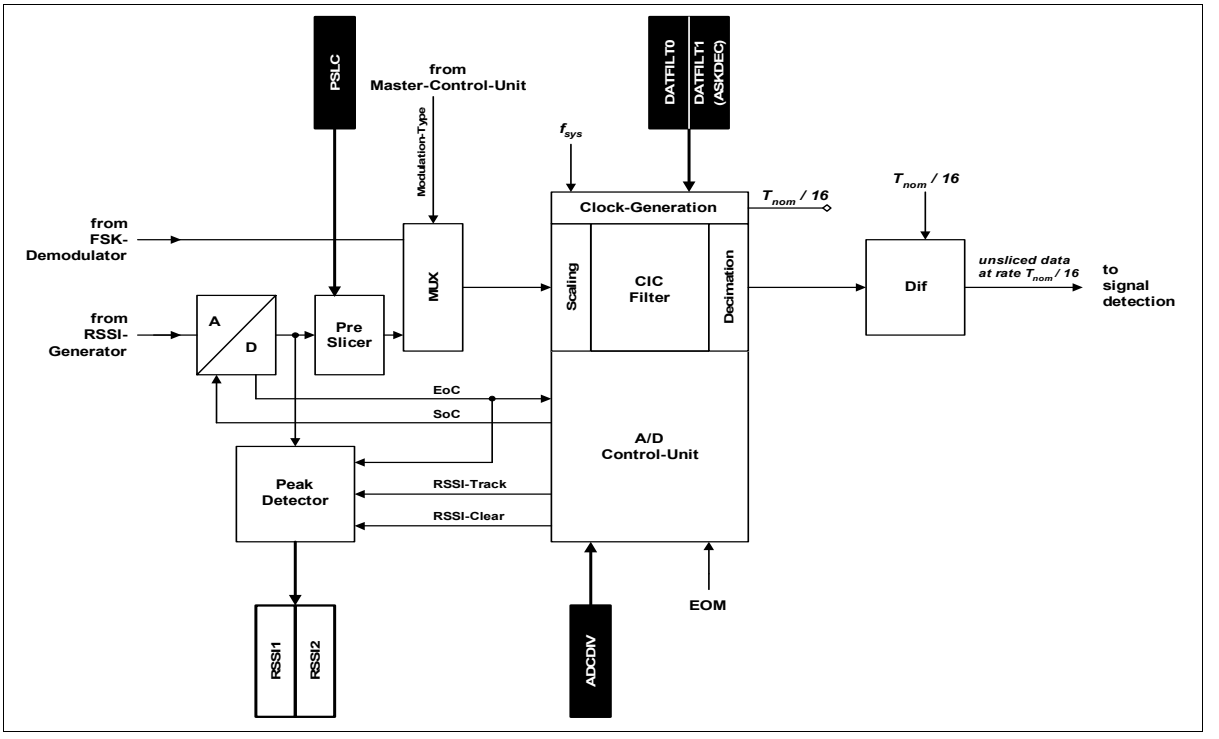

Figure 40 AD-Control and Matched-FIlter

AD Converter:

The AD sampling rate division factor ADCDIV is always a multiple of 16 times of the data rate, and in a range from 96 kHz to 320 kHz. For example for a 2 kb/s data rate the ADC sampling rate has to be a multiple of 32 kHz, the optimal ADC sampling rate is 320 kHz.

Because of f_{SYS} and the used clock divider, not all ADC sampling rates are possible. Therefore, there is an ideal sample rate (e.g. 320 kHz) and finally a real sample rate (322.576 kHz, note: values slightly higher than 320 kHz are tolerated if calculated by the IAF Tool). The difference between the ideal and the real sample rate should not be more than 2%. For better performance, the highest possible ADC sampling rate should be set.

For data rates lower or equal to 1.1kb/s a maximum sample rate of 120 kHz should be selected.

A data decimation is required to correct the values which are dependent on the factor of oversampling.

The calculation formulas for ADCDIV / ASKDEC factors:

The following calculations are fully supported by the IAF TDA523x Configuration Tool!

$$ADCDIV = round\left(\frac{f_{sys}}{f_{ADC}}\right) - 1 \Big|_{f_{ADC} = [96 \ldots 320kHz]}$$

$$ASKDEC = round\left(\frac{f_{ADC}}{16 \cdot f_{data}}\right) - 1 \Big|_{f_{ADC} = \frac{f_{sys}}{ADCDIV + 1}}$$

Dual: ADCSPLRDIV and BDCSPLRDIV: ADC dividing factor

ADDR: 0x6D and 0x8D		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	ADCDIV: ADC sampling rate division factor.

Dual: ADATFILT0 and BDATFILT0: Matched Filter Scaling and Delay

ADDR: 0x6F and 0x8F		*Reset Value: 0x00*
Bit	**R/W**	**Description**
5:3	W	ASKSCA: CIC-filter Input Scaling Factor[1)] 000b: default
2:0	W	ASKDEL: CIC-filter comb Section delay Factor[1)2)] use always 110b

1) use default value

2) the CIC filter delay = ASKDEL + 1

Dual: ADATFILT1 and BDATFILT1: Matched Filter Decimation

ADDR: 0x70 and 0x90		*Reset Value: 0x00*
Bit	**R/W**	**Description**
5:0	W	ASKDEC: CIC filter Decimation Factor

Matched Data Filter

The CIC Filter together with the DC-offset canceller (realized as differentiator) is a matched filter for one manchester coded bit.

The Matched Data Filter has two major tasks: to reconstruct Manchester-coded data of the correct data rate, and to deliver a “quality” value, the so-called ASKNP value.

The higher the output of ASKNP, the better the reliability of the related data bit. The signal detector uses this value to distinguish between acceptable data and unacceptable data (e.g. noise).

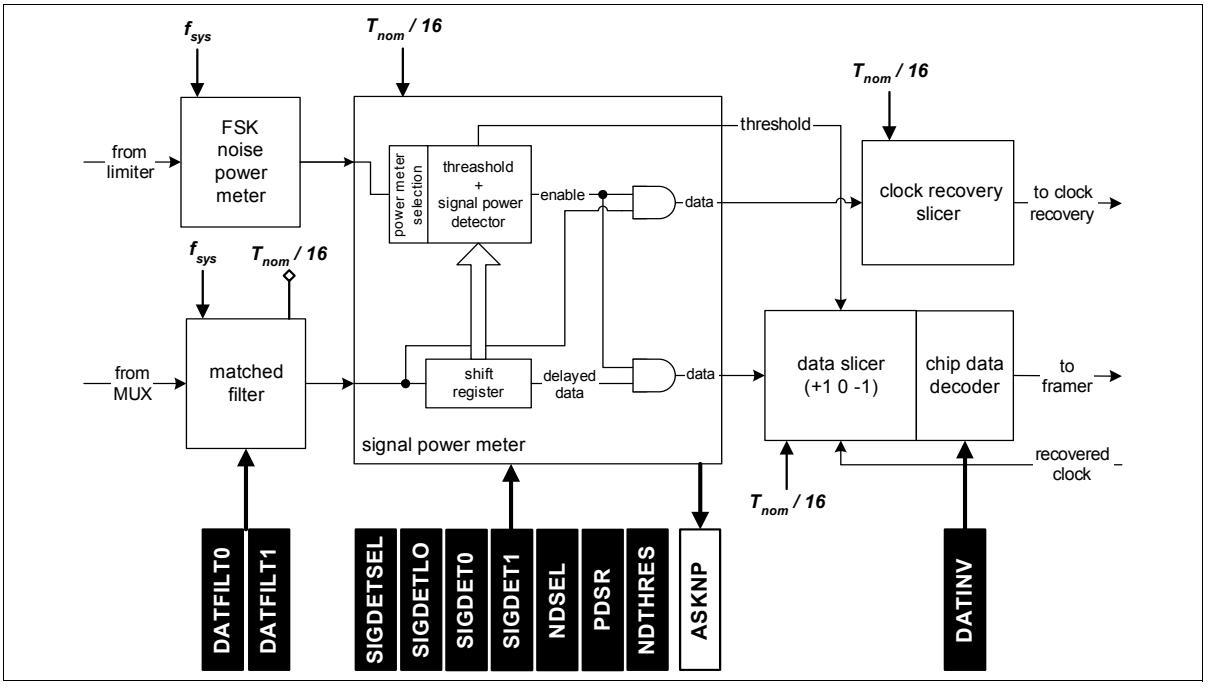

Figure 41 Matched Filter, Signal/Noise Detection and Slicer units

The polarity of the Manchester code can be inverted by setting the SFR control bit DATINV.

Signal and Noise Detector

The Signal and the Noise Detector compare the outputs of ASKNP and FSKNP (see FSK Demodulator) with configurable thresholds.

The Signal Detection Mode must be configured based on whether ASK or FSK modulation is used:

- Signal power detection (=Squelch) only (related registers SIGDET0, SIGDET1 and ASKNP). This mode is generally used for ASK and recommended for FSK.
- Noise power detection only (related registers NDTHRES and FSKNP).
- Signal and noise power detection simultaneously.
- Signal and noise power detection simultaneously, but the FSK noise detect signal is valid only if the SIGDETLO threshold is exceeded. This is the recommended FSK mode, if minimum FSK Deviation is not sufficient to use signal power detection only.

The next diagram shows the system characteristics to consider in choosing the best Signal Detector level. On the one hand, achieving good FAR (False Alarm Rate) performance that a higher threshold level must be set, but the MER/BER (Message Error Rate/Bit Error Rate) performance (high SIGDET level signal) will decrease. On the other hand, the MER/BER performance can be increased by setting smaller threshold levels but then the FAR performance (low SIGDET level signal) will worsen.

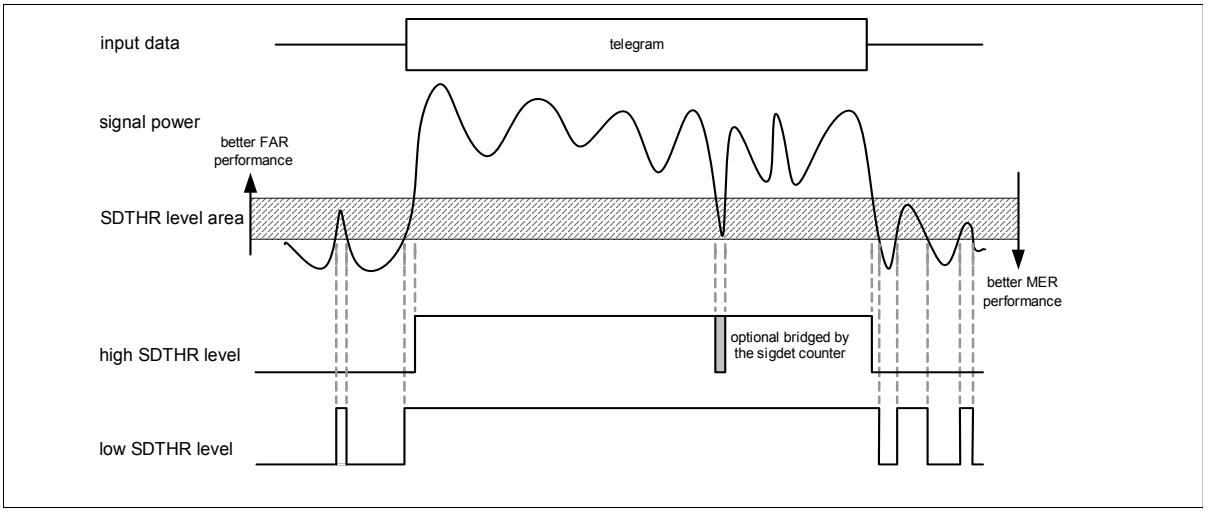

Figure 42 Signal Detection Threshold Level

Quick Procedure to Determine Signal and Noise Detector Thresholds:

Preparation

A set up is required with original RF hardware as in the final application. The values of ASKNP and FSKNP can be read via the final application or using the TDA523x Explorer.

A complete configuration file using right modulation, data rate and Run Mode Slave, must be prepared using the IAF TDA523x Configuration Tool and downloaded to the TDA523x.

Signal Detector Threshold for ASK

Take 500 readings of ASKNP (50 are also possible, but this leads to less accurate results) with no RF input signal applied (=noise only). Calculate average and Standard Deviation (automatically done by TDA523x Explorer). Signal Detector Threshold is average plus 2 times the standard deviation. To load the SIGDET register the calculated value must be rounded and converted to hexadecimals. For a final application, the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.

Signal and Noise Detector Thresholds for FSK

Signal Detector Threshold

Do 500 (50) readings of ASKNP with no RF input signal applied (=noise only). Calculate average and Standard Deviation (automatically done by TDA523x Explorer). Signal Detector Threshold is average plus 2 times the standard deviation. Of course this value has to be rounded and converted to hexadecimals. For a final application the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.

Verification if Squelch only is possible

Apply a bit pattern (e.g.PRBS9) with correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of ASKNP calculate average minus three times the Standard Deviation. This value should be higher than the calculated Signal Detector Threshold calculated above. If this is not the case, Signal Detector AND Noise Detector must be used.

Noise Detector Threshold

Do 500 (50) readings of FSKNP with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Noise Detector Threshold is average minus the standard deviation. Round this value and convert it to hexadecimals. For a final application, the Noise Detector Threshold should be varied to optimize false alarm rate and sensitivity.

Signal Detector Low Threshold:

The Signal Detector Low Threshold is always required in combination with the Noise Detector.

Set register bit SDLORE to 1. Apply a bit pattern (e.g.PRBS9) at correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of ASKNP calculate average. Change SDSELLO till average is smaller than 50d (0x32). SIGDETLO = 0.8 * (average - 3 * standard deviation). Set register SDLORE back to 0. The last setting of SDSELLO has also to be used for configuration!

Verification

Threshold settings should be verified by testing receiver sensitivity over the input frequency range, with a steps size of 100Hz, at minimum FSK deviation with all combinations of minimum and maximum data rate and duty cycle.

A detailed description of the suggested procedure to determine the signal and noise detector thresholds for user specific applications can be found in the application notes *“How to choose an Application specific Signal Detection Threshold for TDA523x based ASK Mode Applications”* and *“How to Choose an Application Specific Signal- and Noise-Detection Threshold for TDA523x based FSK Mode Applications”*.

Dual: ASIGDET0 and BSIGDET0: Signal detector (Run Mode)

ADDR: 0x71 and 0x91		*Reset Value: 0x00*
Bit	**R/W**	**Description** (For detailed procedure, refer to Application note.)
7:6	W	SDCNT: Signal Detector Threshold Counter (Run Mode) 00b: disabled
5:0	W	SDTHR: Signal Detector Threshold Level (Run Mode)

Dual: ASIGDET1 and BSIGDET1: Signal detector (Wake Up)

ADDR: 0x72 and 0x92		*Reset Value: 0x00*
Bit	**R/W**	**Description** (For detailed procedure, refer to Application note.)
7:6	W	SDCNT: Signal Detector Threshold Counter (Run Mode) 00b: disabled
5:0	W	SDTHR: Signal Detector Threshold Level (Wake Up)

Dual: ANDCONFIG and BNDCONFIG: FSK Noise Detector configuration

ADDR: 0x81 and 0xA1		*Reset Value: 0x00*
Bit	**R/W**	**Description**
5:4	W	NDSEL: FSK Noise Detector Selection 00b: Squelch only (signal power) 01b: FSK Noise Detector only (noise power) 10b: Both (Squelch and FSK Noise Detector) 11b: Squelch and (FSK Noise Detector and SIGDETLO threshold)
3:2	W	ND(3:2): FSK Noise Detector configuration:: threshold level always 01b
1:0	W	ND(1:0) FSK Noise Detector configuration: Peak Detector slew rate always 11b

Dual: ASIGDETLO and BSIGDETLO: Signal Detector Threshold Low Level

ADDR: 0xB6 and 0xB7		*Reset Value: 0x00*
Bit	**R/W**	**Description** (For detailed procedure refer to Application note.)
7	W	SDLORE: Source selection of ASK Noise Power status register 0: ASK Noise for SIGDET0/1 1: Signal for SIGDETLO If enabled, the SIGDETLO level can be read out with ASKNP status register
6	W	SDSEL: Manual selection of SIGDET range 0: Disable (default) - SIGDET0/1 range selection factor automatically done; depending on datarate 1: Enable - Use SIGDETSEL control to set the valid range
5:0	W	SDLOTHR: Signal Detector Threshold Low Level. This threshold level is only valid, if the FSK Noise detector selection in the NDCONFIG register is set to “11b”

Dual: ASIGDETSEL and BSIGDETSEL: Signal Detector Factor selection

ADDR: 0xB8 and 0xB9		*Reset Value: 0x0A*
Bit	**R/W**	**Description**
3:2	W	SDSELLO: SIGDETLO range selection factor 00b: 2 01b: 4 10b: 6 (default value) 11b: 8 The selected signal detector value is divided by the 2^range selection factor. Use the correct setting to fit the measured ASKNP value.
1:0	W	SDSEL: SIGDET0/1 range selection factor 00b: 4 01b: 6 10b: 8 (default value) 11b: 10 The selected signal detector value is divided by the 2^range selection factor. Use the correct setting to fit the measured ASKNP value.

2.4.10 Digital FSK Demodulator

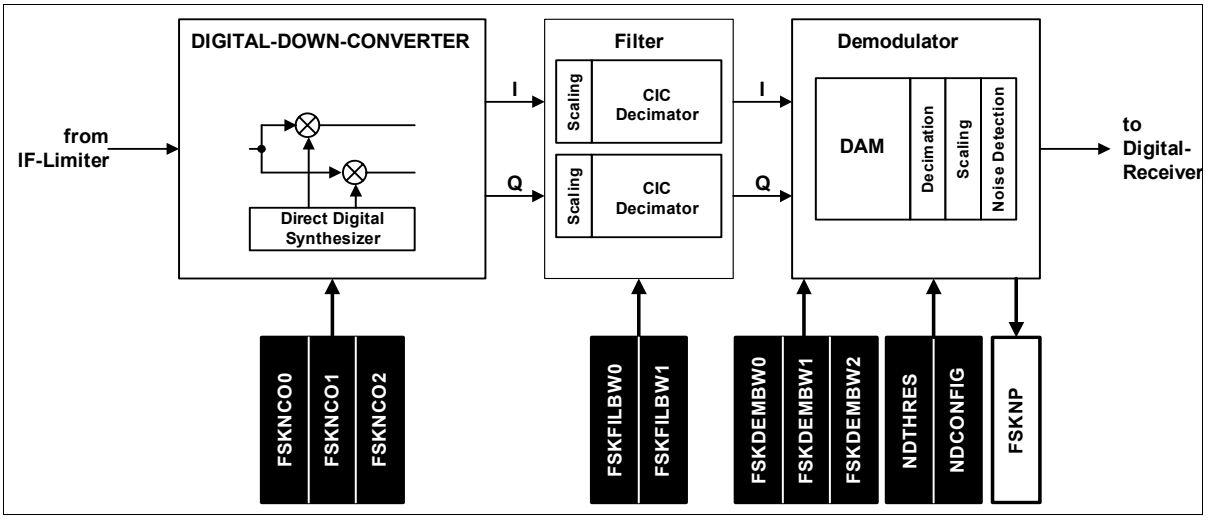

Figure 43 Digital FSK Demodulator

The Digital FSK Demodulator has three major units:

- Digital Down Converter
- CIC Filter
- Demodulator

Digital Down Converter

The output signal of the limiter amplifier at an IF-center-frequency from 10.7 MHz is converted to near baseband by an I/Q mixer, driven from a programmable Direct Digital Synthesizer.

The programming of the Direct Digital Synthesizer is done with the registers FSKNCO0, FSKNCO1 and FSKNCO2.

NCO value calculation:

TDA5230:

For Lo-Side LO Injection mode operation:

$$NCO_{dec} = round\left[2^{24} * \frac{\frac{f_{SYS}}{4} - (f_{SYS} - f_{IF})}{f_{SYS}}\right]$$

TDA2531:

For Hi-Side LO Injection mode operation:

$$NCO_{dec} = round\left[2^{24} * \frac{\frac{5 * f_{SYS}}{4} - f_{IF}}{f_{SYS}}\right]$$

This value must be converted to HEX Format and written to the registers FSKNCO2 FSKNCO1 and FSKNCO0, where FSKNCO2 is the MSB register.

The calculation above is fully automatically performed by the IAF TDA523x Configuration Tool!

Dual: AFSKNCO0 and BFSKNCO0: FSK DDS NCO Frequency Offset

ADDR: 0x78 and 0x98			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	NCOINC: FSK NCO Register Bits (7:0) LSB	

Dual: AFSKNCO1 and BFSKNCO1: FSK DDS NCO Frequency Offset

ADDR: 0x79 and 0x99			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	NCOINC: FSK NCO Register Bits (15:8)	

Dual: AFSKNCO2 and BFSKNCO2: FSK DDS NCO Frequency Offset

ADDR: 0x7A and 0x9A			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	NCOINC: FSK NCO Register Bits (23:16) MSB NCO value calculation (for the register FSKNCO0, FSKNCO1 and FSKNCO2)	

CIC Filter

The CIC Decimation Filter is used for bandwidth reduction. The selectable pre-filter bandwidths are identified in the following table:

The selection is done with the registers FSKFILBW0 and FSKFILBW1.

Setting	Typical 3dB Bandwidth[1)]	FSKDEC Setting
+/-250	+/-80kHz	0001b **recommended**
+/-125	+/-50kHz	0011b
+/-62.5	+/-40kHz	0111b
+/-31.25	+/-20kHz	1111b

1) Values are only ”about” values and should be used for orientation only. Bandwidth is also dependent on IF Filter, FSK Deviation, Data Rate and different configuration settings.

THe CIC-Filter also requires a comb delay and a scaling. For the comb delay, a value of 8 must be used.

The scaling is calculated as below:

$$SCA = 14 - round\left[\log_2(R * M) + 4\right]$$

SCA... Scaling

R...Decimation Factor(=FSKFILBW0+1)

M...Comb Delay Value(=8 +1= 9)

The calculation above is fully automatically performed by the IAF TDA523x Configuration Tool!

Dual: AFSKFILBW0 and BFSKFILBW0: FSK Pre Filter Decimation

ADDR: 0x7B and 0x9B		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3:0	W	FSKDEC: FSK Pre Filter Decimation Factor 0001b: ±250 prefilter bandwidth .. recommended 0011b: ±125 prefilter bandwidth 0111b: ±62.5 prefilter bandwidth 1111b: ±31.25 prefilter bandwidth

Dual: AFSKFILBW1 & BFSKFILBW1: FSK Pre Filter Scaling

ADDR: 0x7C & 0x9C		Reset Value: 0x00
Bit	**R/W**	**Description**
6:4	W	FSKSCA: FSK Pre Filter Scaling
3:0	W	FSKDEL: FSK Pre Filter Comb Delay Setting use 1000b

FSK Demodulator:

The FSK Demodulator is based on a delay and multiply principle (DAM). The required settings are the DAM delay, the decimation factor (IDDEC) of the data filter and a final scaling (ID scaling).

ID decimation:

$$IDDEC = round\left[\frac{f_{SYS}}{16 * R_{FSKCIC} * R_{Datafilter} * f_{Data}}\right] - 1$$

IDDEC...Integrate and Dump decimation

RFSKCIC...Decimation Factor FSK CIC Filter(=FSKFILBW0+1)

RDatafilter...Decimation Factor Data filter(=DATFILT1+1)

f_{Data}...Datarate

ID scaling:

$$IDSCA = floor(\log_2(IDDEC + 1))$$

IDSCA...Integrate and Dump scaling

IDDEC...Integrate and Dump decimation(=FSKDEMBW1)

The calculations above are fully automatically performed by the IAF TDA523x Configuration Tool!

Dual: AFSKDEMBW0 and BFSKDEMBW0: FSK Demodulator Sensitivity

ADDR: 0x7D and 0x9D			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:4	W	not used	
3:0	W	DAMDLY: FSK Demodulator Sensitivity use 0100b	

Dual: AFSKDEMBW1 and BFSKDEMBW1: FSK DAM Output Decimation

ADDR: 0x7E and 0x9E			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	W	DAMDEC: FSK DAM Decimation	

Dual: AFSKDEMBW2 and BFSKDEMBW2: FSK DAM Output Scaling

ADDR: 0x7F and 0x9F			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
3:0	W	DAMSCA: FSK DAM Output Scaling	

Noise Detector:

To decide whether there is a data signal or simply noise at the output of the demodulator, there is a noise detector implemented. The principle is based on a power measurement of the demodulated signal. The current noise power is stored in the FSKNP register and is updated at every SPI controller access.

The Noise Detector is useful if data signal is transmitted with small FSK deviations.

Further information about the use of the Noise Detector is found in ***Chapter 2.4.9.2 Data Filter and Signal Detection***.

2.4.11 Clock Recovery

The Clock Recovery uses the peak from the matched filter as reference and generates the recovered clock. The second main functionality is the generation of the symbol synchronization found indication. This generally happens within the first 4 bits.

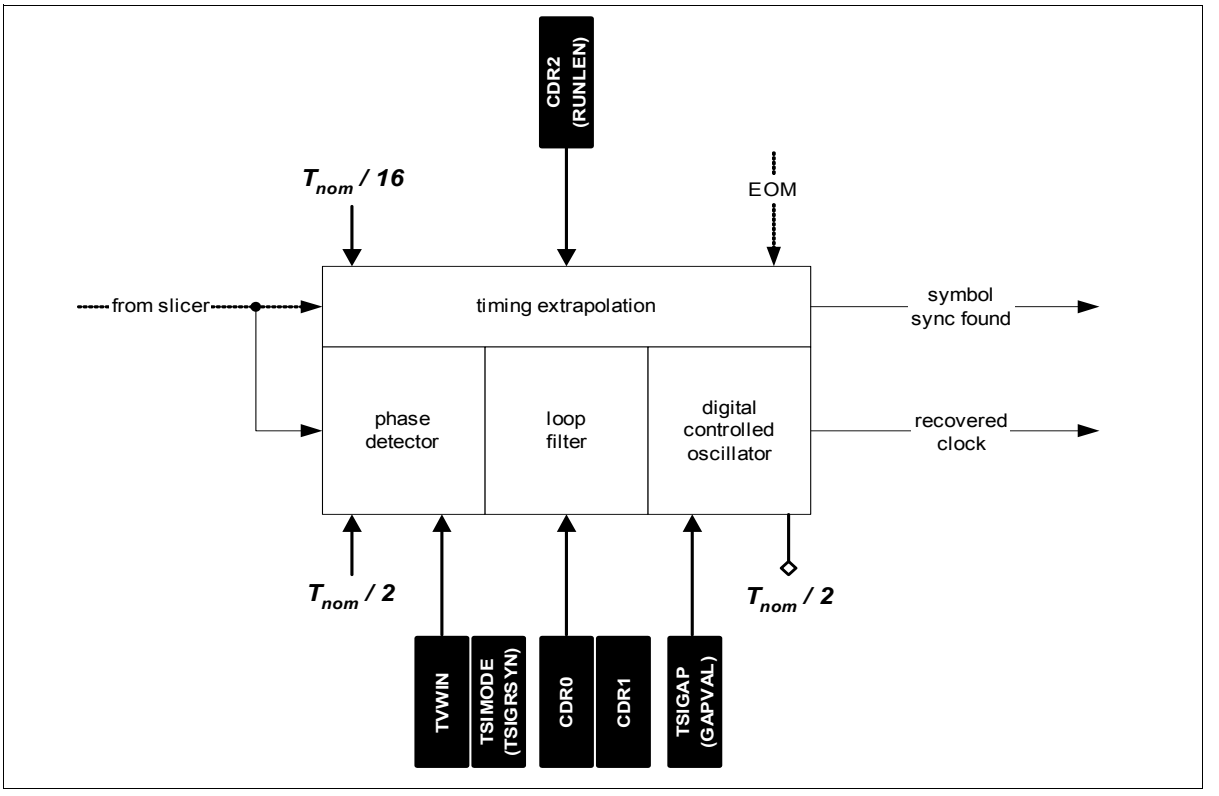

Figure 44 Clock Recovery (ADPLL)

Clock-Recovery is realized as standard ADPLL[1)] PI-regulator with Timing-Extrapolation Unit for fast setting.

The Clock Recovery locks after 4 correct Manchester coded bits, independent of duty cycle (35%, 65%) and data rate (+10%, -10%). After locking, the clock must be stable and has to follow the reference input. Therefore, a rapid setting procedure and a slow PLL are achieved.

If the PLL is locked the reference signal from the Clock Recovery Slicer is used in the phase detector block to compute the actual error. The error is used in the PI loop filter to set the digital controlled oscillator running frequency. For the P, I and Timing Extrapolation Unit settings the default values for the CDR0 and CDR1 control registers should be used.

In the unlocked state, the Timing Extrapolation Unit calculates the frequency offset for the incoming data stream. If 4 correct Manchester coded bits are detected, the RUNIN length can be set in the CDR2 register, the I-part and the PLL oscillator will be set and the PLL will be locked.

1) All Digital PLL

The PLL will be unlocked if a code violation of more than the defined length is detected, which is set in the TVWIN control register. An other criterion for PLL re-synchronization is an End Of Message (EOM) signalled by the Framer block.

The PLL oscillator generates the Manchester clock (2 * f_{data}).

The internal PLL lock signal used by the Framer is generated up to 1 bit before RUNIN ends. The timing extrapolation unit counts the incoming edges and interprets the delay between two edges as a bit or a chip. Due to the fact that the first edge of a low bit, coded as ’0’ and ’1,’ rises one Chip later than a “High” Bit, the PLL locks later in this cases. This can be seen in the figure below. The real needed RUNIN time can be shorter than the configured RUNIN length in the CDR2 register by up to two chips. This should be considered when setting the TSI Pattern and/or TSI length. See also **Chapter 2.4.13 Frame Synchronization**

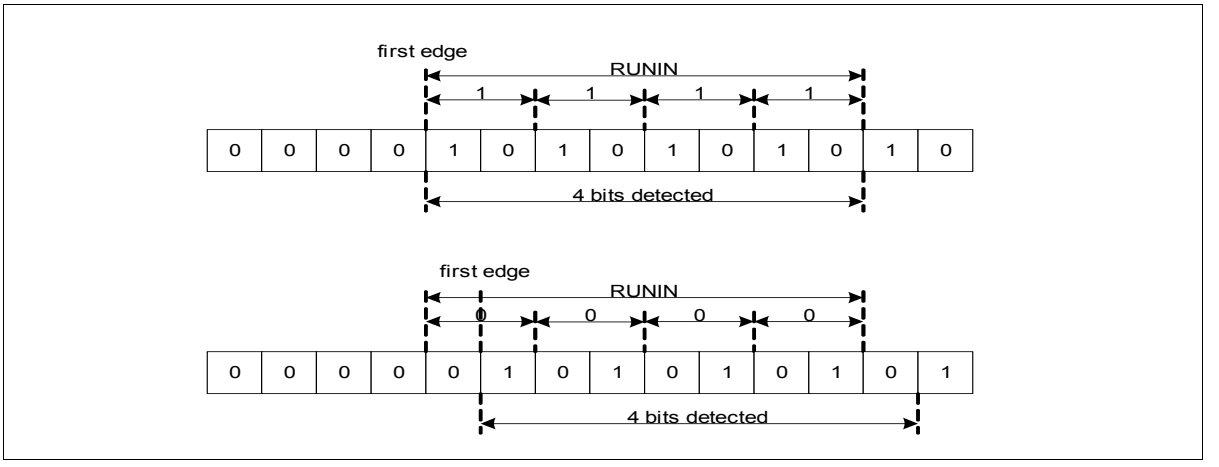

Figure 45 RUNIN generation principle

Number of Required RUNIN Bits:

The number of RUNIN bits specified in SFR RUNLEN must always be 3.5. This setting defines the duration of the internal synchronisation. Because of internal processing delays, the pattern length that must be reserved for RUNIN is longer.

The ideal RUNIN pattern is a series of either 1’s or 0’s. This pattern includes the highest number of edges that can be used for synchronisation. In this case the number of RUNIN bits is 4.

For any other RUNIN pattern, 5.5 bits should be reserved for RUNIN.

TVWIN CV Window Length

The PLL unlocks if the reference signal is lost for more than the time defined in the TVWIN register. During the TSI GAP (See TSI GAP Mode) the PLL and the TVWIN are frozen.

The TVWIN time is the time that DigRX should stay locked without incoming signal edges detected. The time resolution is T/16.

TVWIN is calculated as follows:

$$TVWIN = round((8 + 16 \cdot CV + 8) \cdot 1{,}25)$$

CV is the number of code violations in a block.

This calculation is done by IAF TDA523x Configuration Tool, if the number of CV's is entered.

Dual: ACDR0 and BCDR0: Clock recovery P parameters

ADDR: 0x73 and 0x93		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:6	W	PDSR: Peak Detector slew rate use 11b
5	W	PHDEN(1): Phase detector error (PDE) outer tolerance range use 1b
4	W	PHDEN(0): Phase detector error (PDE) inner tolerance range use 0b
3:2	W	PVAL: P Value use 01b
1:0	W	PSAT: P Value Saturation use 10b

Dual: ACDR1 and BCDR1: Clock recovery I parameters

ADDR: 0x74 and 0x94		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:6	W	CORSAT: Correlator output value (Timing extrapolation unit) use 01b
5:4	W	LFSAT: Loop Filter Saturation use 10b

ADDR: 0x74 and 0x94		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3:2	W	IVAL: I Value use 01b
1:0	W	ISAT: I Value Saturation use 01b

Dual: ACDR2 and BCDR2: Clock recovery RUNIN length

ADDR: 0x75 and 0x95		*Reset Value: 0x00*
Bit	**R/W**	**Description**
1:0	W	RUNLEN: RUNIN length use 01b: 3 1/2 bit

Dual: ATVWIN and BTVWIN: CV Window Length

ADDR: 0x77 and 0x97		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TVWIN: CV Window Length 28h: 40/16 bits FFh: 255/16 bits

2.4.12 Wake Up Generation Unit

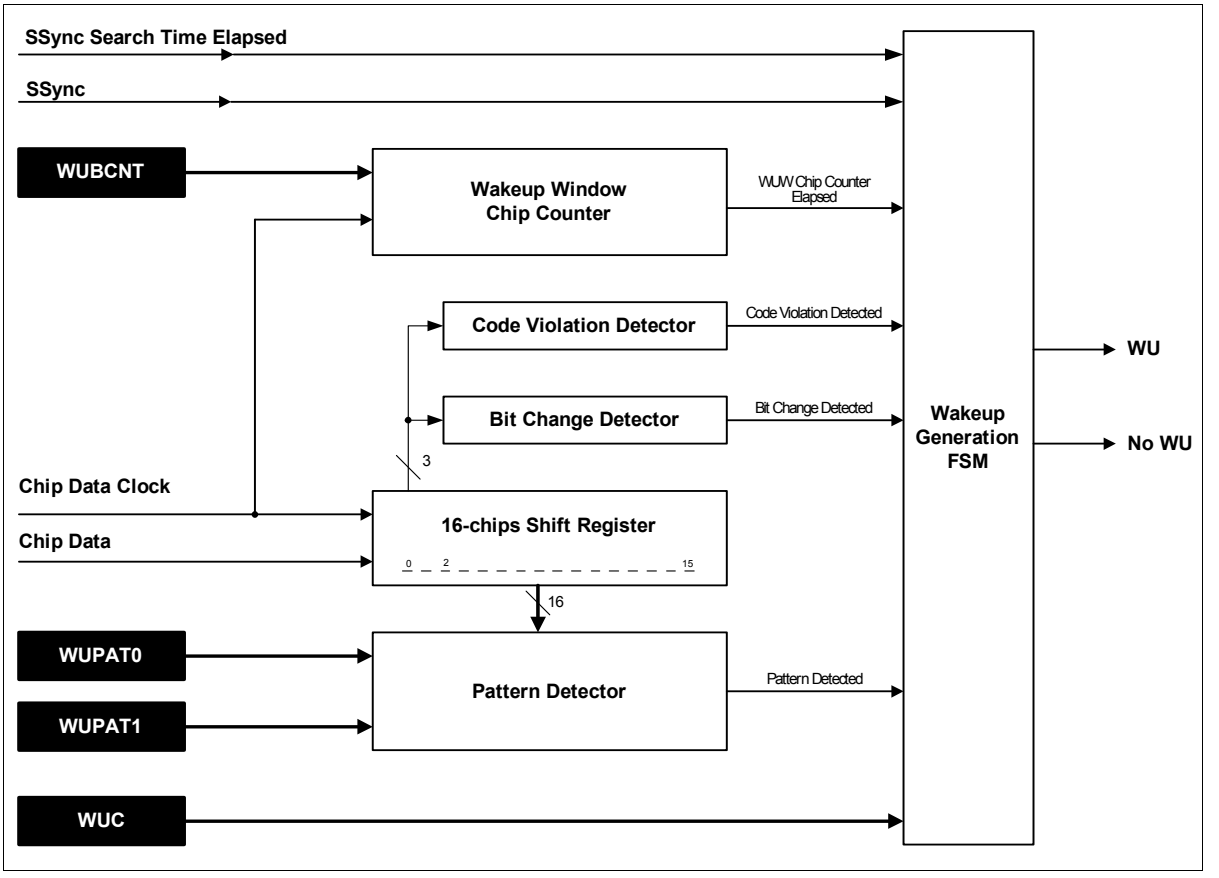

Figure 46 Wake Up Generation Unit

The Wake Up Generation Unit is used only in the Self Polling Mode for the detection of a predefined wake up criterion in the received pattern. All SFRs configuring the Wake Up Generation Unit support the dual configuration capability (Config A and B). The search for wake up criteria is started if symbol synchronization is given within the duration of four symbols (RUNIN); otherwise the wake up search is aborted. During the observation period, the wake up search is aborted immediately if symbol synchronization is lost. If this is not the case, the wake up search will last for the number of chips defined in the register WUBCNT.

The Wake Up Window (WUW) Chip Counter counts the number of received chips and compares this number vs. the number of chips defined in the register WUBCNT.

The Code Violation Detector checks the incoming chip data stream for being manchester coded. A Code Violation is given if three consecutive chips are ’One’ or ’Zero’

The Bit Change Detector checks the incoming Manchester coded bit data stream for changes from 'Zero' to 'One' or 'One' to 'Zero'. This is the case if two consecutive chips are ’One’ or ’Zero’.

The Pattern Detector is searching for a pattern with 16 chips length within the Wake Up Window. The pattern is configurable via the register WUPAT0 and WUPAT1. The selection of 1 out of 4 wake up criteria is done via the WUC register:

The four wake up criteria are in detail:

Pattern Detection

The incoming signal must match a dedicated pattern of up to 8 bits or 16 chips. When the WUW chip counter elapses, the search is stopped. The higher the setting of WUBCNT the longer it is possible to search for the wake up pattern. The minimum for the WUBCNT is 0x11!

The pattern detection is stopped either when WUW elapses, or symbol synchronization is lost.

Equal Bits Detection

Wake up condition is fulfilled if all received bits inside of WUW are either 0 or 1. WUBCNT holds the number of required equal bits. The higher the setting of WUBCNT the lower the number of wrong wake ups.

Equal bits detection is stopped if a wrong bit has been detected, or symbol synchronization is lost.

Random Bits Detection

Wake up condition is fulfilled if there is no code violation inside of WUW. WUBCNT holds the number of required manchester coded bits. The higher the setting of WUBCNT, the lower the number of wrong wake ups.

Random bits detection is stopped if a code violation has been detected, or symbol synchronization is lost.

Valid Data Rate Detection

Wake up condition is fulfilled if symbol synchronization is possible inside of Sync Search Time out, which is by default 7.625 data bits long. WUBCNT is not used.

This is the weakest wake up criterion, and should be avoided.

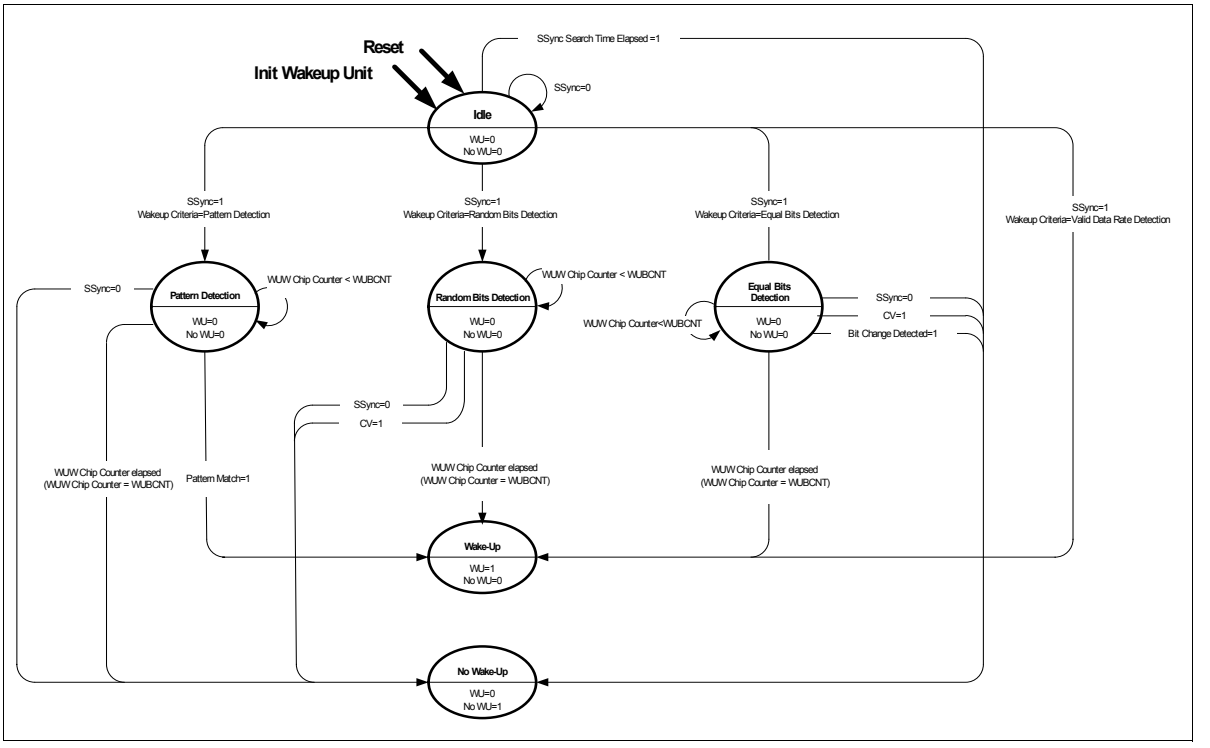

Figure 47 Wake Up Criteria Search

Dual: AWUC and BWUC: Conf.A Wake up Control Register

ADDR: 0x25 and 0x46		*Reset Value:0x00*
Bit	**R/W**	**Description**
1:0	W	WUCRT: Wake Up Criteria 00b: Pattern Detection 01b: Random Bits 10b: Equal Bits 11b: Wake Up on Symbol Sync, Valid Data Rate; The WUBCNT Register has no meaning in this mode.

Dual: AWUPAT0 and BWUPAT0: Conf.A Wake Up Detection Pattern0

ADDR: 0x26 and 0x47		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	WUPAT0: Wake Up Detection Pattern: Bit 7...Bit 0(LSB) (in Chips)

Dual: AWUPAT1 and BWUPAT1: Conf.A Wake Up Detection Pattern1

ADDR: 0x27 and 0x48		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	WUPAT1: Wake Up Detection Pattern: Bit 15(MSB)...Bit 8 (in Chips)

Dual: AWUBCNT & BWUBCNT: Conf.A Wake Up Bit Count Register

ADDR: 0x28 and 0x49		*Reset Value:0x00*
Bit	**R/W**	**Description**
6:0	W	WUBCNT: Wake Up Bit Count Register Counter Register to define the maximum counts of chips for Wake Up detection. Min: 00h = 0 Chips to count In “Random Bits” or “Equal Bits” Mode, this will cause a Wake Up immediately after Symbol Synchronization is found. In “Pattern Detection” Mode, this will cause no Wake Up found. In this Mode, there is a required minimum of 11h= 17 Chips= 8.5 Bits to shift one Pattern through the entire Pattern Detector because comparison can only be started when at least the comparison register is fully filled. Max: 7Fh: 127 Chips to count after Symbol Sync found

2.4.13 Frame Synchronization

The Frame Synchronization Unit (Framer) synchronizes to a specific pattern to identify the exact start of a data frame. This pattern is called TSI (Telegram Start Identifier).

There are different TSI modes selectable via the configuration:

- TSI Mode 16-Bit, supporting a TSI length up to 16 bits or 32 chips
- TSI Mode 8-Bit, supporting two independent TSI pattern of up to 8 bits length
- TSI GAP Mode 8-Bit, supporting the TSI GAP mode
- TSI Mode 8-Bit extended, identical to TSI Mode 8-Bit, but identifies which pattern matches by adding a single bit to the data frame

All SFR configuring the Frame Synchronization Generation Unit are supporting the dual configuration capability (Config A and B). The Framer starts working in Slave Mode after Symbol Sync found and in Self Polling Mode after wake up found and searches for a frame until TSI is found or synchronization is lost. The input of the Framer is a sequence of manchester coded data (Chips). Basically the Framer consists of two identical correlators of 16 chips in length. It allows a Telegram Start Identifier (TSI) to be composed of Manchester coded “Zeros” and “Ones”. The active length of each of the 16 chips correlators is defined independently in the TSILENA and TSILENB registers. The pattern to match is defined as sequence of chips in the TSIPTA0, TSIPTA1, TSIPTB0 and TSIPTB1 registers.

Note that the RUNIN length shown in the figures below is the maximum needed RUNIN with the length of 8 chips set in the register. The needed RUNIN time of the receiver can be shorter by 1-2 chips. It depends on the expected data rate error, duty cycle error, and the starting chip sequence of the protocol.

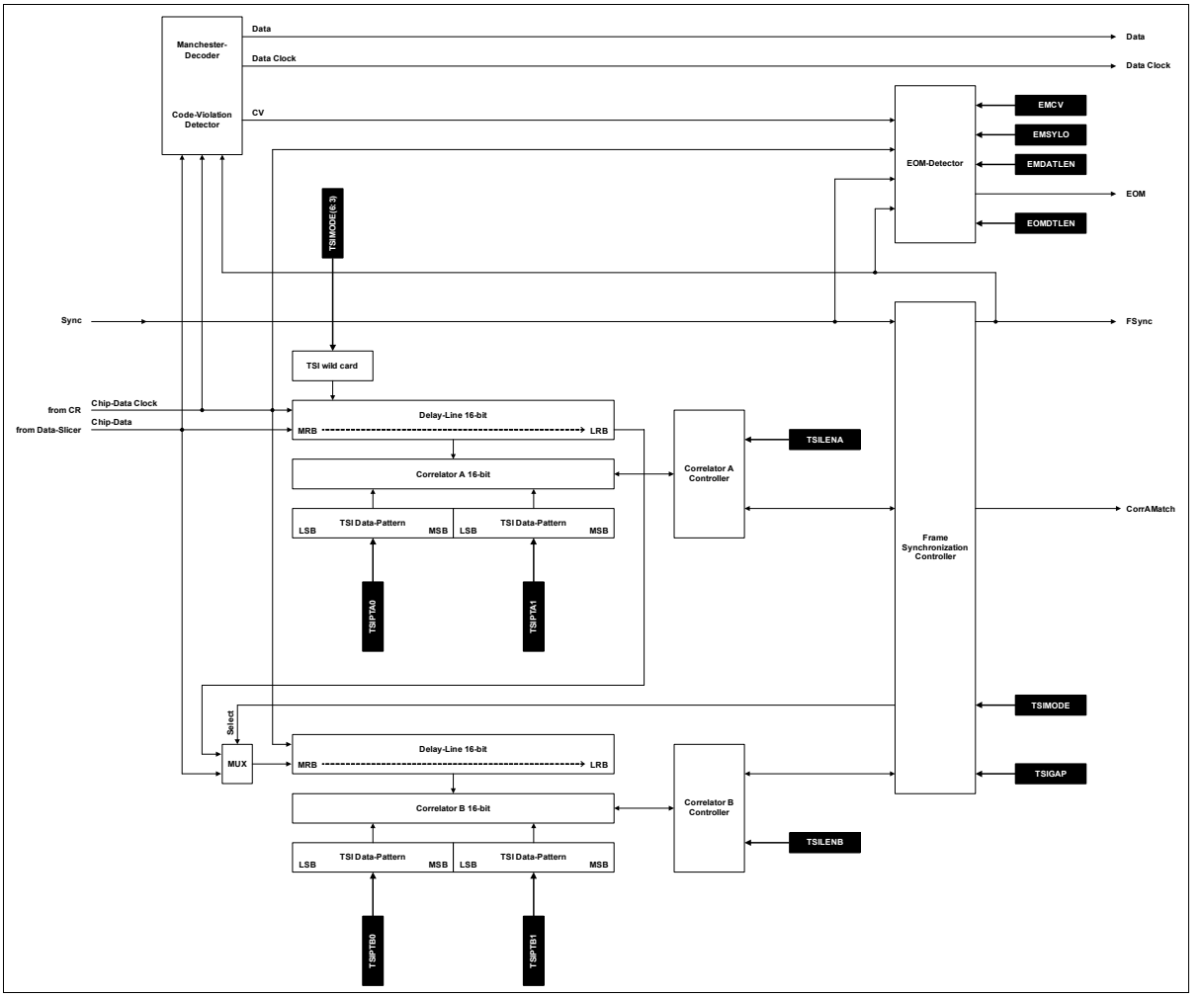

Figure 48 Frame Synchronisation Unit

The two independent correlators can be configured in the TSIMODE register to work in one of the following four modes:

16-Bit Mode: As a single correlator of up to 32 chips

The length of the TSILENA register has to be set to 16d whenever TSILENB is higher than 0.

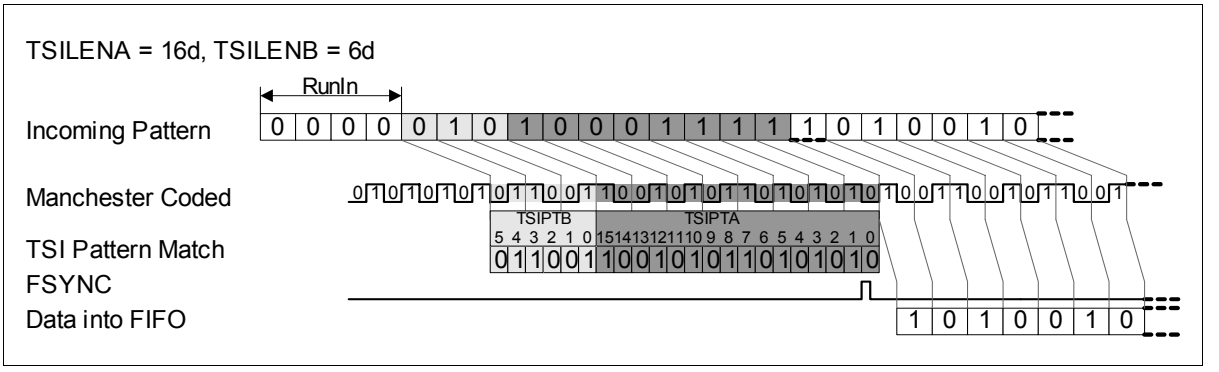

Figure 49 TSI Mode 16-Bit

8-Bit Mode: As two correlators working simultaneously in parallel of up to 16 chips length each

In the following example, TSI Pattern B matched first and generates a FSYNC. The lengths of both TSI Patterns are now independently from each other.

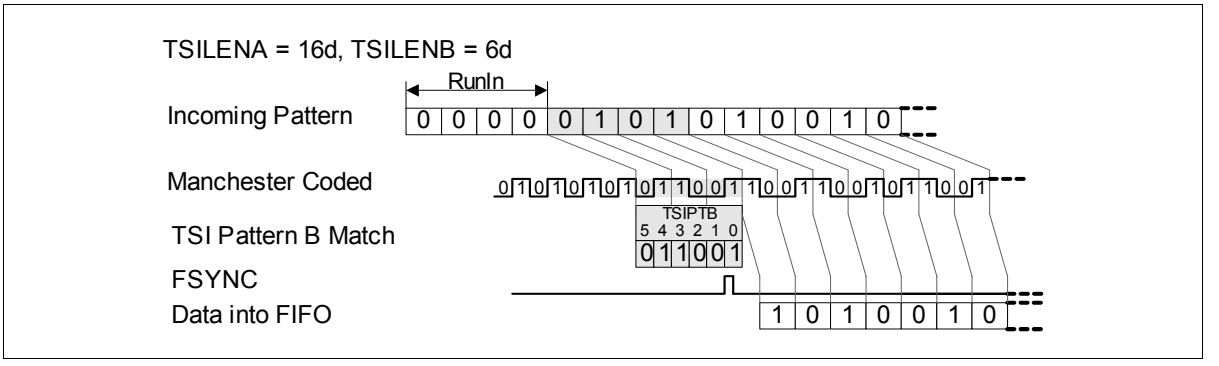

Figure 50 TSI Mode 8-Bit

8-Bit Gap Mode: As two sequentially working correlators of up to 16 chips length each

This mode is only used in combination with the TSI GAP Mode!

This mode is used to define a gap between the two patterns which is preset in the TSIGAP register.To identify exactly the beginning of the Gap it would be helpful on occasion to place the first CV of the Gap into the TSI Pattern A. In this case, the Gap length needed for the TSIGAP register must be shortened and the TVWIN length must be extended (see also **Chapter 2.4.13 Frame Synchronization**).

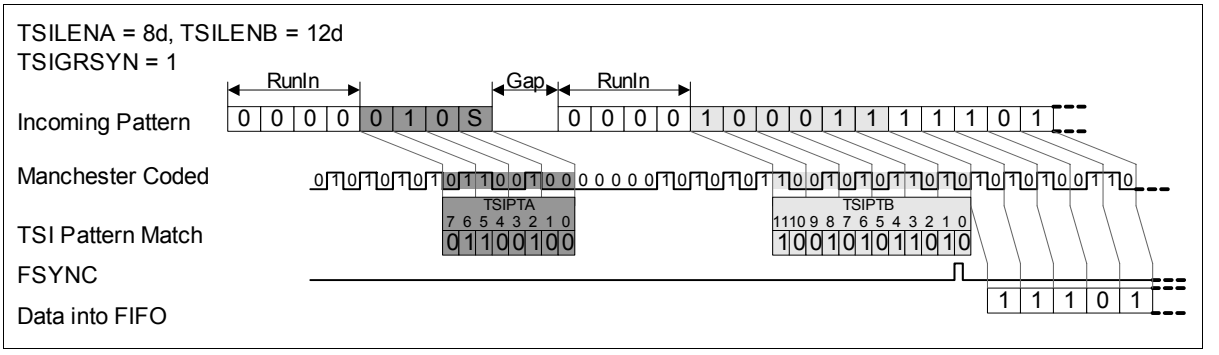

Figure 51 TSI Mode 8-Bit Gap

8-Bit extended Mode: As two correlators working simultaneously in parallel of up to 16 chips length each, with matching information insertion

This bit is inserted at the beginning of the payload. “0” is inserted, when correlator A has matched and “1” when correlator B has matched.

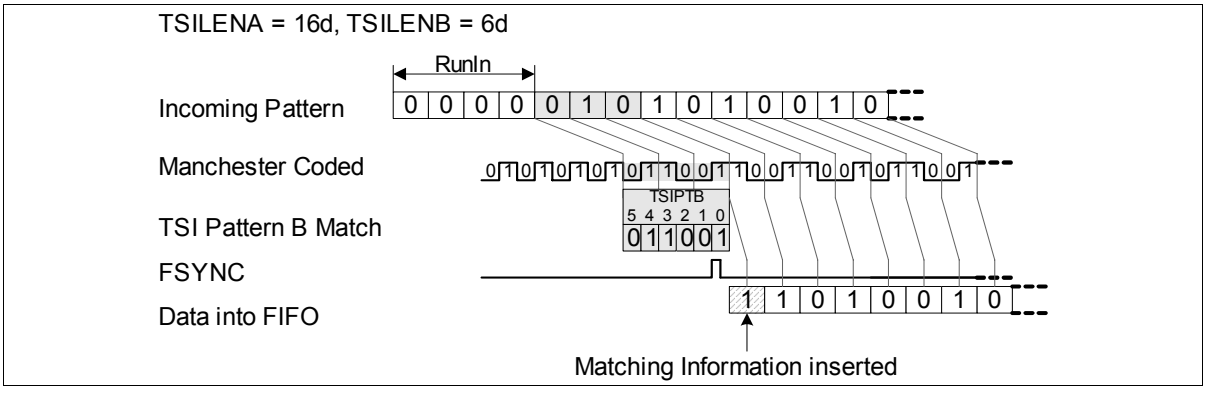

Figure 52 TSI Mode 8Bit extended

Selection of a TSI Pattern:

TSI Patterns must be different to the wake up bit stream and the RUNIN to clearly mark the start of the following data frame. It should be considered that the sychronization has a tolerance of about one bit. In addition, synchronization is related to data chips, and may occur in the middle of a data bit. This all must be tolerated by the data framer.

Ideal TSI patterns have at their end a unique bit combination, which may also contain a number of code violations (CVs).

Some examples of TSI patterns:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

When CVs are used:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 M 1

0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 M

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 M

Note: CVs in a TSI are practical for better differentiation to the real data, especially if repetition of data frames is used for wake up.

End of Message (EOM) Detection

An End Of Message (EOM) detection feature is provided by the EOM detector. Three criteria can be selected to indicate EOM. The first is based on the number of received bits since frame synchronization. The number of expected bits is preset in the EOMDTLEN register. Sending fewer bits as defined in the register will result in no EOM. The EOM counter will be reset after new frame synchronization. The second criterion is the detection of a Manchester Code Violation. The third criterion is the loss of symbol-synchronization. Depending on the TVWIN register, the Sync signal persists for a certain amount of time after the end of the Pattern has been reached. Therefore, more bits could be written into the FIFO than sent. All three EOM criteria can be combined with each other. If one of the selected EOM criteria is fulfilled an EOM signal will be generated.

Dual: ATSIMODE and BTSIMODE: TSI Detection Mode

ADDR: 0x82 and 0xA2			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7	W	TSIGRSYN: TSI Gap Resync Mode (For detailed information, see ATSIGAP/BTSIGAP register description) 0: OFF 1: PLL reset after TSI Gap	
6:3	W	TSIWCA: Wild Cards for Correlator A	

ADDR: 0x82 and 0xA2		*Reset Value: 0x00*
Bit	**R/W**	**Description**
2	W	MANCPAJ: Manchester code phase readjustment 0: disabled - Manchester code polarity is defined by the TSI pattern. 1: enabled - the code phase readjustment will be done with each “1001” or “0110” manchester data change.
1:0	W	TSIDETMOD: TSI Detection Mode 00b: 16-Bit Mode - TSI configuration A AND B valid (sequentially), B is valid if the **ATSILENB**>0 01b: 8-Bit Mode - TSI configurations A OR B (parallel) 10b: 8-Bit Gap Mode- TSI configurations A AND B with Gap (sequentially with Gap between TSIA & TSIB) 11b: 8-Bit extended Mode - TSI configurations A OR B (parallel with matching information), synchronization will be done on full TSI length, dependent on found TSI A or B, 1 or 0 will be send as 1st received bit.

Dual: ATSILENA and BTSILENA: TSI A Length

ADDR: 0x83 and 0xA3		*Reset Value: 0x00*
Bit	**R/W**	**Description**
4:0	W	TSI A Length (in chips): (0x11 up to 0x1F not used) Min: 00h = 0 Bit; works only in 16-Bit Mode: FSYNC will be generated after Symbol Synchronization. In other modes, the smallest possible value to generate a FSYNC will be 01h. Be aware that such small values makes it impossible to find the right phase of the pattern in the data stream and therefore incorrect data and code violations can be generated. Max: 10h = 16 Chips = 8 Bit

Dual: ATSILENB and BTSILENB: TSI B Length

ADDR: 0x84 and 0xA4		*Reset Value: 0x00*
Bit	**R/W**	**Description**
4:0	W	TSI B Length (in chips): (0x11 up to 0x1F not used) Min: 00h =0 Bit (see also ATSILENA) Max: 10h = 16 Chips = 8 Bit

Dual: ATSIPTA0 and BTSIPTA0: TSI Data Reference Low Byte A

ADDR: 0x86 and 0xA6		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTA0: Data Pattern for TSI comparison: Bit 7...Bit 0(LSB) (in chips)

Dual: ATSIPTA1 and BTSIPTA1: TSI Data Reference High Byte A

ADDR: 0x87 and 0xA7		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTA1: Data Pattern for TSI comparison: Bit 15(MSB)...Bit 8 (in chips)

Dual: ATSIPTB0 and BTSIPTB0: TSI Data Reference Low Byte B

ADDR: 0x88 and 0xA8		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTB0: Data Pattern for TSI comparison (in chips)

Dual: ATSIPTB1 and BTSIPTB1: TSI Data Reference High Byte B

ADDR: 0x89 and 0xA9		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTB1: Data Pattern for TSI comparison (in chips)

Dual: AEOMC and BEOMC: EOM Control

ADDR: 0x8A and 0xAA		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3	W	Not used: always set to 0
2	W	EMSYLO: EOM by Sync Loss[1)]
1	W	EMCV: EOM by Code Violation[1)]
0	W	EMDATLEN: EOM by Data Length[1)]

1) The EOM criteria can be combined.

Dual: AEOMDTLEN and BEOMDTLEN: EOM Data Length Limit

ADDR: 0x8B and 0xAB		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	DATLEN: Length of Data Field in Telegram Counting starts after the last TSI Bit Min: 00h = The next bit after TSI found (when EOM criterion is EMDATLEN) will generate EOM Max: FFh

TSI Gap Mode

The TSI GAP Mode is only used if TSI patterns contain a GAP that is not synchronous to the data rate, e.g. if a GAP is 7.7 data bits, or if a GAP is longer than 10 data bits. In all other cases, GAPs should be included in the TSI pattern as code violations.

Because of its complexity in configuration, TSI Gap Mode should be used only in applications as noted above!

For these special protocols, it is possible to lock the actual frequency during a long Code Violation period inside a TSI (TSIGAP must possess a minimum of 8 chips). After the lock period, two different re-synchronization modes are available:

- **Preferred:** phase readjustment only, TSIGRSYN = 0. In this mode, the GAPVAL value is used to correct the phase after the GAP phase. Overall GAP time can be defined in T/16 steps. The 5 MSB bits define the real GAP time and the 3 LSB bits (GAPVAL) the DCO phase correction value.

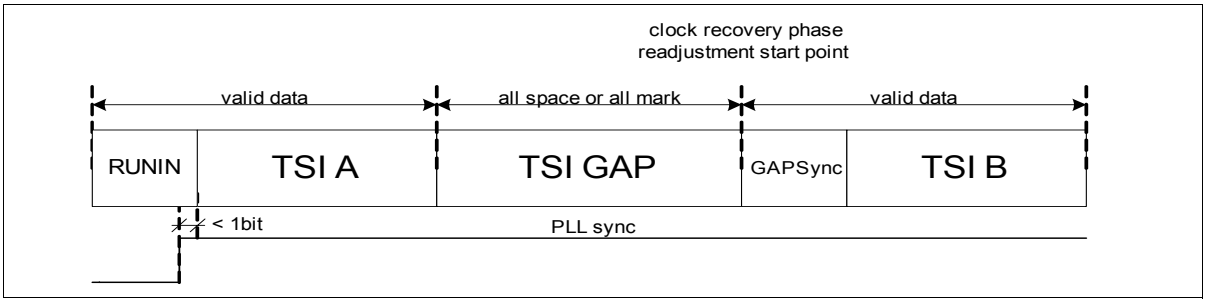

Figure 53 Clock Recovery GAP Re-synchronization mode 0

- Frequency readjustment (in this case, PLL starts from the beginning), TSIGRSYN = 1. In this mode the T/2 GAP resolution can be set in the 5 MSB TSIGAP register bits. GAPVAL (3 LSB register bits) value is not used.

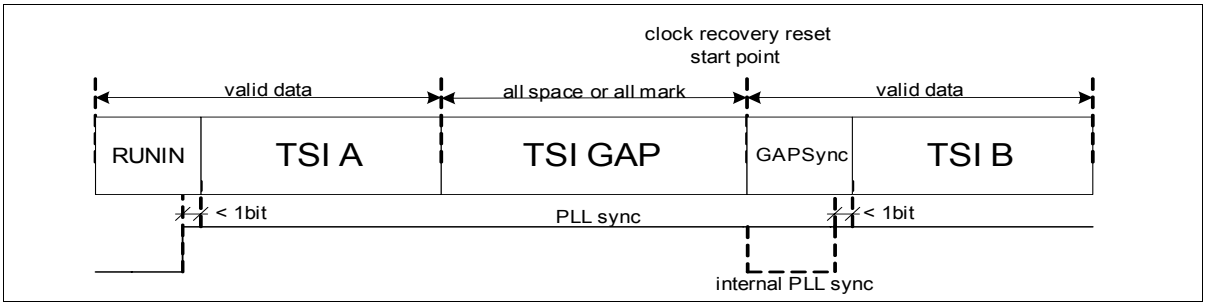

Figure 54 Clock Recovery GAP Re-synchronization Mode 1

When the time TSI GAP in the start sequence of the transmitted telegram has elapsed, the receiver needs a certain time (GAPSync = 5...6 chips) to readjust the PLL settings.

Behavior of the system at the starting position of the TSI B:

The starting position (TSI B start) for the TSI B comparison is independent from the RUNIN settings (CDR2 register) and the Re-synchronization mode (TSIMODE register):

$$TSIBstart[chips] = TSIGAP[chips] + 6...8$$

The incoming chips at TSI B start and the following incoming chips are compared with the contents of the register TSI B. Please notice that the receiver's PLL runs at the data rate determined before the gap. Therefore, the receiver calculates the gap based on this data rate.

Behavior of the system at the ending position of TSI B:

The system checks for the TSI B to match within a limited time. If there is no match within this time, then the receiver starts again to search for the TSI A pattern at the following incoming chips:

$$TSIBstop[chips] = TSIGAP[chips] + TSILENB[chips] + 11$$

For a successful TSI B pattern match, the defined TSI B pattern must be between "Start of TSIB" and "Stop of TSI B". In the example below, the earliest possible start position would be the 18^{th} chip and the latest possible start position would be the 22^{nd} chip.

Please note that after a gap the internal TSI comparison register is cleared (all chips set to '0'). In this case, a TSI B criteria of "0000" would always match at the beginning. To avoid such an unwanted matching, set the highest TSI B match chip to '1'.

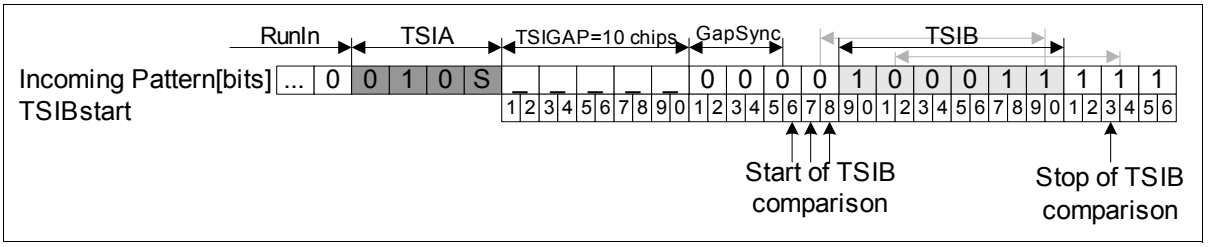

Figure 55 TSIGap TSIB Timing

The next figure shows the TVWIN and TSIGAP dependency.

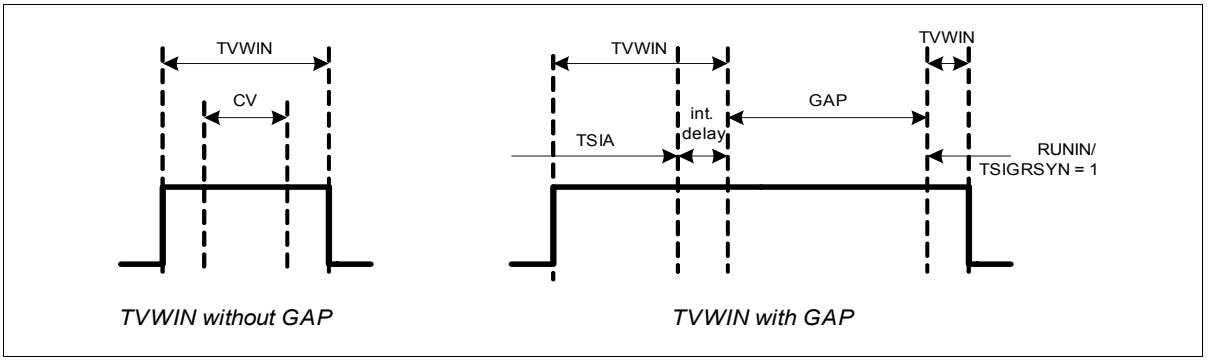

Figure 56 TVWIN and TSIGAP dependency example

TVWIN calculation for pattern without GAP time:

$$TVWIN = round((8 + 16 \cdot CV + 8) \cdot 1{,}25)$$

The entire TVWIN time is made up of the CV[1)] number itself, the half bit before CV and the half bit after the CV. To reach all frequency and duty cycle errors, 25% of the overall sum must be added.

TVWIN calculation with GAP time:

1) CV...number of bits containing manchester code violations

$$TVWIN = round(max\{((8 + 16 \cdot CV + 8) \cdot 1{,}25), (8 + 16 \cdot TSIA_{CV} + 16 \cdot 1 + 8) \cdot 1{,}25\})$$

Dual: ATSIMODE and BTSIMODE: TSI Detection Mode

ADDR: 0x82 and 0xA2		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7	W	TSIGRSYN: TSI Gap Resync Mode (For detailed information, see ATSIGAP/BTSIGAP register description) 0: OFF 1: PLL reset after TSI Gap
2	W	MANCPAJ: Manchester code phase readjustment 0: disabled - Manchester code polarity is defined by the TSI pattern. Use as default, if TSI 8bit GAP Mode is not used 1: enabled - the code phase readjustment will be done with each “1001” or “0110” Manchester data change. Use for TSI 8bit GAP Mode

Dual: ATSIGAP and BTSIGAP: TSI GAP

ADDR: 0x85 and 0xA5		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:3	W	TSIGAP: TSI Gap (T/2 bit resolution) 1Fh: 15 1/2 bit gap 00h: 0 bit gap TSIGAP is used to lock the PLL after TSI A is found, if the TSI detection mode 10b is selected.
2:0	W	GAPVAL: TSI Gap (T/16 bit resolution) 111b: 7/16 bit gap 000b: 0 bit gap GAPVAL is used to correct the DCO phase after TSIGAP time, if the TSIMODE.TSIGRSYN is disabled

Pre-Slicer Setting:

During the GAP time there is high sensitivity to jammer, especially if the jammer is close to the bit rate or 1/2 bit rate.

The Pre-Slicer helps to suppress jammer during the GAP time. Therefore, in TSI GAP mode, and in TSI GAP mode only should the Pre-Slicer be enabled using the default settings.

Dual: APSLC and BPSLC: Pre Slicer Control

ADDR: 0xB4 and 0xB5		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7	W	PSLCDA: Pre-Slicer disable 0: pre-silcer enable...use only for TSI GAP Mode 1: pre-slicer disable (default)
6:5	W	PSLCHYS: Pre-Slicer hysteresis use 01b
4:0	W	PSLCTHR: Pre-Slicer disable threshold use 10010 (0x12)

2.4.14 Message-ID Scanning

Hardware Description

This unit is used to define an ID or special combination of bits in the data stream, which identifies the pattern. All SFRs configuring the Message ID Scanning Unit feature the dual configuration capability. Furthermore, it is available in the Slave and Self Polling Mode. The MID Unit can be mainly configured in 2 Modes: 4-Byte and 2-Byte organized Message ID. For each configuration there are 20 8-bit registers designed for ID storage (MID0...MID19). The MIDC0 and MIDC1 are used to configure the MID Unit: Enabling of the MID scanning, setting of the ID storage organization, the starting position of the comparison and number of Bytes to scan.

When the Message ID Scanning Unit is activated by the MIDC1, the incoming data stream is compared bit-wise serially with all stored IDs. If the Scan End Position is reached and all received data have matched the observed part of at least one MID, the Message ID Scanning Unit indicates successful MID scanning to the Master FSM, which generates a MID interrupt.

Please note that the default register value of the MID Registers is set to 0x00. All MID registers must be set to a pattern value to avoid matching to default value 0x00.

If the MID Unit finishes ID matching without success, the data receiving is stopped and the FSM waits again for a Frame Start criterion. The received bits are still stored in the FIFO. For details see also **Chapter 2.4.15 Data FIFO**.

4-Byte Organized Message ID

In this mode four bytes are merged to define an ID Pattern. This does not mean that the ID must be exactly four Bytes long. The number of bytes used there is defined in the MIDC1 register. Up to 5 ID Patterns are available.

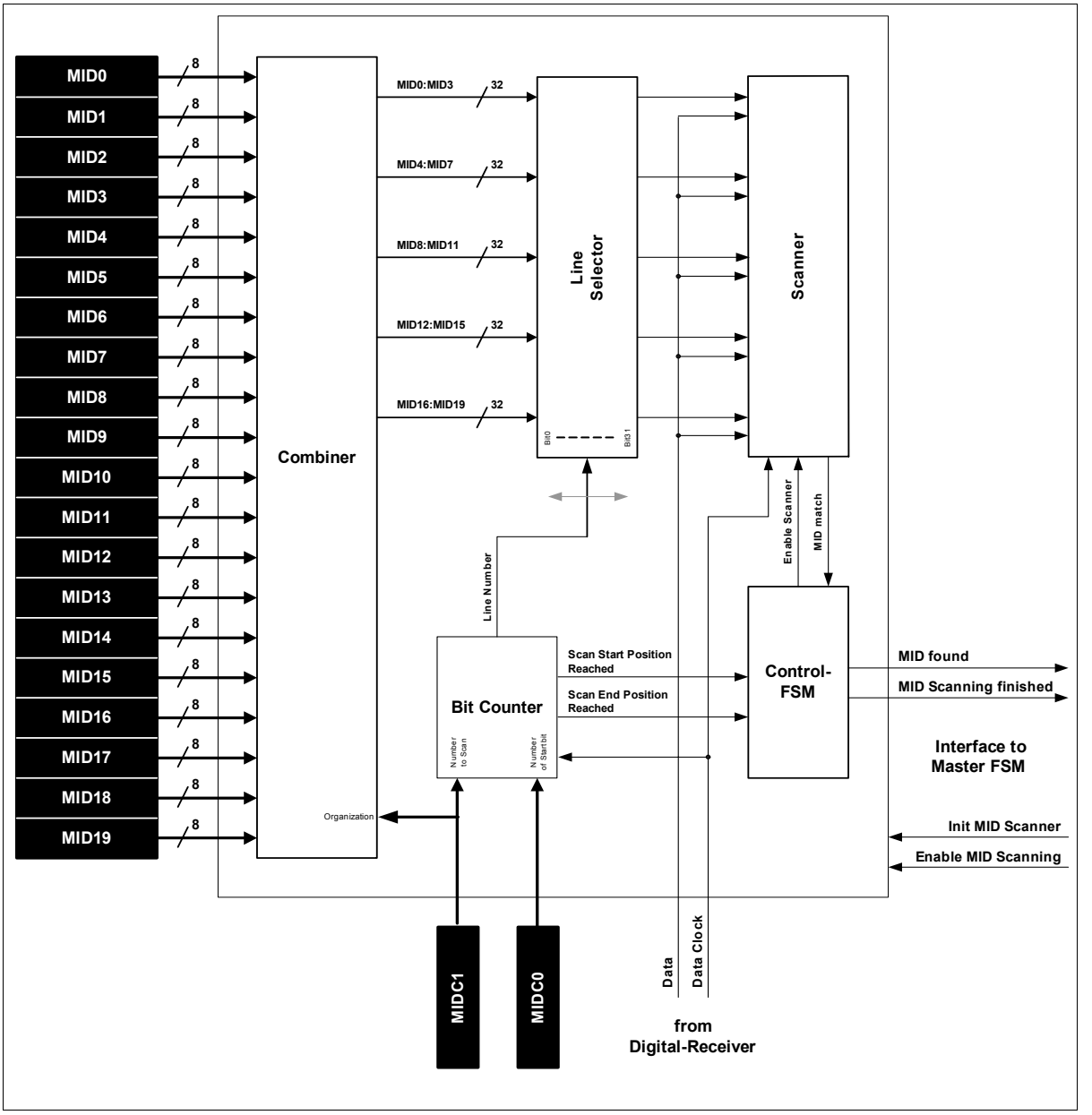

Figure 57 4-Byte Message-ID Scanning

4-Byte Organized Message ID

In this mode two bytes are merged to define an ID Pattern. Up to 10 patterns are possible.

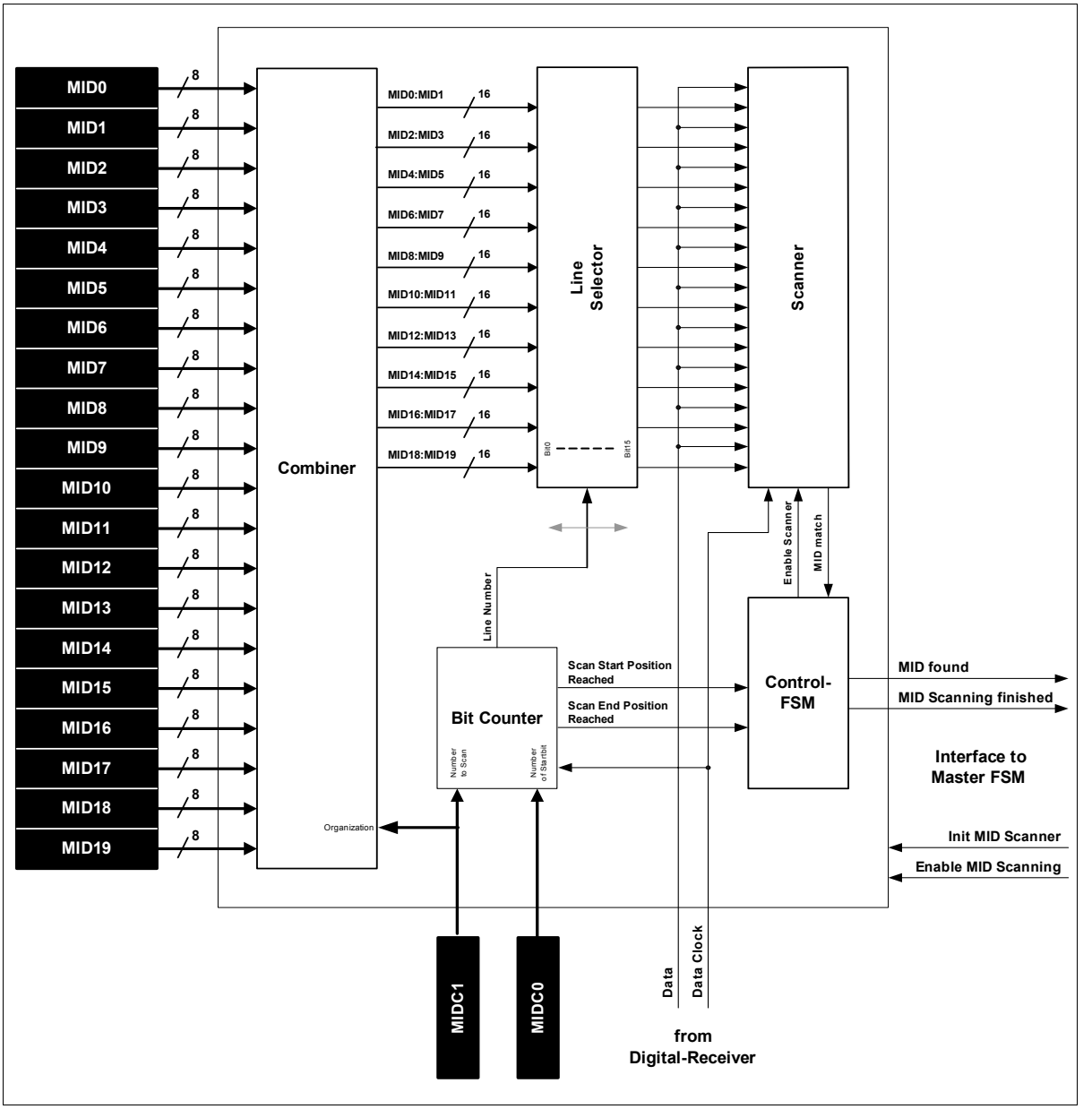

Figure 58 2-Bytes Message ID Scanning

ID Position Configuration

It is possible to choose which part of the incoming data stream is compared against the stored MIDs. The register MIDC0 contains the Scan Start Position (Bit 0 to Bit 127). If the Bit Counter detects the Scan Start Position the Control FSM enables the Scanner. The register MIDC1 contains the number of bytes to scan (Byte 0 to Byte 3). During the observation period, the Message ID Scanning is aborted immediately by the Master FSM if symbol synchronization is lost or an EOM (End Of Message) is detected.

Example:

Start Selection: 0010001b

Number to scan: 00b, 01b, 10b, 11b

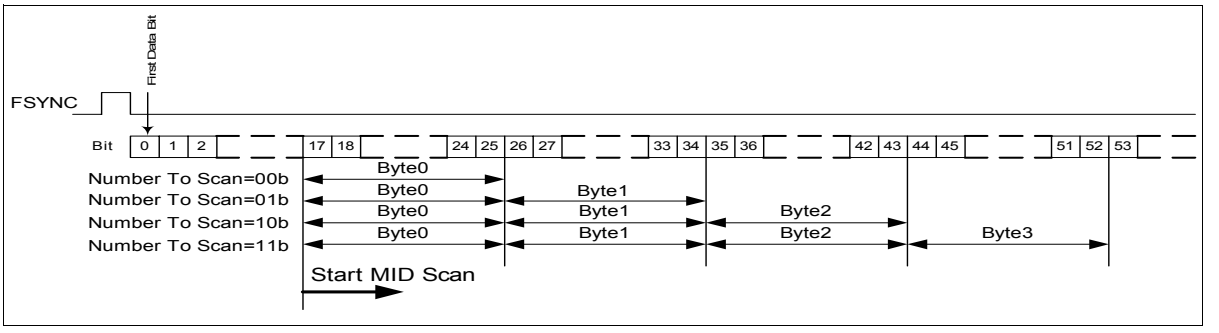

Figure 59 ID Scanning

The starting position in this case is Bit 17. Depending on the number to scan, the corresponding number of bytes is compared with the stored MIDs.

Dual: AMID0-AMID19 and BMID0-BMID19: Conf.A Message ID Register0

ADDR: 0x29-0x3C and 0x4A-0x5D		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	MID0: Message ID Register

Dual: AMIDC0 and BMIDC0: Conf.A Message ID Control Register0

ADDR: 0x3D and 0x5E		*Reset Value:0x00*
Bit	**R/W**	**Description**
6:0	W	SP: MID scan start position Min: 00h = Comparison starts one bit after FSYNC Max: 7F = Comparison starts 128 bits after FSYNC

Dual: AMIDC1 and BMIDC1: Conf.A Message ID Control Register1

ADDR: 0x3E and 0x5F		*Reset Value:0x00*
Bit	**R/W**	**Description**
3	W	MIDSEN: Enable ID screening 0: Disabled 1: Enabled
2	W	MIDBO: Message ID organization 0: 2-Byte 1: 4-Byte
1:0	W	MIDNTS: Message ID Number of Bytes To Scan Min: 00b = 1 Byte to scan Max for 2-Byte organization: 01b: 2 bytes to scan. Higher values than 01b will be mapped automatically to 2 bytes to scan Max for 4-Byte organization: 11b= 4 bytes to scan

2.4.15 Data FIFO

The Data FIFO is the storage for the received data frames. It is written during data reception. The host microcontroller is able to start reading via SPI right after frame sync (interrupt). The FIFO can store up to 128 received data bits. If the expected data transmission contains more bits (note that in TSI 8-Bit Mode Extended the first bit is used to indicate which of the two TSI pattern has matched), reading must start after frame sync to prevent an overrun.

Architecture:

The 128-bit data FIFO is based on a bit addressable 2-port memory architecture.

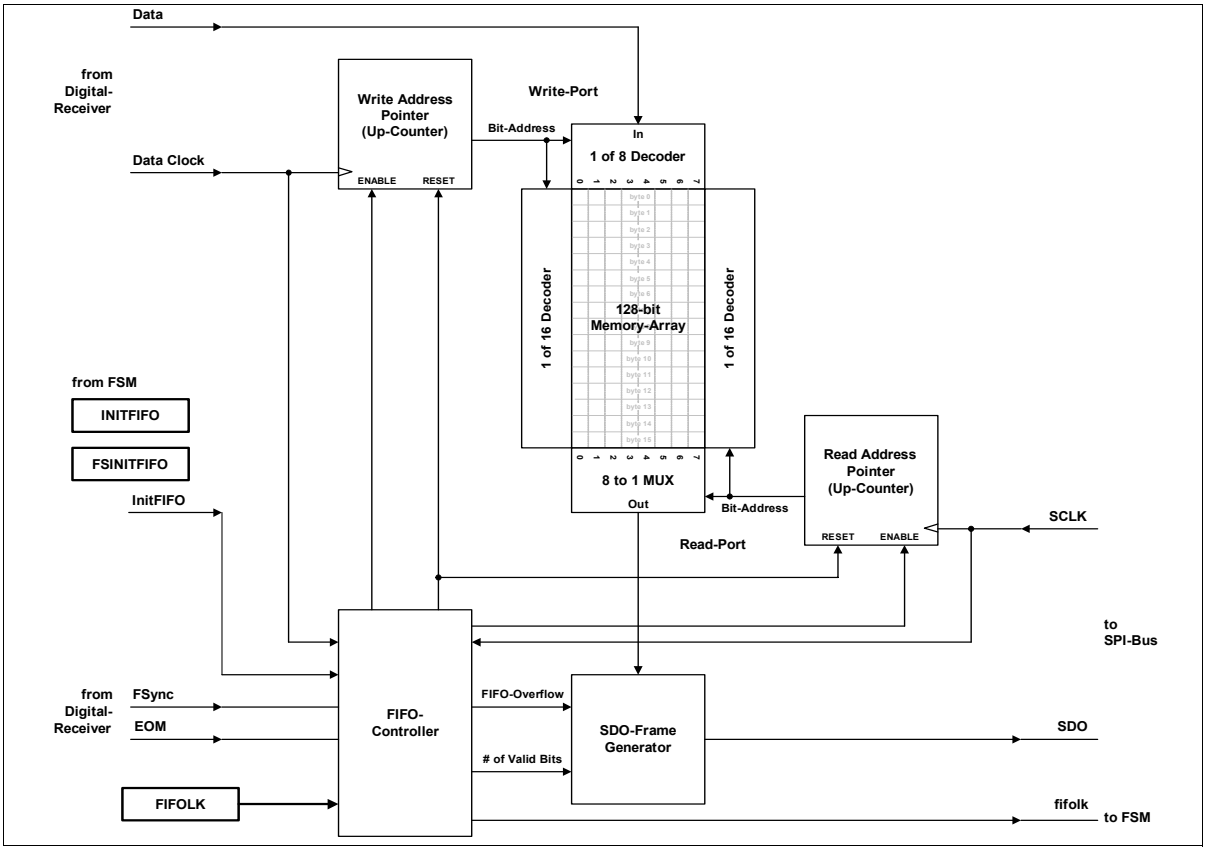

Figure 60 Data FIFO

The write port is controlled by the Digital Receiver using the Write Address Pointer. Writing data into the FIFO starts with the detection of a TSI. The Write Address Pointer is incremented with each data clock signal generated by the Digital Receiver. The read port is controlled by the SPI controller using the Read Address Pointer. Each bit read from the SPI controller increments the Read Address Pointer. The Read and Write

Address Pointers jump from their maximum value (127_d) to address zero. Writing to the FIFO stops at EOM or after Sync loss.

FIFO Lock Behavior

The FIFO possesses a lock mechanism that is enabled via the SFR control bit FIFOLK in CMC0 register. If this mechanism is enabled, the FIFO will enter a FIFO Lock state at the detection of the EOM criterion. During the time that the FIFO is locked, it is not possible for additional data to be received in the Run Mode Self Polling. This means that it is only possible to detect another wake up in the Self Polling Mode, but no more data in the Run Mode Self Polling. This will guarantee that only the first complete data packet is stored in the FIFO. The FIFO will remain locked unless one of three conditions occurs:

1.) The remaining contents of the FIFO are completely read out via the SPI

2.) The SFR control bit FIFOLK is cleared.

3.) INITFIFO at Cycle Start is set in the CMC0 register and

a) FSM is switched to Run Mode Slave or

b) FSM switches from Self Polling Mode to Run Mode Self Polling

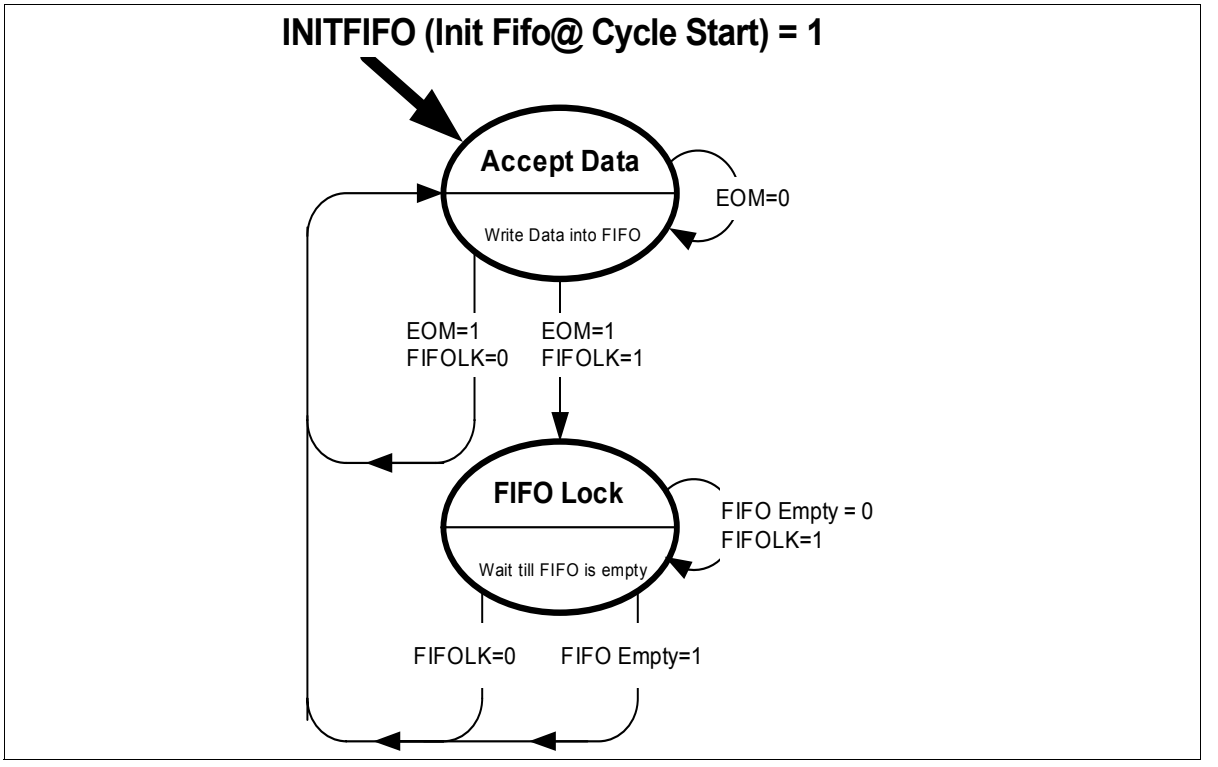

Figure 61 FIFO Lock Behavior

Known Problem on using FIFO Lock in combination with EOM Interrupt in Run Mode Slave:

Indifferent to the described behavior in Run Mode Slave, the NINT sticks low for low active Interrupt or high for high active interrupt, after an EOM Interrupt, if FIFO Lock is enabled. NINT is reset after reading the FIFO. See also **Chapter 2.4.17 Interrupt Generation Unit**.

FIFO Status Word

The FIFO Status Word is mixed to FIFO SPI transmission, and shows if there was an overflow, and how many valid data bits are transmitted. The number of valid FIFO bits is indicated at bit positions S0 to S5. S6 of the Status Word is always undefined.

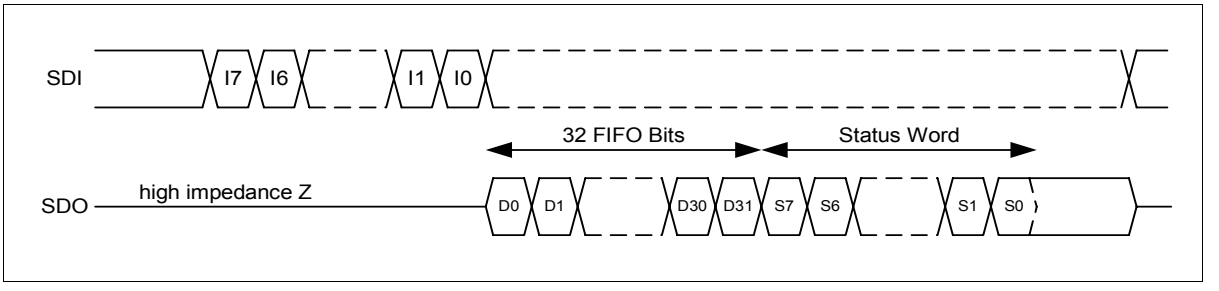

Figure 62 SPI Data FIFO Read

If the Write Address Pointer outruns the Read Address Pointer, an overflow is indicated in the FIFO Overflow Status bit in the FIFO Read Status Word at position S7. All 32 FIFO bits and the bits S5 to S0 of the Status Word are undefined while the Overflow Status bit is set.

If a TSI is detected after an overflow, the FIFO Overflow Status bit is cleared and the entire data FIFO is initialized.

Initialization

Additionally there are two possibilities to initialize the Data FIFO.

- If the INITFIFO bit is set in the CMC0 register(“Init FIFO at Cycle Start”) the entire Data FIFO is always initialized

  a.) after switching to Run Mode Slave or

  b.) switching from Self Polling Mode to Run Mode Self Polling.
- If the FSINITFIFO-bit in CMC1 register is set, the entire Data FIFO is initialized when a TSI is detected and the Data FIFO is not locked (“Init FIFO at Frame Start”).

CMC0: Chip Mode Control Register 0

ADDR: 0x02		*Reset Value: 0x40*
Bit	**R/W**	**Description**
7	W	INITFIFO: Init FIFO at Cycle Start This Initialization of the FIFO can be configured in both Slave Mode and Self Polling Mode. In Slave Mode, this occurs at the beginning of the Slave Run Mode. In Self Polling Mode, the initialization is done after Wake up found (switching from Self Polling Mode to Run Mode Self Polling). 0: No Init 1: Init FIFO
4	W	FIFOLK: Lock Data FIFO at EOM 0: FIFO lock is disabled 1: FIFO lock is enabled at EOM (see also Chapter FIFO)

CMC1: Chip Mode Control Register 1

ADDR: 0x03		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3	W	FSINITFIFO: Init FIFO at Frame Start 0: No Init 1: Init

2.4.16 Transparent Mode

In addition to the FIFO functionality, the TDA5230 offers the received data in a Transparent Mode. In this mode, the Manchester decoded data is available at an external pin.

This is the same data that is written into the FIFO. This means that data is only available after a frame synchronization. Wake up pattern, RUNIN and TSI are not visible. If the FIFO is locked, no data will be written in the Tranparent Mode.

Two pins can be configured to act as the RX data output (CLKOUT/RXD or alternatively RX-RUN/RXD). The pin NINT/NSTR acts as a data strobe signal. The strobe signal is active high and has a delay of TBIT/16 relative to the data bit and a duration of TBIT/16. Configuration of the Transparent Mode is done in the CMC1 register.

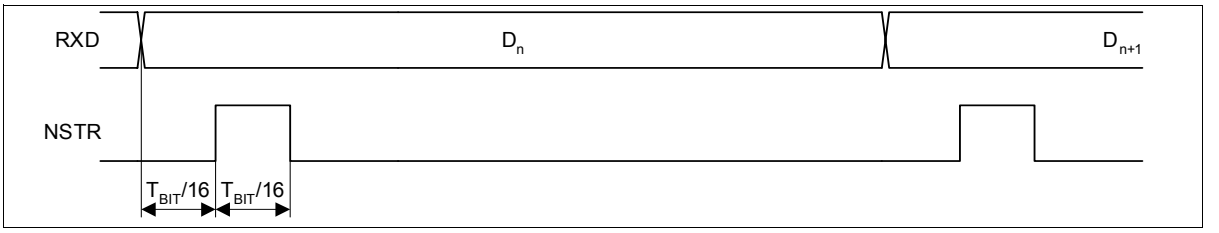

Figure 63 Transparent Mode

CMC1: Chip Mode Control Register 1

ADDR: 0x03		*Reset Value: 0x00*
Bit	**R/W**	**Description**
2	W	CLKRXDSEL: CLKOUT/RXD pin Function 0: CLKOUT at Pin CLKOUT/RXD 1: RX-Data out at pin CLKOUT/RXD
1	W	NINTNSTRSEL: NINT/NSTR pin Function 0: Interrupt out at pin NINT/NSTR 1: RX-Data Strobe out NINT/NSTR
0	W	RXRUNRXDSEL: RX-RUN/RXD pin Function 0: RX-Run Signal out at pin RX-RUN/RXD 1: RX-Data out at Pin RX-RUN/RXD

2.4.17 Interrupt Generation Unit

The Interrupt Generation Unit receives all possible interrupts and sets the NINT signal based on the configuration of the Interrupt Mask register (IM). The Interrupt Status register is set from the Interrupt Generation Unit, depending on which interrupt occurred. The polarity of the interrupt that is routed to the NINT/NSTR Pin is defined in the CMC1 register. Please note that during power up and brown out reset, the polarity of the NINT/NSTR Pin is always as described in **Chapter 2.4.2 Chip Reset**.

A Reset Event has the highest priority. It sets all bits in the Status register to “1” and sets the Interrupt Pin to “0”. The first interrupt after the Reset Event will clear the Status register and will set the Interrupt Pin to “1”, even if this interrupt is masked.

A wake up interrupt clears the FsyncA, FsyncB and the complementary wake up Flag. A Fsync Interrupt clears the EOMA, EOMB, MIDA, MIDB and the complementary Fsync Flag.

The Interrupt Status register is always cleared after it is read via SPI.

It is not possible to disable the Power On Reset Indicator Interrupt using the Interrupt Mask register.

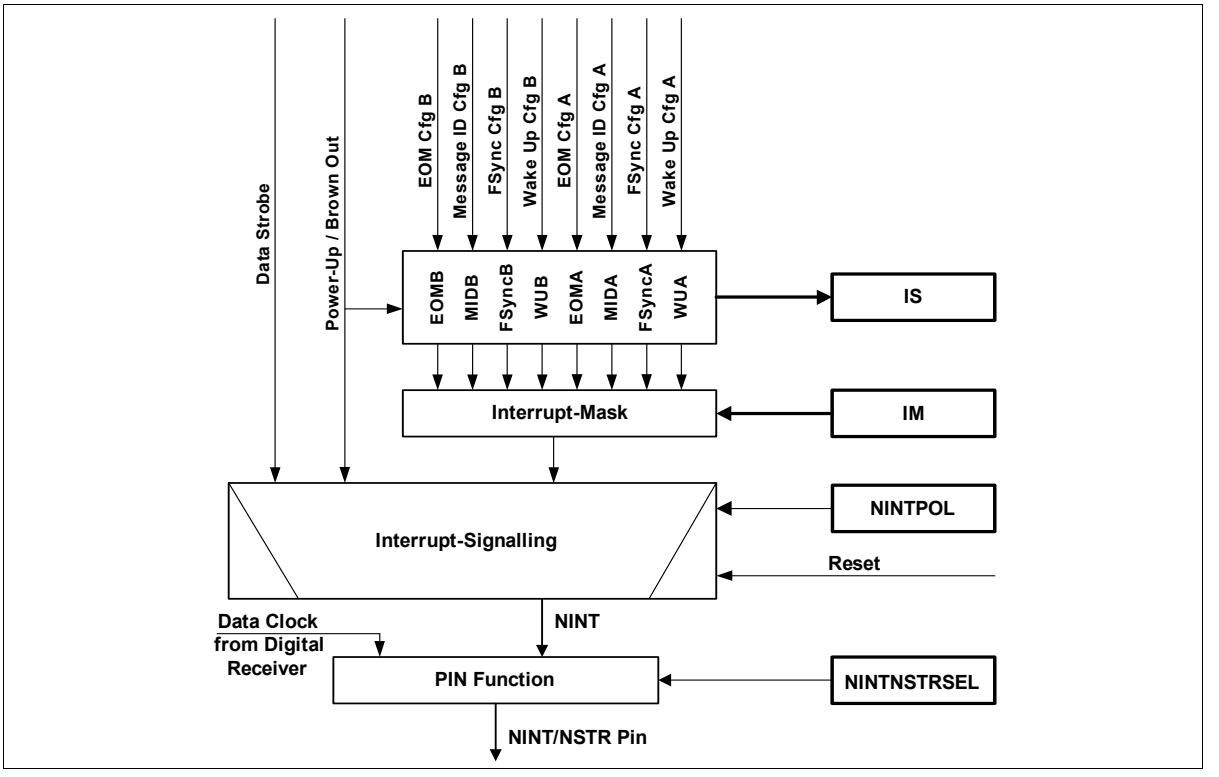

Figure 64 Interrupt Generation Unit

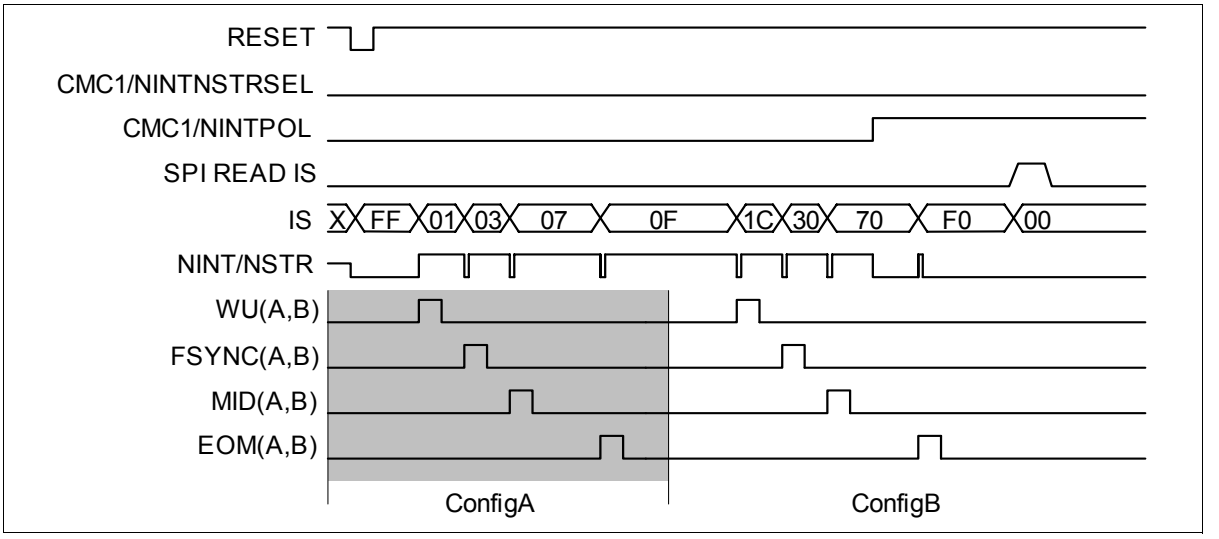

Figure 65 Interrupt Generation Waveform

Known Problem on using EOM Interrupt in combination with FIFO Lock in Run Mode Slave:

In difference to the described behavior in Run Mode Slave NINT sticks low for low active Interrupt or high for high active interrupt, after an EOM Interrupt, if FIFO Lock is enabled. NINT is reset after reading the FIFO. See also **Chapter 2.4.15 Data FIFO**.

CMC1: Chip Mode Control Register 1

ADDR: 0x03			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
5	W	NINTPOL: Invert NINT Polarity 0: The Interrupt is active low 1: The polarity of the Interrupt is inverted (active high)	
1	W	NINTNSTRSEL: NINT/NSTR Pin Function 0: Interrupt out at pin NINT/NSTR 1: RX-Data Strobe out NINT/NSTR	

IS: Interrupt Status Register

ADDR: 0x04		Reset Value: 0xFF
Bit	**R/W**	**Description**
7	C	EOMB: End of Message Config.B Reset event sets all bits to 1
6	C	MIDFB: Message ID Found Config.B Reset event sets all bits to 1
5	C	FSYNCB: Frame Sync Config.B Reset event sets all bits to 1
4	C	WUCFB: Wake Up Criteria Found Config.B Reset event sets all bits to 1
3	C	EOMA: End of Message Config.A Reset event sets all bits to 1
2	C	MIDFA: Message ID Found Config.A Reset event sets all bits to 1
1	C	FSYNCA: Frame Sync Config.A Reset event sets all bits to 1
0	C	WUCFA: Wake Up Criteria Found Config.A Reset event sets all bits to 1

IM: Interrupt Mask Register

ADDR: 0x05		Reset Value: 0x00
Bit	**R/W**	**Description**
7	W	IMEOMB: Mask End of Message Config.B 0: No Mask(active) 1: Mask(inactive)
6	W	IMMIDFB: Mask Message ID Found Config.B 0: No Mask(active) 1: Mask(inactive)
5	W	IMFSYNCB: Mask Frame Sync Config.B 0: No Mask(active) 1: Mask(inactive)
4	W	IMWUCFB: Mask Wake Up Criteria Found Config.B 0: No Mask(active) 1: Mask(inactive)

ADDR: 0x05		Reset Value: 0x00
Bit	**R/W**	**Description**
3	W	IMEOMA: Mask End of Message Config.A 0: No Mask(active) 1: Mask(inactive)
2	W	IMMIDFA: Mask Message ID Found Config.A 0: No Mask(active) 1: Mask(inactive)
1	W	IMFSYNCA: Mask Frame Sync Config.A 0: No Mask(active) 1: Mask(inactive)
0	W	IMWUCFA: Mask Wake Up Criteria Found Config.A 0: No Mask(active) 1: Mask(inactive)

2.4.18 SPI Interface

General Information

- NCS: Select input, active low
- SCK: Clock input. Data bits on SDI are read at rising SCK edges and written out on SDO at falling SCK edges.
- SDI: Data input
- SDO: Data output

Level definition:

logic 0 = low voltage level

logic 1 = high voltage level

Note: It is possible to send multiple frames while the device is selected. It is also possible to change the access mode while the device is selected by sending a different instruction.

Note: In all bus transfers MSB is sent first, except the received data read out from the FIFO. There the bit order is given as first bit that is received is also the first bit that is transferred via the bus.

Read Register

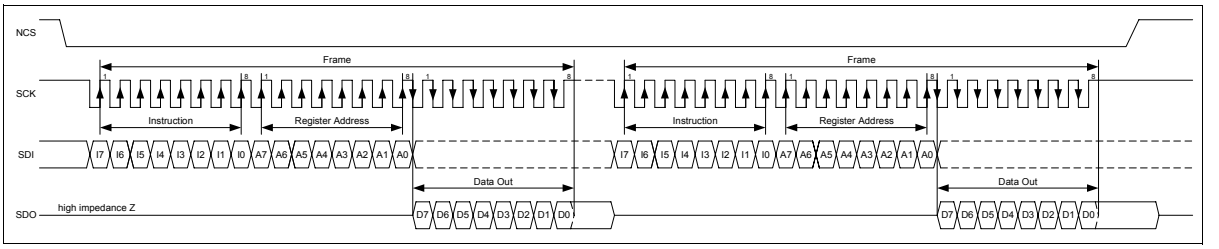

Figure 66 Read Register

To read from the device, the chip must be selected first. Therefore, the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The data byte at this address is then shifted out on SDO. After completing the read operation the master sets the NCS line to high.

Write Register

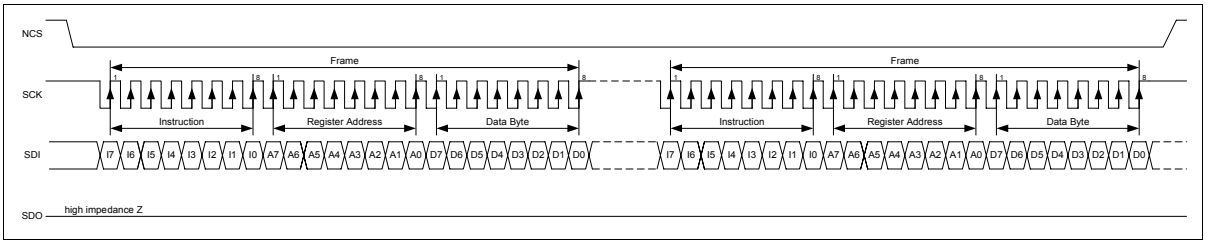

Figure 67 Write Register

To write to the device, the chip must be selected first. Therefore the master must set the NCS line to low. After this, the instruction byte and the address byte are shifted in on SDI and stored in the internal instruction and address register. The following data byte is then stored at this address.

After completing the write operation, the master sets the NCS line to high.

Use of the SPI Trace Registers:

The received address byte is stored into the register SPIAT and the received data byte is stored into the register SPIDT. These two trace registers are readable. Therefore, an external controller is able to check the correct address and data transmission by reading out these two registers after each write instruction. The trace registers are updated at every write instruction, so only the last transmission can be checked by a read out of these two registers.

SPIAT: SPI Address Tracer

ADDR: 0x00		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	R	Address Tracer Register

SPIDT: SPI Data Tracer

ADDR: 0x01		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	R	Data Tracer Register

Read FIFO

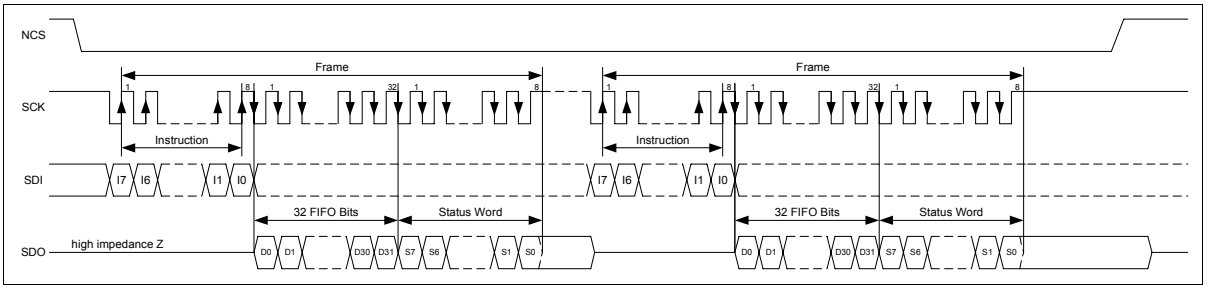

Figure 68 Read FIFO

To read the FIFO, the chip must be selected first. Therefore, the master must set the NCS line to low. After this, the instruction byte is shifted in on SDI and stored in the internal instruction register. The data bits of the FIFO are then shifted out on SDO. The following byte is a status word that contains the number of valid bits in the data packet. After completing the read operation, the master sets the NCS line to high.

Instruction Set

Instruction	Description	Instruction Format
WR	Write to chip	0000 0010
RD	Read from chip	0000 0011
RDF	Read FIFO from chip	0000 0100

2.4.19 Chip Serial Number

Every device contains a unique, preprogrammed 32-bit wide serial number. This number can be read out as registers SN0, SN1, SN2 and SN3 via the SPI interface.

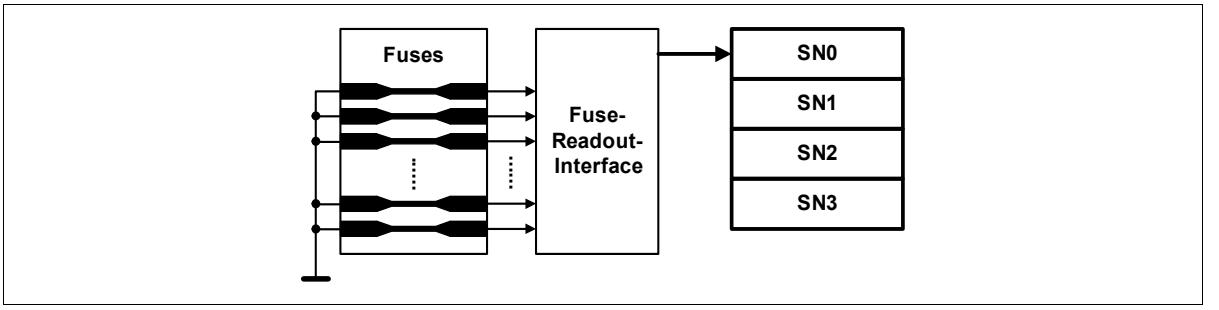

Figure 69 Chip Serial Number

Table 2 Serial Number Register

Control Register	Address	Description
SN0 SN1 SN2 SN3	0x0E 0x0F 0x10 0x11	Serial number of the IC

SN0: Serial Number Register0

ADDR: 0x0E		*Reset Value: SN*
Bit	**R/W**	**Description**
7:0	R	SN: Serial Number: Bit 7...Bit 0(LSB)

SN1: Serial Number Register1

ADDR: 0x0F		*Reset Value: SN*
Bit	**R/W**	**Description**
7:0	R	SN: Serial Number: Bit 15...Bit 8

SN2: Serial Number Register2

ADDR: 0x10		*Reset Value: SN*
Bit	**R/W**	**Description**
7:0	R	SN: Serial Number: Bit 23...Bit 16

SN3: Serial Number Register3

ADDR: 0x11			*Reset Value: SN*
Bit	**R/W**	**Description**	
7:0	R	SN: Serial Number: Bit 31 (MSB)...Bit 24	

2.4.20 Digital Input/Output Pins

As long as the pin P_ON is high, all digital output pins operate as described. If the pin P_ON is low, all digital output pins are switched to a high output impedance mode.

Interfacing to 3.3V Logic:

The TDA523x is able to interface directly to any 3.3 V logic, in 3.3 V operation mode as well as in 5 V operation mode.

Interfacing to 5V Logic:

in 5 V operation mode, all digital inputs are 5 V tolerant and can be directly connected to 5 V logic outputs. The digital outputs are able to deliver minimal 2.6 V output voltage at 500µA load current. This output level fits to TTL compatible CMOS logic inputs (e.g. 74HCTxxx). If a higher output voltage level is required, levelshifters have to be used.

EMC Reduction of Digital IO's:

Because EMC noise generated by the digital signals may influence the receiver sensitivity, it is recommended that all inputs are filtered by adding an RC circuit such as in the Evaluation Board using 10 pF and 100 Ω.

3 Register Descriptions

Due to the variety of device functions and protocols, several registers and register bits have dedicated functions according to the selected operation mode. **Modification of register settings, unless otherwise noted, is only allowed in Sleep and Hold Mode.** Registers that are defined independently for each configuration A and B are marked with “Dual”. Registers marked with “R” are read only, “W” are write only and “C” are cleared after read.

Settings for all registers are supported by the IAF TDA523x Configuration Tool!

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
SPIAT	0x00	R	0x00	SPI Address Tracer	135
SPIDT	0x01	R	0x00	SPI Data Tracer	135
CMC0	0x02	W	0x40	Chip Mode Control Register 0	135
CMC1	0x03	W	0x00	Chip Mode Control Register 1	136
IS	0x04	C	0xFF	Interrupt Status Register	137
IM	0x05	W	0x00	Interrupt Mask Register	138
RFPLLAC	0x06	R	0x00	RF PLL Actual Channel Register	138
SPMC	0x07	W	0x00	Self Polling Mode Control Register	139
SPMRT	0x08	W	0x01	Self Polling Mode Reference Timer	139
SPMOFFT0	0x09	W	0x01	Self Polling Mode Off Time Register 0	139
SPMOFFT1	0x0A	W	0x00	Self Polling Mode Off Time Register 1	140
SPMAP	0x0B	W	0x01	Self Polling Mode Active Periods Reg.	140
SPMIP	0x0C	W	0x01	Self Polling Mode Idle Periods Register	140
SN0	0x0E	R	Fuse	Serial Number Register 0	140
SN1	0x0F	R	Fuse	Serial Number Register 1	140
SN2	0x10	R	Fuse	Serial Number Register 2	141
SN3	0x11	R	Fuse	Serial Number Register 3	141
RFC	0x12	W	0x00	RF Control Register	141
CLKOUT0	0x13	W	0x07	Clock Divider Register 0	141
CLKOUT1	0x14	W	0x00	Clock Divider Register 1	141
CLKOUT2	0x15	W	0x00	Clock Divider Register2	142

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
LOC	0x16	W	0x00	Local Oscillator Control Register	142
LIMC0	0x1B	W	0x0C	Trim RSSI Gain	142
LIMC1	0x1C	W	0x15	Trim RSSI Offset, enable RSSI pin	142
ASPMONT0	0x1F	W	0x01	Conf. A Self Polling Mode On Time Reg.0	143
ASPMONT1	0x20	W	0x00	Conf. A Self Polling Mode On Time Reg.1	143
AMT	0x21	W	0x04	Conf. A Modulation Type Register	144
ARFPLL1	0x22	W	0x29	Conf. A RF PLL setting, channel 1 (Slave Mode & Self Polling Mode)	144
ARFPLL2	0x23	W	0x08	Conf. A RF PLL setting, channel 2 (Self Polling Mode)	145
ARFPLL3	0x24	W	0x0A	Conf. A RF PLL setting, channel 3 (Self Polling Mode)	146
AWUC	0x25	W	0x00	Conf. A Wake up Control Register	146
AWUPAT0	0x26	W	0x00	Conf. A Wake Up Detection Pattern 0	146
AWUPAT1	0x27	W	0x00	Conf. A Wake Up Detection Pattern 1	147
AWUBCNT	0x28	W	0x00	Conf. A Wake Up Bit Count Register	147
AMID0	0x29	W	0x00	Conf. A Message ID Register 0	147
AMID1	0x2A	W	0x00	Conf. A Message ID Register 1	147
AMID2	0x2B	W	0x00	Conf. A Message ID Register 2	147
AMID3	0x2C	W	0x00	Conf. A Message ID Register 3	147
AMID4	0x2D	W	0x00	Conf. A Message ID Register 4	147
AMID5	0x2E	W	0x00	Conf. A Message ID Register 5	147
AMID6	0x2F	W	0x00	Conf. A Message ID Register 6	147
AMID7	0x30	W	0x00	Conf. A Message ID Register 7	147
AMID8	0x31	W	0x00	Conf. A Message ID Register 8	147
AMID9	0x32	W	0x00	Conf. A Message ID Register 9	147
AMID10	0x33	W	0x00	Conf. A Message ID Register 10	147
AMID11	0x34	W	0x00	Conf. A Message ID Register 11	147
AMID12	0x35	W	0x00	Conf. A Message ID Register 12	147
AMID13	0x36	W	0x00	Conf. A Message ID Register 13	147

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
AMID14	0x37	W	0x00	Conf. A Message ID Register 14	147
AMID15	0x38	W	0x00	Conf. A Message ID Register 15	147
AMID16	0x39	W	0x00	Conf. A Message ID Register 16	147
AMID17	0x3A	W	0x00	Conf. A Message ID Register 17	147
AMID18	0x3B	W	0x00	Conf. A Message ID Register 18	147
AMID19	0x3C	W	0x00	Conf. A Message ID Register 19	147
AMIDC0	0x3D	W	0x00	Conf. A Message ID Control Register 0	147
AMIDC1	0x3E	W	0x00	Conf. A Message ID Control Register 1	148
AIF0	0x3F	W	0x00	Conf. A IF Buffer Amplifier Enable	148
BSPMONT0	0x40	W	0x01	Conf. B Self Polling Mode On Time Reg.0	143
BSPMONT1	0x41	W	0x00	Conf. B Self Polling Mode On Time Reg.1	143
BMT	0x42	W	0x04	Conf. B Modulation Type Register	144
BRFPLL1	0x43	W	0x29	Conf. A RF PLL setting, channel 1 (Slave Mode & Self Polling Mode)	144
BRFPLL2	0x44	W	0x08	Conf. A RF PLL setting, channel 2 (Self Polling Mode)	145
BRFPLL3	0x45	W	0x0A	Conf. A RF PLL setting, channel 3 (Self Polling Mode)	146
BWUC	0x46	W	0x00	Conf. B Wake up Control Register	146
BWUPAT0	0x47	W	0x00	Conf. B Wake Up Detection Pattern 0	146
BWUPAT1	0x48	W	0x00	Conf. B Wake Up Detection Pattern 1	147
BWUBCNT	0x49	W	0x00	Conf. B Wake Up Bit Count Register	147
BMID0	0x4A	W	0x00	Conf. B Message ID Register 0	147
BMID1	0x4B	W	0x00	Conf. B Message ID Register 1	147
BMID2	0x4C	W	0x00	Conf. B Message ID Register 2	147
BMID3	0x4D	W	0x00	Conf. B Message ID Register 3	147
BMID4	0x4E	W	0x00	Conf. B Message ID Register 4	147
BMID5	0x4F	W	0x00	Conf. B Message ID Register 5	147
BMID6	0x50	W	0x00	Conf. B Message ID Register 6	147
BMID7	0x51	W	0x00	Conf. B Message ID Register 7	147

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
BMID8	0x52	W	0x00	Conf. B Message ID Register 8	147
BMID9	0x53	W	0x00	Conf. B Message ID Register 9	147
BMID10	0x54	W	0x00	Conf. B Message ID Register 10	147
BMID11	0x55	W	0x00	Conf. B Message ID Register 11	147
BMID12	0x56	W	0x00	Conf. B Message ID Register 12	147
BMID13	0x57	W	0x00	Conf. B Message ID Register 13	147
BMID14	0x58	W	0x00	Conf. B Message ID Register 14	147
BMID15	0x59	W	0x00	Conf. B Message ID Register 15	147
BMID16	0x5A	W	0x00	Conf. B Message ID Register 16	147
BMID17	0x5B	W	0x00	Conf. B Message ID Register 17	147
BMID18	0x5C	W	0x00	Conf. B Message ID Register 18	147
BMID19	0x5D	W	0x00	Conf. B Message ID Register 19	147
BMIDC0	0x5E	W	0x00	Conf. B Message ID Control Register 0	147
BMIDC1	0x5F	W	0x00	Conf. B Message ID Control Register 1	148
BIF0	0x60	W	0x00	IF Buffer Amplifier Enable, B	148
XTALCAL0	0x61	W	0x10	Trim XTAL frequency, coarse	148
XTALCAL1	0x62	W	0x00	Trim XTAL frequency, fine	149
TOTIM	0x6B	W	0xFF	Time Out Timer Register	149
Digital Receiver A					
Global register					
ADIGRXC	0x6C	W	0x00	Global Settings	149
ADCSPLRDIV	0x6D	W	0x00	ADC dividing factor	150
APKBITPOS	0x6E	W	0x00	RSSI Detector Start-up Delay	150
Data filter related register					
ADATFILT0	0x6F	W	0x00	Matched Filter Scaling and Delay	150
ADATFILT1	0x70	W	0x00	Matched Filter Decimation	151
ASIGDET0	0x71	W	0x00	Signal detector (Run Mode)	151
ASIGDET1	0x72	W	0x00	Signal detector (Wake Up)	151
additional data filter related registers see end of table					
Clock recovery related register					

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
ACDR0	0x73	W	0x00	Clock recovery P parameters	153
ACDR1	0x74	W	0x00	Clock recovery I parameters	154
ACDR2	0x75	W	0x00	Clock recovery RUNIN length	154
ASYSRCT0	0x76	W	0x00	Synchronization search time out	154
ATVWIN	0x77	W	0x00	CV Window Length	155
FSK related register					
AFSKNCO0	0x78	W	0x00	FSK DDS NCO Frequency Offset	155
AFSKNCO1	0x79	W	0x00	FSK DDS NCO Frequency Offset	155
AFSKNCO2	0x7A	W	0x00	FSK DDS NCO Frequency Offset	155
AFSKFILBW0	0x7B	W	0x00	FSK Pre Filter Decimation	155
AFSKFILBW1	0x7C	W	0x00	FSK Pre Filter Scaling	156
AFSKDEMBW0	0x7D	W	0x00	FSK Demodulator Sensitivity	156
AFSKDEMBW1	0x7E	W	0x00	FSK DAM Output Decimation	156
AFSKDEMBW2	0x7F	W	0x00	FSK DAM Output Scaling	156
ANDTHRES	0x80	W	0x00	FSK Noise Detector Threshold	157
ANDCONFIG	0x81	W	0x00	FSK Noise Detector configuration	157
Framer related register					
ATSIMODE	0x82	W	0x00	TSI Detection Mode	158
ATSILENA	0x83	W	0x00	TSI A Length	158
ATSILENB	0x84	W	0x00	TSI B Length	159
ATSIGAP	0x85	W	0x00	TSI GAP	159
ATSIPTA0	0x86	W	0x00	TSI Data Reference Low Byte A	159
ATSIPTA1	0x87	W	0x00	TSI Data Reference High Byte A	159
ATSIPTB0	0x88	W	0x00	TSI Data Reference Low Byte B	160
ATSIPTB1	0x89	W	0x00	TSI Data Reference High Byte B	160
AEOMC	0x8A	W	0x00	EOM Control	160
AEOMDTLEN	0x8B	W	0x00	EOM Data Length Limit	160
Digital Receiver B					
Global register					
BDIGRXC	0x8C	W	0x00	Global Settings	149

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
BDCSPLRDIV	0x8D	W	0x00	ADC dividing factor	150
BPKBITPOS	0x8E	W	0x00	RSSI Detector Start-up Delay	150
Data filter related register					
BDATFILT0	0x8F	W	0x00	Matched Filter Scaling and Delay	150
BDATFILT1	0x90	W	0x00	Matched Filter Decimation	151
BSIGDET0	0x91	W	0x00	Signal detector (Run Mode)	151
BSIGDET1	0x92	W	0x00	Signal detector (Wake Up)	151
additional data filter related registers see end of table					
Clock recovery related register					
BCDR0	0x93	W	0x00	Clock recovery P parameters	153
BCDR1	0x94	W	0x00	Clock recovery I parameters	154
BCDR2	0x95	W	0x00	Clock recovery RUNIN length	154
BSYSRCT0	0x96	W	0x00	Synchronization search time out	154
BTVWIN	0x97	W	0x00	CV Window Length	155
FSK related register					
BFSKNCO0	0x98	W	0x00	FSK DDS NCO Frequency Offset	155
BFSKNCO1	0x99	W	0x00	FSK DDS NCO Frequency Offset	155
BFSKNCO2	0x9A	W	0x00	FSK DDS NCO Frequency Offset	155
BFSKFILBW0	0x9B	W	0x00	FSK Pre Filter Decimation	155
BFSKFILBW1	0x9C	W	0x00	FSK Pre Filter Scaling	156
BFSKDEMBW0	0x9D	W	0x00	FSK Demodulator Sensitivity	156
BFSKDEMBW1	0x9E	W	0x00	FSK DAM Output Decimation	156
BFSKDEMBW2	0x9F	W	0x00	FSK DAM Output Scaling	156
BNDTHRES	0xA0	W	0x00	FSK Noise Detector Threshold	157
BNDCONFIG	0xA1	W	0x00	FSK Noise Detector configuration	157
Framer related register					
BTSIMODE	0xA2	W	0x00	TSI Detection Mode	158
BTSILENA	0xA3	W	0x00	TSI A Length	158
BTSILENB	0xA4	W	0x00	TSI B Length	159
BTSIGAP	0xA5	W	0x00	TSI GAP	159

Table 3 Register Descriptions

Name	Addr.	R/W	Def.	Description	Page
BTSIPTA0	0xA6	W	0x00	TSI Data Reference Low Byte A	159
BTSIPTA1	0xA7	W	0x00	TSI Data Reference High Byte A	159
BTSIPTB0	0xA8	W	0x00	TSI Data Reference Low Byte B	160
BTSIPTB1	0xA9	W	0x00	TSI Data Reference High Byte B	160
BEOMC	0xAA	W	0x00	EOM Control	160
BEOMDTLEN	0xAB	W	0x00	EOM Data Length Limit	160
Status Register					
RSSI1	0xAC	R	0x00	Peak-Detector 1 read register	161
RSSI2	0xAD	C	0x00	Peak-Detector 2 read register	161
FSKNP	0xAF	R	0x00	FSK Noise Power	161
ASKNP	0xB0	R	0x00	ASK Noise Power	161
Additional data filter related registers					
APSLC	0xB4	W	0x00	Pre Slicer Control	152
BPSLC	0xB5	W	0x00	Pre Slicer Control	152
ASIGDETLO	0xB6	W	0x00	Signal Detector Threshold Low Level	152
BSIGDETLO	0xB7	W	0x00	Signal Detector Threshold Low Level	152
ASIGDETSEL	0xB8	W	0x0A	Signal Detector Factor selection	153
BSIGDETSEL	0xB9	W	0x0A	Signal Detector Factor selection	153

3.1 Detailed register descriptions

SPIAT: SPI Address Tracer

ADDR: 0x00			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	R	Address Tracer Register	

SPIDT: SPI Data Tracer

ADDR: 0x01			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
7:0	R	Data Tracer Register	

CMC0: Chip Mode Control Register 0

ADDR: 0x02			*Reset Value: 0x40*
Bit	**R/W**	**Description**	
7	W	INITFIFO: Init FIFO at Cycle Start This Initialization of the FIFO can be configured in both Slave Mode and Self Polling Mode. In Slave Mode, this happen at the beginning of the Slave Run Mode. In Self Polling Mode, initialization is done after Wake up found (switching from Self Polling Mode to Run Mode Self Polling). 0: No Init 1: Init FIFO	
6	W	CLKOUTEN: CLKOUT Enable 0: Disable 1: Enable programmable clock output	
5	W	TOTIMEN: ToTim Timer Enable Time Out Timer is used to return from Run Mode Self Polling to Self Polling Mode whenever there is no Sync for a specific time. 0: Disable 1: Enable ToTim Timer	
4	W	FIFOLK: Lock Data FIFO at EOM 0: FIFO lock is disabled 1: FIFO lock is enabled at EOM	

ADDR: 0x02		Reset Value: 0x40
Bit	**R/W**	**Description**
3	W	RMSL: Run Mode Slave Configuration This Bit is only relevant in Slave Mode, used to define the configuration 0: Configuration A 1: Configuration B
2	W	DCE: Dual Configuration Enable This Bit is only relevant in Self Polling Mode, to define whether both configurations are used. 0: Only Configuration A is used 1: First Configuration A and then Configuration B is used
1	W	SLRXEN: Slave Receiver enable This Bit is only used in Operating Mode Run Mode Slave/Sleep Mode 0: Receiver is in Sleep Mode 1: Receiver is in Run Mode Slave
0	W	MSEL: Operating Mode 0: Run Mode Slave/Sleep Mode 1: Self Polling Mode

CMC1: Chip Mode Control Register 1

ADDR: 0x03		Reset Value: 0x00
Bit	**R/W**	**Description**
6	W	HOLD: Holds the chip in the config state (only in Run Mode Slave) 0: Normal Operation 1: Jump into the config state Hold
5	W	NINTPOL: Invert NINT Polarity 0: The Interrupt is active low 1: The polarity of the Interrupt is inverted (active high)
4	W	XTALTREN: XTAL Trim Enable 0: Trimming is disabled 1: Trimming is enabled
3	W	FSINITFIFO: Init FIFO at Frame Start 0: No Init 1: Init
2	W	CLKRXDSEL: CLKOUT/RXD Pin Function 0: CLKOUT at Pin CLKOUT/RXD 1: RX-Data out at Pin CLKOUT/RXD

ADDR: 0x03		Reset Value: 0x00
Bit	**R/W**	**Description**
1	W	NINTNSTRSEL: NINT/NSTR Pin Function 0: Interrupt out at Pin NINT/NSTR 1: RX-Data Strobe out NINT/NSTR
0	W	RXRUNRXDSEL: RX-RUN/RXD Pin Function 0: RX-Run Signal out at Pin RX-RUN/RXD 1: RX-Data out at Pin RX-RUN/RXD

IS: Interrupt Status Register

ADDR: 0x04		Reset Value: 0xFF
Bit	**R/W**	**Description**
7	C	EOMB: End of Message Config.B Reset event sets all Bits to 1
6	C	MIDFB: Message ID Found Config.B Reset event sets all Bits to 1
5	C	FSYNCB: Frame Sync Config.B Reset event sets all Bits to 1
4	C	WUCFB: Wake Up Criteria Found Config.B Reset event sets all Bits to 1
3	C	EOMA: End of Message Config.A Reset event sets all Bits to 1
2	C	MIDFA: Message ID Found Config.A Reset event sets all Bits to 1
1	C	FSYNCA: Frame Sync Config.A Reset event sets all Bits to 1
0	C	WUCFA: Wake Up Criteria Found Config.A Reset event sets all Bits to 1

IM: Interrupt Mask Register

ADDR: 0x05		Reset Value: 0x00
Bit	**R/W**	**Description**
7	W	IMEOMB: Mask End of Message Config.B 0: No Mask (active) 1: Mask (inactive)
6	W	IMMIDFB: Mask Message ID Found Config.B 0: No Mask (active) 1: Mask (inactive)
5	W	IMFSYNCB: Mask Frame Sync Config.B 0: No Mask (active) 1: Mask (inactive)
4	W	IMWUCFB: Mask Wake Up Criteria Found Config.B 0: No Mask (active) 1: Mask (inactive)
3	W	IMEOMA: Mask End of Message Config.A 0: No Mask (active) 1: Mask (inactive)
2	W	IMMIDFA: Mask Message ID Found Config.A 0: No Mask (active) 1: Mask (inactive)
1	W	IMFSYNCA: Mask Frame Sync Config.A 0: No Mask (active) 1: Mask (inactive)
0	W	IMWUCFA: Mask Wake Up Criteria Found Config.A 0: No Mask (active) 1: Mask (inactive)

RFPLLAC: RF PLL Actual Channel Register

ADDR: 0x06		Reset Value: 0x00
Bit	**R/W**	**Description**
1:0	R	RFPLLACS: Actual Channel This Register is set after a Wake Up is found in the Self Polling Mode 00b: No Channel was actually found 01b: Channel 1 Wake Up according to RFPLL1 setting was found 10b: Channel 2 Wake Up according to RFPLL2 setting was found 11b: Channel 3 Wake Up according to RFPLL3 setting was found

SPMC: Self Polling Mode Control Register

ADDR: 0x07		Reset Value: 0x00
Bit	**R/W**	**Description**
3	W	PERMWUSEN: Permanent Wake Up Search enable during On-Time 0: Disabled 1: Enabled
2	W	SPMAIEN: Self Polling Mode Active Idle Enable 0: Disabled 1: Enabled
1:0	W	SPMSEL: Self Polling Mode Selection 00b: Constant On/Off 01b: Fast Fall Back to Sleep 10b: Mixed Mode (Conf. A: Const On/Off, Conf. B: Fast Fall Back to Sleep)

SPMRT: Self Polling Mode Reference Timer

ADDR: 0x08		Reset Value: 0x01
Bit	**R/W**	**Description**
7:0	W	SPMRT: Set Value Self Polling Mode Reference Timer The output of this timer is used as the input for the On/Off Timer Incoming Periodic Time = 64/fsys Output Periodic Time= T_{RT} = (64 * SPMRT) /fsys Min: 01h = (64*1)/fsys Max: 00h = (64 * 256)/fsys

SPMOFFT0: Self Polling Mode Off Time Register 0

ADDR: 0x09		Reset Value: 0x01
Bit	**R/W**	**Description**
7:0	W	SPMOFFT: Set Value Self Polling Mode Off Time: Bit 7...Bit 0(LSB) Off-Time = T_{RT} *SPMOFFT Min: 0001h = 1*T_{RT} Reg.Value 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}

SPMOFFT1: Self Polling Mode Off Time Register 1

ADDR: 0x0A			Reset Value: 0x00
Bit	**R/W**	**Description**	
5:0	W	SPMOFFT: Set Value Self Polling Mode Off Time: Bit 13(MSB)...Bit 8 Off-Tim = T_{RT} *SPMOFFT Min: 0001h = 1*T_{RT} Reg.Value 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}	

SPMAP: Self Polling Mode Active Periods Reg.

ADDR: 0x0B			Reset Value: 0x01
Bit	**R/W**	**Description**	
4:0	W	SPMAP: Set Value Self Polling Mode Active Periods. Min: 01h = 1 (Master) Period Max: 1Fh = 31 (Master) Periods Reg.Value 00h = 256 (Master) Periods	

SPMIP: Self Polling Mode Idle Periods Register

ADDR: 0x0C			Reset Value: 0x01
Bit	**R/W**	**Description**	
7:0	W	SPMIP: Set Value Self Polling Mode Idle Periods. Min: 01h = 1 (Master) Period Max: 00h = 256 (Master) Periods	

SN0: Serial Number Register 0

ADDR: 0x0E			Reset Value: SN
Bit	**R/W**	**Description**	
7:0	R	SN: Serial Number: Bit 7...Bit 0(LSB)	

SN1: Serial Number Register 1

ADDR: 0x0F			Reset Value: SN
Bit	**R/W**	**Description**	
7:0	R	SN: Serial Number: Bit 15...Bit 8	

SN2: Serial Number Register 2

ADDR: 0x10		Reset Value: SN
Bit	**R/W**	**Description**
7:0	R	SN: Serial Number: Bit 23...Bit 16

SN3: Serial Number Register 3

ADDR: 0x11		Reset Value: SN
Bit	**R/W**	**Description**
7:0	R	SN: Serial Number: Bit 31 (MSB)...Bit 24

RFC: RF Control Register

ADDR: 0x12		Reset Value: 0x00
Bit	**R/W**	**Description**
4	W	RFOFF: Switch off RF-path (for RSSI trimming) 0: RF-path enabled 1: RF-path off
3:0	W	IFATT: Adjust IF attenuation in 16 steps to trim the gain RFIN --> IF-OUT 0000: 0 dB attenuation 1111: 12 dB attenuation

CLKOUT0: Clock Divider Register 0

ADDR: 0x13		Reset Value: 0x07
Bit	**R/W**	**Description**
7:0	W	CLKOUT0: Clock Out Divider: Bit 7...Bit 0 (LSB) Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2

CLKOUT1: Clock Divider Register 1

ADDR: 0x14		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	CLKOUT1: Clock Out Divider: Bit 15...Bit 8 Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2

CLKOUT2: Clock Divider Register2

ADDR: 0x15			Reset Value: 0x00
Bit	**R/W**	**Description**	
3:0	W	CLKOUT2: Clock Out Divider: Bit 19 (MSB)...Bit 16 Min: 0 00 01h = Clock divided by 2 Max: 0 00 00h = Clock divided by (2^20)*2	

LOC: Local Oscillator Control Register

ADDR: 0x16			Reset Value: 0x00
Bit	**R/W**	**Description**	
7:5	W	Always set to 0	
4	W	SSBSEL: Local Oscillator Injection Mode Selection 0: Lo-Side LO Injection..use for TDA5230 1: Hi-Side LO Injection..use for TDA5231	
3:0	W	Always set to 0	

LIMC0: Trim RSSI Gain

ADDR: 0x1B			Reset Value: 0x0C
Bit	**R/W**	**Description**	
4:0	W	LIMGAIN: Trim the RSSI Gain (Slope) Min: 00h = Minimum gain Max: 1Fh = Maximum gain	

LIMC1: Trim RSSI Offset, enable RSSI pin

ADDR: 0x1C			Reset Value: 0x15
Bit	**R/W**	**Description**	
6:5	W	RSSIMTR: Select signal for RSSI pin 00b: RSSI+ 01b: RSSI- (reference) 10b: REF+ (reference) 11b: REF- (reference)	

ADDR: 0x1C		Reset Value: 0x15
Bit	**R/W**	**Description**
4	W	RSSIMONE: Enable buffer for RSSI pin 0: buffer off 1: buffer on
3:0	W	LIMOFFS: Trim the RSSI Offset Min: 0h = Minimum offset Max: Fh= Maximum offset

Dual: ASPMONT0 and BSPMONT0: Conf. A Self Polling Mode On Time Reg.0

ADDR: 0x1F and 0x40		Reset Value: 0x01
Bit	**R/W**	**Description**
7:0	W	SPMONT: Set Value Self Polling Mode On Time: Bit 7...Bit 0(LSB) On-Tim = T_{RT} *SPMONT Min: 0001h = 1*T_{RT} Reg.Value: 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}

Dual: ASPMONT1 and BSPMONT1: Conf. A Self Polling Mode On Time Reg.1

ADDR: 0x20 and 0x41		Reset Value: 0x00
Bit	**R/W**	**Description**
5:0	W	SPMONT: Set Value Self Polling Mode On Time: Bit 13(MSB)...Bit 8 On-Tim = T_{RT} * SPMONT Min: 0001h = 1*T_{RT} Reg.Value: 3FFFh = 16383*T_{RT} Max: 0000h = 16384*T_{RT}

Dual: AMT and BMT: Conf. A Modulation Type Register

ADDR: 0x21 and 0x42		*Reset Value: 0x04*
Bit	**R/W**	**Description**
3:2	W	NOC:: Number of Channels Only used in the Self Polling Mode to define how many channels are to be scanned. In the Slave Mode, only one channel used, regardless of the configuration. Min: 01b = 1 channel Max: 11b= 3 channels
1:0	W	MT: Modulation Type

	Run Mode Slave	Self Polling Mode	Run Mode Self Polling
00b	ASK	ASK	ASK
01b	FSK	FSK	FSK
10b	ASK	FSK	ASK
11b	FSK	ASK	FSK

Dual: ARFPLL1 and BRFPLL1:Conf. A RF PLL setting, channel 1 (Slave Mode & Self Polling Mode)

ADDR: 0x22 and 0x43		*Reset Value: 0x29*
Bit	**R/W**	**Description**
6:5	W	RFPLLA: Band Selection 00 : select 315 MHz band, A=3 01 : select 434 MHz band, A=2 10 : select 868 MHz band, A=1

ADDR: 0x22 and 0x43		Reset Value: 0x29
Bit	**R/W**	**Description**
4:2	W	RFPLLR1: Channel 1, PLL Divider Factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS1: Channel 1, PLL Divider Factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

1) Channels with receive frequencies close to the harmonics of the reference crystal frequency should not be used in applications.

Dual: ARFPLL2 and BRFPLL2:Conf. A RF PLL setting, channel 2 (Self Polling Mode)

ADDR: 0x23 and 0x44		Reset Value: 0x08
Bit	**R/W**	**Description**
4:2	W	RFPLLR2: Channel 2, PLL Divider Factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS2: Channel 2, PLL Divider Factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

Dual: ARFPLL3 and BRFPLL3:Conf. A RF PLL setting, channel 3 (Self Polling Mode)

ADDR: 0x24 and 0x45		*Reset Value: 0x0A*
Bit	**R/W**	**Description**
4:2	W	RFPLLR3: Channel 3, PLL Divider Factor R[1)] 000 : R = 8 001 : R = 1 010 : R = 2 011 : R = 3 100 : R = 4 101 : R = 5 110 : R = 6 111 : R = 7
1:0	W	RFPLLS3: Channel 3, PLL Divider Factor S[1)] 00 : S = 1 01 : S = 0 10 : S = -1 11 : S = 0

1) Channels with receive frequencies close to the harmonics of the reference crystal frequency should not be used in applications.

Dual: AWUC and BWUC: Conf. A Wake up Control Register

ADDR: 0x25 and 0x46		*Reset Value:0x00*
Bit	**R/W**	**Description**
1:0	W	WUCRT: Wake Up Criteria 00b: Pattern Detection 01b: Random Bits 10b: Equal Bits 11b: Wake Up on Symbol Sync, Valid Data Rate; the WUBCNT Register is not used in this mode.

Dual: AWUPAT0 and BWUPAT0: Conf. A Wake Up Detection Pattern 0

ADDR: 0x26 and 0x47		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	WUPAT0: Wake Up Detection Pattern: Bit 7...Bit 0(LSB) (in Chips)

Dual: AWUPAT1 and BWUPAT1: Conf. A Wake Up Detection Pattern 1

ADDR: 0x27 and 0x48		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	WUPAT1: Wake Up Detection Pattern: Bit 15(MSB)...Bit 8 (in chips)

Dual: AWUBCNT and BWUBCNT: Conf. A Wake Up Bit Count Register

ADDR: 0x28 and 0x49		*Reset Value:0x00*
Bit	**R/W**	**Description**
6:0	W	WUBCNT: Wake Up Bit Count Register Counter Register to define the maximum counts of chips for Wake Up detection. Min: 00h = 0 chips to count In “Random Bits” or “Equal Bits” Mode, this will cause a Wake Up immediately after Symbol Synchronization is found. In “Pattern Detection” Mode this will cause no Wake Up found. In this Mode, a minimum of 11h= 17 Chips= 8 1/2 Bits is needed to shift one Pattern through the entire Pattern Detector because comparison can only be started when at least the comparison register is fully filled. Max: 7Fh: 127 Chips to count after Symbol Sync found

Dual: AMID0-AMID19 and BMID0-BMID19: Conf. A Message ID Register 0

ADDR: 0x29-0x3C and 0x4A-0x5D		*Reset Value:0x00*
Bit	**R/W**	**Description**
7:0	W	MID0: Message ID Register

Dual: AMIDC0 and BMIDC0: Conf. A Message ID Control Register 0

ADDR: 0x3D and 0x5E		*Reset Value:0x00*
Bit	**R/W**	**Description**
6:0	W	SP: MID Scan Start Position Min: 00h = Comparison starts one Bit after FSYNC Max: 7F = Comparison starts 128 Bits after FSYNC

Dual: AMIDC1 and BMIDC1: Conf. A Message ID Control Register 1

ADDR: 0x3E and 0x5F			*Reset Value:0x00*
Bit	**R/W**	**Description**	
3	W	MIDSEN: Enable ID Screening 0: Disabled 1: Enabled	
2	W	MIDBO: Message ID Organization 0: 2-Byte 1: 4-Byte	
1:0	W	MIDNTS: Message ID Number of Bytes To Scan Min: 00b = 1 Byte to scan Max for 2-Byte organization: 01b: 2 bytes to scan. Higher values than 01b will be mapped automatically to 2 bytes to scan Max for 4-Byte organization: 11b= 4 bytes to scan	

Dual: AIF0 and BIF0: Conf. A IF Buffer Amplifier Enable

ADDR: 0x3F and 0x60			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
1	W	IFBUF: Enable IF-Buffer amplifier 0: Buffer disabled 1: Buffer enabled	
0	W	IFMUX: select IF-limiter input 0: use pin LIM-IN+ as input 1: use pin IFBUF-IN as input	

XTALCAL0: Trim XTAL frequency, coarse

ADDR: 0x61			*Reset Value: 0x10*
Bit	**R/W**	**Description**	
4	W	XTAL_SW_COARSE_4: Connect trim capacitor: 16 pF	
3	W	XTAL_SW_COARSE_3: Connect trim capacitor: 8 pF	
2	W	XTAL_SW_COARSE_2: Connect trim capacitor: 4 pF	
1	W	XTAL_SW_COARSE_1: Connect trim capacitor: 2 pF	
0	W	XTAL_SW_COARSE_0: Connect trim capacitor: 1 pF	

XTALCAL1: Trim XTAL frequency, fine

ADDR: 0x62			*Reset Value: 0x00*
Bit	**R/W**	**Description**	
3	W	XTAL_SW_FINE_3: Connect trim capacitor: 500 fF	
2	W	XTAL_SW_FINE_2: Connect trim capacitor: 250 fF	
1	W	XTAL_SW_FINE_1: Connect trim capacitor: 125 fF	
0	W	XTAL_SW_FINE_0: Connect trim capacitor: 62.5 fF	

TOTIM: Time Out Timer Register

ADDR: 0x6B		*Reset Value: 0xFF*
Bit	**R/W**	**Description**
7:0	W	TO_TIMER: Set value time out timer Timer is used to return from Run Mode Self Polling to the Self Polling Mode whenever there is no Symbol Synchronization. Timer is set back after EOM. TOTIM must be enabled in the **CMC0** register. TimeOut= (TOTIM * 64 * 512) / fsys Min: 01h = (1 * 64 *512)/ fsys Max: 00h= (256 * 64 * 512) / fsys

Dual: ADIGRXC and BDIGRXC: Global Settings

ADDR: 0x6C and 0x8C		*Reset Value: 0x00*
Bit	**R/W**	**Description**
2:1	W	AAFILT: Anti Aliasing Filter 00b: 40kHz (default) 01b: 13.6kHz 10b: 5kHz 11b: 3.6kHz The anti-aliasing filter corner frequency can be changed to achieve better performance. Note that the corner frequency and the data rate must be set together.
0	W	DATINV 0: default 1: Invert data polarity

Dual: ADCSPLRDIV and BDCSPLRDIV: ADC dividing factor

ADDR: 0x6D and 0x8D		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	ADCDIV: ADC Sampling Rate Division Factor. The ADC sampling rate factor must be calculated together with ASKDEC. Note that for better performance, the highest possible ADC sampling rate should be set. $$ADCDIV = round\left(\frac{f_{sys}}{f_{ADC}}\right) - 1\Big|_{f_{ADC} = [96 \ldots 320kHz]}$$

Dual: APKBITPOS and BPKBITPOS: RSSI Detector Start-up Delay

ADDR: 0x6E and 0x8E		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	RSSI Detector Start-up Delay[1)] Min: 00h: 0 bit delay (Start with first bit after FSYNC) Max: FFh: 255 bits delay

1) Due to filtering and signal computation the latency T_1 and T_2 must be added (see also Chapter 2.4.9.1)

Dual: ADATFILT0 and BDATFILT0: Matched Filter Scaling and Delay

ADDR: 0x6F and 0x8F		Reset Value: 0x00
Bit	**R/W**	**Description**
5:3	W	ASKSCA: CIC-filter Input Scaling Factor[1)] 000b: default
2:0	W	ASKDEL: CIC-filter cmb Section delay Factor[1)2)] 110b: default For better performance from reduced duty and data rate errors set 111b.

1) use default value

2) the CIC filter delay = ASKDEL + 1

Dual: ADATFILT1 and BDATFILT1: Matched Filter Decimation

ADDR: 0x70 and 0x90		Reset Value: 0x00
Bit	**R/W**	**Description**
5:0	W	ASKDEC: CIC-filter Decimation Factor: Choose the highest possible ADC sampling rate for the best performance $$ASKDEC = round\left(\frac{f_{ADC}}{16 \cdot f_{data}}\right) - 1 \Big|_{f_{ADC} = \frac{f_{sys}}{ADCDIV + 1}}$$

Dual: ASIGDET0 and BSIGDET0: Signal detector (Run Mode)

ADDR: 0x71 and 0x91		Reset Value: 0x00
Bit	**R/W**	**Description** (For detailed procedure refer to Application Notes.)
7:6	W	SDCNT: Signal Detector Threshold Counter (Run Mode) use 00b: disabled
5:0	W	SDTHR: Signal Detector Threshold Level (Run Mode)[1)] See application notes *"How to choose an Application specific Signal Detection Threshold for TDA523x based ASK Mode Applications"* and *"How to Choose an Application Specific Signal- and Noise-Detection Threshold for TDA523x based FSK Mode Applications" for specific procedure to determine this threshold by application*.

1) For threshold calculation use the **ASKNP: ASK Noise Power** register.

Dual: ASIGDET1 and BSIGDET1: Signal detector (Wake Up)

ADDR: 0x72 and 0x92		Reset Value: 0x00
Bit	**R/W**	**Description** (For detailed procedure refer to Application Notes.)
7:6	W	SDCNT: Signal Detector Threshold Counter (Wake Up) use 00b: disabled
5:0	W	SDTHR: Signal Detector Threshold Level (Wake Up) See application notes *"How to choose an Application specific Signal Detection Threshold for TDA523x based ASK Mode Applications"* and *"How to Choose an Application Specific Signal- and Noise-Detection Threshold for TDA523x based FSK Mode Applications" for specific procedure to determine this threshold by application*.

Dual: APSLC and BPSLC: Pre Slicer Control

ADDR: 0xB4 and 0xB5		Reset Value: 0x00
Bit	**R/W**	**Description**
7	W	PSLCDA: Pre-Slicer disable 0: Pre-Slicer enable: only used in combination with TSI GAP Mode using standard settings as below! 1: Pre-Slicer disable (default)
6:5	W	PSLCHYS: Pre-Slicer hysteresis use 01b
4:0	W	PSLCTHR: Pre-Slicer disable threshold use 10010 (0x12).

Dual: ASIGDETLO and BSIGDETLO: Signal Detector Threshold Low Level

ADDR: 0xB6 and 0xB7		Reset Value: 0x00
Bit	**R/W**	**Description** (For detailed procedure refer to application note.)
7	W	SDLORE: Source selection of ASK Noise Power status register 0: ASK Noise for SIGDET0/1 1: Signal for minimal usable FSK deviation If enabled, the SIGDET low level can be read out from ASKNP register
6	W	SDSEL: Manual selection of SIGDET range[1)] 0: Disable(default) - SIGDET0/1 range selection factor automatically done; depending on data rate 1: Enable - Use SIGDETSEL control to set the valid range
5:0	W	SDLOTHR: Signal Detector Threshold Low Level. This threshold level is only valid if the FSK Noise detector selection in the NDCONFIG register is set to “11b” See application notes *“How to choose an Application specific Signal Detection Threshold for TDA523x based ASK Mode Applications”* and *“How to Choose an Application Specific Signal- and Noise-Detection Threshold for TDA523x based FSK Mode Applications” for specific procedure to determine this threshold by application*.

1) Use default value

Dual: ASIGDETSEL and BSIGDETSEL: Signal Detector Factor selection

ADDR: 0xB8 and 0xB9		*Reset Value: 0x0A*
Bit	**R/W**	**Description**
3:2	W	SDSELLO: SIGDETLO Range Selection Factor 00b: 2 01b: 4 10b: 6 (default value) 11b: 8 The selected Signal Detector value is divided by the 2^Range Selection Factor. Use the right setting suitable to the measured ASKNP value.
1:0	W	SDSEL: SIGDET0/1 Range Selection Factor 00b: 4 01b: 6 10b: 8 (default value) 11b: 10 The selected Signal Detector value is divided by the 2^Range Selection Factor. Use the right setting suitable to the measured ASKNP value.

Dual: ACDR0 and BCDR0: Clock recovery P parameters

ADDR: 0x73 and 0x93		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:6	W	PDSR: Peak-Detector slew rate use 11b
5	W	PHDEN(1): Phase detector error (PDE) outer tolerance range use 1b
4	W	PHDEN(0): Phase detector error (PDE) inner tolerance range use 0b
3:2	W	PVAL: P Value use 01b
1:0	W	PSAT: P Value Saturation use 10b

Dual: ACDR1 and BCDR1: Clock recovery I parameters

ADDR: 0x74 and 0x94		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:6	W	CORSAT: Correlator Output Value (Timing extrapolation unit) use 01b
5:4	W	LFSAT: Loop Filter Saturation use 10b
3:2	W	IVAL: I Value use 01b
1:0	W	ISAT: I Value Saturation use 01b

Dual: ACDR2 and BCDR2: Clock recovery RUNIN length

ADDR: 0x75 and 0x95		*Reset Value: 0x00*
Bit	**R/W**	**Description**
1:0	W	RUNLEN: RUNIN length use 01b: 3 1/2 bits (default)

Dual: ASYSRCT0 and BSYSRCT0: Synchronization search time out

ADDR: 0x76 and 0x96		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	SYNCTO: Synchronization search time out FFh: 15 15/16 bits 00h: 0 bit

Dual: ATVWIN and BTVWIN: CV Window Length

ADDR: 0x77 and 0x97		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TVWIN: CV Window Length 28h: 40/16 bits FFh: 255/16 bits The minimal value for the TVWIN Register must be configured to 1 CV=28h ((8 + 16 *CV + 8)*1.25). Note that if the TSIGAP framer mode is used (e.g. 8-bit Gap protocol) the value must be higher and is dependent on other TSI framer settings.

Dual: AFSKNCO0 and BFSKNCO0: FSK DDS NCO Frequency Offset

ADDR: 0x78 and 0x98		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	NCOINC: FSK NCO Register Bits (7:0) LSB

Dual: AFSKNCO1 and BFSKNCO1: FSK DDS NCO Frequency Offset

ADDR: 0x79 and 0x99		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	NCOINC: FSK NCO Register Bits (15:8)

Dual: AFSKNCO2 and BFSKNCO2: FSK DDS NCO Frequency Offset

ADDR: 0x7A and 0x9A		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	NCOINC: FSK NCO Register Bits (23:16) MSB

Dual: AFSKFILBW0 and BFSKFILBW0: FSK Pre Filter Decimation

ADDR: 0x7B and 0x9B		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3:0	W	FSKDEC: FSK Pre-Filter Decimation Factor 0001b: ±250 pre-filter bandwidth (recommended) 0011b: ±125 pre-filter bandwidth 0111b: ±62.5 pre-filter bandwidth 1111b: ±31.25 pre-filter bandwidth

Dual: AFSKFILBW1 and BFSKFILBW1: FSK Pre Filter Scaling

ADDR: 0x7C and 0x9C		Reset Value: 0x00
Bit	**R/W**	**Description**
6:4	W	FSKSCA: FSK Pre-Filter Scaling $FSKSCA_{dec} = \left(14 - round\left(\frac{\log((FSKFILBW0 + 1) \cdot 9)}{\log(2)} + 4\right)\right)$
3:0	W	FSKDEL: FSK Pre-Filter Comb Delay Setting use 1000b: default

Dual: AFSKDEMBW0 and BFSKDEMBW0: FSK Demodulator Sensitivity

ADDR: 0x7D and 0x9D		Reset Value: 0x00
Bit	**R/W**	**Description**
7:4	W	not used
3:0	W	DAMDLY: FSK Demodulator Sensitivity use 0100b: default

Dual: AFSKDEMBW1 and BFSKDEMBW1: FSK DAM Output Decimation

ADDR: 0x7E and 0x9E		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	DAMDEC: FSK DAM Decimation $DAMDEC_{dec} = round\left(\frac{f_{sys}}{(FSKFILBW0 + 1) \cdot (DATFILT1 + 1) \cdot f_{data} \cdot 16}\right) - 1$

Dual: AFSKDEMBW2 and BFSKDEMBW2: FSK DAM Output Scaling

ADDR: 0x7F and 0x9F		Reset Value: 0x00
Bit	**R/W**	**Description**
3:0	W	DAMSCA: FSK DAM Output Scaling $DAMSCA_{dec} = rounddown\left(\frac{\log(FSKDEMBW1 + 1)}{\log(2)}\right)$

Dual: ANDTHRES and BNDTHRES: FSK Noise Detector Threshold

ADDR: 0x80 and 0xA0		Reset Value: 0x00
Bit	**R/W**	**Description** (For detailed procedure refer to application note.)
7:0	W	NDTHRES: FSK Noise Detector Threshold[1)] See application notes *"How to choose an Application specific Signal Detection Threshold for TDA523x based ASK Mode Applications"* and *"How to Choose an Application Specific Signal- and Noise-Detection Threshold for TDA523x based FSK Mode Applications" for specific procedure to determine this threshold by application.*

1) For threshold calculation use the **FSKNP: FSK Noise Power** register.

Dual: ANDCONFIG and BNDCONFIG: FSK Noise Detector configuration

ADDR: 0x81 and 0xA1		Reset Value: 0x00
Bit	**R/W**	**Description**
5:4	W	NDSEL: FSK Noise Detector Selection 00b: Squelch only (signal power) • signal power detection only (related registers **Dual: ASIGDET0 and BSIGDET0: Signal detector (Run Mode)**, **Dual: ASIGDET1 and BSIGDET1: Signal detector (Wake Up)** and **ASKNP: ASK Noise Power**). This mode should be used for ASK and FSK. 01b: FSK Noise Detector only (noise power) • noise power detection only (related registers **Dual: ANDTHRES and BNDTHRES: FSK Noise Detector Threshold** and **FSKNP: FSK Noise Power**). This mode should be used for FSK signals with small deviations. 10b: Both (Squelch and FSK Noise Detector) • signal and noise power detection simultaneous. 11b: Squelch and (FSK Noise Detector and SIGDETLO threshold) • signal and noise power detection simultaneous but the FSK noise detect signal is valid if the SIGDETLO threshold is exceeded only. This mode is used for FSK with low FSK deviations.
3:2	W	ND(3:2): FSK Noise Detector configuration: threshold level use 01b:
1:0	W	ND(1:0) FSK Noise Detector configuration: Peak-Detector slew rate use 11b

Dual: ATSIMODE and BTSIMODE: TSI Detection Mode

ADDR: 0x82 and 0xA2		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7	W	TSIGRSYN: TSI Gap Resync Mode (For detailed information, see ATSIGAP/BTSIGAP register description) 0: OFF (default) 1: PLL reset after TSI Gap
6:3	W	TSIWCA: Wild Cards for Correlator A
2	W	MANCPAJ: Manchester Code Phase Readjustment 0: disabled - Manchester code polarity is defined by the TSI pattern. 1: enabled - the code phase readjustment will be done with each “1001” or “0110” Manchester data change.
1:0	W	TSIDETMOD: TSI Detection Mode 00b: 16-Bit Mode - TSI configuration A AND B valid (sequentially), B is valid if the ATSILENB>0 01b: 8-Bit Mode - TSI configurations A OR B (parallel) 10b: 8-Bit Gap Mode- TSI configurations A AND B with Gap (sequentially with Gap between TSIA & TSIB) 11b: 8-Bit extended Mode - TSI configurations A OR B (parallel with matching information), synchronization will be done on full TSI length, dependent on found TSI A or B, 0 or 1 will be sent as 1st received bit.

Dual: ATSILENA and BTSILENA: TSI A Length

ADDR: 0x83 and 0xA3		*Reset Value: 0x00*
Bit	**R/W**	**Description**
4:0	W	TSI A Length (in chips): (0x11 up to 0x1F not used) Min: 00h = 0 Bit; Does only work in 16-Bit Mode: FSYNC will be generated after Symbol Synchronization. In other Modes the smallest possible value to generate a FSYNC will be 01h. Be aware that such small values makes it impossible to find the correct phase of the pattern in the data stream and, therefore, wrong data and code violations can be generated. Max: 10h = 16 chips = 8 bits

Dual: ATSILENB and BTSILENB: TSI B Length

ADDR: 0x84 and 0xA4		Reset Value: 0x00
Bit	**R/W**	**Description**
4:0	W	TSI B Length (in chips): (0x11 up to 0x1F not used) Min: 00h =0 bit (see also ATSILENA) Max: 10h = 16 chips = 8 bits

Dual: ATSIGAP and BTSIGAP: TSI GAP

ADDR: 0x85 and 0xA5		Reset Value: 0x00
Bit	**R/W**	**Description**
7:3	W	TSIGAP: TSI Gap (T/2 bit resolution) 1Fh: 15 1/2 bits gap 00h: 0 bit gap TSIGAP is used to lock the PLL after TSI A is found, if the TSI detection mode 10b is selected.
2:0	W	GAPVAL: TSI Gap (T/16 bit resolution) 111b: 7/16 bit gap 000b: 0 bit gap GAPVAL is used to correct the DCO phase after TSIGAP time, if the TSIMODE.TSIGRSYN is disabled

Dual: ATSIPTA0 and BTSIPTA0: TSI Data Reference Low Byte A

ADDR: 0x86 and 0xA6		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	TSIPTA0: Data Pattern for TSI comparison : Bit 7...Bit 0(LSB) (in chips)

Dual: ATSIPTA1 and BTSIPTA1: TSI Data Reference High Byte A

ADDR: 0x87 and 0xA7		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	W	TSIPTA1: Data Pattern for TSI Comparison: Bit 15(MSB)...Bit 8 (in chips)

Dual: ATSIPTB0 and BTSIPTB0: TSI Data Reference Low Byte B

ADDR: 0x88 and 0xA8		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTB0: Data Pattern for TSI Comparison (in chips)

Dual: ATSIPTB1 and BTSIPTB1: TSI Data Reference High Byte B

ADDR: 0x89 and 0xA9		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	TSIPTB1: Data Pattern for TSI Comparison (in chips)

Dual: AEOMC and BEOMC: EOM Control

ADDR: 0x8A and 0xAA		*Reset Value: 0x00*
Bit	**R/W**	**Description**
3	W	Not used: always set to 0
2	W	EMSYLO: EOM by Sync Loss[1)]
1	W	EMCV: EOM by Code Violation[1)]
0	W	EMDATLEN: EOM by Data Length[1)]

1) The EOM criteria can be combined.

Dual: AEOMDTLEN and BEOMDTLEN: EOM Data Length Limit

ADDR: 0x8B and 0xAB		*Reset Value: 0x00*
Bit	**R/W**	**Description**
7:0	W	DATLEN: Length of Data Field in Telegram Counting starts after the last TSI Bit Min: 00h = The next Bit after TSI found (when EOM criteria is EMDATLEN) will generate EOM Max: FFh

FSKNP: FSK Noise Power

ADDR: 0xAF		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	R	FSK Noise Power The read only register contains the actual noise power that should be used to set the **Dual: ANDTHRES and BNDTHRES: FSK Noise Detector Threshold** register.

ASKNP: ASK Noise Power

ADDR: 0xB0		Reset Value: 0x00
Bit	**R/W**	**Description**
5:0	R	ASK Noise Power The read only register contains the actual noise power that should be used to set the **Dual: ASIGDET0 and BSIGDET0: Signal detector (Run Mode)** and **Dual: ASIGDET1 and BSIGDET1: Signal detector (Wake Up)** register.

RSSI1: Peak-Detector 1 read register

ADDR: 0xAC		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	R	RSSI: Peak Level During Payload Tracking started after FSYNC + PKBITPOS Set at EOM Cleared at Reset

RSSI2: Peak-Detector 2 read register

ADDR: 0xAD		Reset Value: 0x00
Bit	**R/W**	**Description**
7:0	C	RSSI: Peak Level. Tracking is active when Digital Receiver is enabled Set at higher peak levels than stored Cleared at Reset and SPI read out

4 Specifications

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: The AC/DC characteristic limits are not guaranteed. The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as latch-up or permanent damage to the IC may result.

Table 4 Absolute Maximum Ratings, T_{amb} = -40 °C … +105 °C

#	Parameter	Symbol	Limit Values		Unit
			min.	max.	
A.1	Voltage range at pin VDD5V	V_{VCCmax}	-0,3	6	V
A.2	Voltage range at pin VDDD, VDDA	V_{VCCmax}	-0,3	4	V
A.3	Voltage between voltage-regulator terminals VDD5V vs. VDDD and VDD5V vs.VDDA	V_{VCCmax}	-0,3	4	V
A.4	Storage ambient temperature	$T_{storage}$	-40	150	°C
A.5	Thermal resistance junction to air	$R_{th(ja)}$		140	K/W
A.6	Total power dissipation at Tamb=105°C	P_{tot}		100	mW
A.7	RF input power (500 Ω source between pin RFIN+ and pin RFIN-)	P_{RFIN}		0	dBm
A.8	ESD classification: human body model	V_{HBM}		2	kV
A.9	Maximum input voltage at digital input pins	V_{inmax}	-0,3	VDD5V + 0,5 or 6 (whichever is lower)	V
A.10	High level DC-output current (digital output pins) 1 pin all pins	 I_{OH1} I_{OHAll}	 -1 -4		 mA mA
A.11	Low level DC-output current (digital output pins) 1 pin all pins	 I_{OL1} I_{OLAll}		 1 4	 mA mA
A.12	Maximum current to digital input and output pins	I_{IOmax}		4	mA

4.1.2 Operating Ratings

Table 5 Operating Ratings

#	Parameter	Symbol	Limit Values			Unit
			min.	Typ.	max.	
A.13	Operating ambient temperature	T_{amb}	-40		105	°C
A.14	Supply voltage range 1 at pin VDD5V	V_{DD5V}	4.5		5.5	V
A.15	Supply voltage range 2 at pin VDD5V=VDDD=VDDA	V_{DD3V3}	3.0		3.6	V
A.16	Percentage of operating time of lifetime Condition: T_{amb} = -40 °C T_{amb} = 25 °C T_{amb} = 85 °C T_{amb} = 105 °C	$t_{mission\_profile}$		 6 20 65 9	 % % % %	
A.17	Useful lifetime	T_{Life}	15			years

4.1.3 AC/DC Characteristics

Table 6 AC/DC Characteristics, TA = -40 to 105 °C, VDD5V = 5 V or VDD5V = VDDA = VDDD = 3,3 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
General								
B.1	**TDA5230** Supply current in Run Mode (excluding IF buffer)	$I_{VDDrun,ASK}$		7.6	9.6	mA	2 kBit; ASK; Pin < -50 dBm	
B.1E	**TDA5231** Supply current in Run Mode (excluding IF buffer)	$I_{VDDrun31,ASK}$		8.0	10.1	mA	2 kBit; ASK; Pin < -50 dBm	
B.2	**TDA5230** Supply current in Run Mode (excluding IF buffer)	$I_{VDDrun,FSK}$		8.0	10	mA	2 kBit; FSK; Pin < -50 dBm	
B.2E	**TDA5231** Supply current in Run Mode (excluding IF buffer)	$I_{VDDrun31,FSK}$		8.4	10.5	mA	2 kBit; FSK; Pin < -50 dBm	
B.3	Supply current in Sleep Mode T_{amb} = 25 °C T_{amb} = 85 °C T_{amb} = 105 °C	$I_{VDDsleep,low}$		 40 60 90	 50 90 140	 µA µA µA	crystal oscillator in low precision mode; clock generation unit off	
B.4	Supply current in Sleep Mode and crystal oscillator in high precision mode	$I_{VDDsleep,high}$			220	µA	Ctrim = 32 pF; clock generation unit off	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
B.5	Supply current in Power Down Mode T_{amb} = 25 °C T_{amb} = 85 °C T_{amb} = 105 °C	$I_{VDDpdwn}$		 0.6 3 6	 1.5 12 25	 µA µA µA	VDD5V = VDDA = VDDD = 3.6 V	
B.6	Supply current in Power Down Mode T_{amb} = 25 °C T_{amb} = 85 °C T_{amb} = 105 °C	$I_{VDDpdwn}$		 0.8 2.5 5	 1.5 10 20	 µA µA µA	VDD5V = 5.5 V	
B.7	Supply current of IF buffer-amplifier	I_{buff}		0.5	0.7	mA	P_{in} < -50 dBm	
B.8	Supply current of clock generation unit	$I_{VDDclock}$		20	25	µA	f_{CLKOUT} =1 kHz C_{Load} =10 pF	
B.9	Receiver reset time	t_{Reset}	0,8		5	ms		
B.10	Brownout threshold	V_{BOR}		2,45		V		
B.11	Receiver startup time	$t_{RXstartup}$	119	Note 1	119	64*T_{sys} Note 2	Time to startup RF-Frontend (comprises time required to switch crystal oscillator from low power to high precision mode)	*
B.12	Channel Hop Latency Time and Configuration Change Latency Time (Configuration A to B)	t_{CHHOP}	12	Note 1	12	64*T_{sys}	Time to switch RF-PLL between different RF-Channels. (does not include settling of the data clock recovery.)	*
B.13	RF-Frontend startup delay	$t_{RFstartdelay}$	72	Note 1	72	64*T_{sys}	Delay of startup of RF-Frontend	*
B.14	Interrupt duration	t_{INT}	1	Note 1 Note 3	1	64*T_{sys}	Pulse width of interrupt	*
B 15	P_ON minimal pulse width	t_{P_ON}	100			µs	Minimum pulse width to reset the chip	*
B 16	Minimal $T_{MasterPeriod}$	$T_{MasterPeriod}$	5	Note 4		ms	Minimal Masterperiod for stable operation	*
RF Characteristics								
C.1	**TDA5230** RF-PLL Operational frequency band 1 Operational frequency band 2	 f_{band1} f_{band2}	 433 865		 450 870	 MHz MHz	Lo-Side LO Injection	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
C.1E	**TDA5231** RF-PLL Operational frequency band 1	$f_{band1,31}$	302		320	MHz	Hi-Side LO Injection	
C.2	Receiver input impedance f_{RF} = 315 MHz f_{RF} = 434 MHz f_{RF} = 868 MHz	 $R_{RFIN315}$ $C_{RFIN315}$ $R_{RFIN434}$ $C_{RFIN434}$ $R_{RFIN868}$ $C_{RFIN868}$		 610 0.8 550 0.6 620 0.5		 Ω pF Ω pF Ω pF	parallel equivalent circuit; differentially between RFIN+ vs. RFIN-; Run-Mode	*
C.3	Voltage Gain RFIN → IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	G_{RF,min_att}		41		dB	min. IF attenuation	
C.4	1dB compression point RFIN →IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	P_{1dB,min_att}		-33		dBm	min. IF attenuation	*
C.5	Input 3rd order intercet point RFIN →IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	$IIP3_{min\_att}$		-22		dBm	min. IF attenuation	*
C.6	Voltage Gain RFIN →IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	G_{RF,max_att}		29		dB	max. IF attenuation	
C.7	1dB compression point RFIN →IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	P_{1dB,max_att}		-21		dBm	max. IF attenuation	*
C.8	Input 3rd order intercet point RFIN →IF-OUT RF-IN matched to 50 Ω IF-OUT loaded with 330 Ω	$IIP3_{max\_att}$		-13		dBm	max. IF attenuation	*
C.9	Image rejection (CW-Image at Df = 2•10.7 MHz)	a_{image}	30			dB	Pin = -50 dBm	
C.10	IF output impedance (IF-OUT)	Z_{IFout}		330		Ω		*

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
C.11	Emission at pins RFIN+ and RFIN- f_{RF} = 315 MHz f_{RF} = 434 MHz f_{RF} = 868 MHz	 P_{LO315} P_{4LO315} P_{VCO315} P_{LO434} P_{4LO434} P_{VCO434} P_{LO868} P_{VCO868}		 -106 -108 -84 -91 -102 -88 -84 -79		 dBm dBm dBm dBm dBm dBm dBm dBm	Single ended matching of input pins to 50 Ω; measured at 50 Ω	*
IF Characteristics								
D.1	IF buffer amplifier center frequency	f_{IF}		10.7		MHz		
D.2	IF buffer amplifier bandwidth	B_{IF}	600			kHz		
D.3	IF buffer amplifier gain	G_{IF}		7		dB		
D.4	IF buffer amplifier input impedance	Z_{IFin}		330		Ω		*
D.5	IF buffer amplifier output impedance	Z_{IFin}		330		Ω		*
Limiter Characteristics								
E.1	Limiter center frequency	f_{LIM}		10.7		MHz		
E.2	Limiter bandwidth	B_{LIM}	600			kHz		
E.3	Limiter input impedance between LIM-IN+ and LIM-IN-	Z_{LIM}		330		Ω		*
E.4	RSSI dynamic range		65	70		dB	Pin RSSI; true RSSI-Signal	
E.5	RSSI linear dynamic range	DP_{RSSI}		70		dB	t_{amb} = 25 °C; Pin RSSI; nonlinearity of true RSSI-Signal < ±1dB	*
E.6	RSSI temperature drift within linear dynamic range	$DRSSI_{temp}$	-2		2	dB	Pin RSSI; true RSSI-Signal	*
E.7	RSSI error untrimmed	$DRSSI_{untrim}$	-6		6	dB	t_{amb} = 25 °C; Pin RSSI; true RSSI-Signal; 2 mVeff at Pins LIM-IN- vs. LIM-IN+	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
E.8	RSSI error user trimmed via SFRs LIMGAIN and LIMOFFS	$DRSSI_{offtrim}$	-1		1	dB	t_{amb} = 25 °C; Pin RSSI; true RSSI-Signal; 2 mVeff at Pins LIM-IN- vs. LIM-IN+	*
E.9	RSSI slope untrimmed	$dU_{RSSI}/dP_{i\ untrim}$	11	14.5	18	mV/dB	t_{amb} = 25 °C; Pin RSSI; 2 mVeff at Pins LIM-IN- vs. LIM-IN+	
E.10	RSSI slope user trimmed via SFRs LIMGAIN and LIMOFFS	$dU_{RSSI}/dP_{i\ trim}$	13.5	14.5	15.5	mV/dB	t_{amb} = 25 °C; Pin RSSI; 2 mVeff at Pins LIM-IN- vs. LIM-IN+	*
E.11	Resistive load at pin RSSI	$R_{L,RSSImax}$	100			kΩ		*
E.12	Capacitive load at pin RSSI	$C_{L,RSSI}$			20	pF		*
Crystal Oscillator Characteristics								
F.1	**TDA5230** Crystal frequency	f_{XTAL}	13.1		13.75	MHz		
F.1E	**TDA5231** Crystal frequency	f_{XTAL31}	14.65		15.5	MHz		
F.2	Shunt capacitance	C_0		2		pF		*
F.3	Motional capacitance	C_1	3	6	10	fF		*
F.4	Load capacitance	C_L		12		pF		*
F.5	Trimming range of frequency	Df_{Trim}	-50		50	ppm		
F.6	Trimming steps	Df_{Trim_step}			4	ppm		*
F.7	Oscillator untrimmed tolerance, not incl. crystal tolerance		-25		30	ppm	trim capacitor default settings, usage of recommended crystal	*
F.8	Crystal oscillator settling time (switching from low power to high precision mode)	$t_{COSCsettle}$	110	note 1	110	$64*T_{sys}$		*
F.9	Clock output frequency at pin CLKOUT/RXD	f_{clock_out}			0.5	f_{sys}	10 pF load	
Digital Inputs/Outputs								

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	*
			min.	typ.	max.			
G.1	High level input voltage	V_{IH}	0.7• VDDD		VDD5V +0.1	V		
G.2	Low level input voltage (except pin P_ON)	V_{IL}	0		0.8	V		
G.3	Low level input voltage at pin P_ON	V_{IL,P_ON}	0		0.5	V		
G.4	High level input leakage current	I_{LIH}			5	µA		
G.5	Low level input leakage current	I_{LIL}	-5			µA		
G.6	High level output voltage (IOH=-500 µA)	V_{OH}	VDDD-0.4V		VDDD	V		
G.7	Low level output voltage (IOL=500 µA)	V_{OL}	0		0.4	V		
Timing SPI-Bus								
G.1E	Clock Frequency	f_C			1.2	MHz		
G.2E	Clock High Time	t_{CH}	400			ns		*
G.3E	Clock Low Time	t_{CL}	400			ns		*
G.4E	Active Setup Time	t_{SSu}	400			ns		*
G.5E	Not Active Hold Time	t_{CS}	400			ns		*
G.6E	Active Hold Time	t_{SHo}	400			ns		*
G.7E	Not Active Setup Time	t_{NSC}	400			ns		*
G.8	Deselect Time	t_{DS}	1			us		*
G.9	SDI Setup Time	t_{SDISu}	100			ns		*
G.10	SDI Hold Time	t_{SDIHo}	170			ns		*
G.11	Clock Low To SDO Valid @ 80 pF load	t_{CDOV}			350	ns		*
G.12	Clock Low To SDO Valid @ 10 pF load	t_{CDOV}			270	ns		
G.13	SDO Rise Time @ 80 pF load	t_{SDOri}			80	ns		*
G.14	SDO Fall Time @ 80 pF load	t_{SDOfa}			80	ns		*
G.15	SDO Rise Time @ 10 pF load	t_{SDOri}			10	ns		*
G.16	SDO Fall Time @ 10 pF load	t_{SDOfa}			10	ns		*
G.17	SDO Disable Time	t_{NSDOZ}			270	ns		*

* not subject to production test - verified by characterization/design

Note 1: Timings are generated by finite state machine and are therefore exact values. Absolute timing tolerances are only influenced by oscillator tolerance.

Note 2: $T_{sys} = 1 / f_{sys} = 1 / f_{XTAL}$

Note 3: If EOM Interrupt is used in combination with FIFO Lock in Run Mode Slave, the Interrupt line is not reset till FIFO is read. See also **Chapter 2.4.15** and **Chapter 2.4.17**.

Note 4: $T_{MasterPeriod}$ limitation is only valid for TDA523x C1 and C2. Mask steps C3 and C4 and higher have no limitation. The mask step is visible on the component stamping.

Unless explicitly otherwise noted, the following test conditions apply to the given specification values in Tables 7..12:

TDA5230:
* Hardware: Testboard TDA523x V2.1
* Single-Ended Matching for 433.92 MHz
* Receive Frequency 433.92 MHz; Lo-Side LO-Injection
* Reference-Clock: XTAL=13.225625 MHz; RF-PLL: R=2, S=0

TDA5231:
* Hardware: Testboard TDA523x V2.1
* Single-Ended Matching for 315.00 MHz
* Receive Frequency 315.00MHz; Hi-Side LO-Injection
* Reference-Clock: XTAL=15.2671875 MHz; RF-PLL: R=2, S=0

TDA5230 and TDA5231:
* IF-Gain: Attenuation set to minimum
* IF-Filter: Center=10.7MHz; BW=280kHz; Connected between IF-OUT and LIM-IN+
* Received-Signal at zero Offset to IF Center Frequency
* RSSI trimmed
* FSK-Demodulator Pre-filter BW +/-250
* No SPI-traffic during telegram reception, CLKOUT disabled
* Specification values are in respect to Manchester-coded Reference Protocol
  (11 Bits '0' ,1 Bit '1' , PRBS5 (31 Bit), 1 Bit 'M') according to **Figure 37**

* DRE ... Data-Rate Error of received telegram vs. adjusted Data-Rate
* DC ... Duty-Cycle
  (duration of first chip of manchester-coded bit in respect to duration of complete bit according to **Figure 37**)
* MER ... Message Error Rate
  [MER = 1 - (number_of_correctly_received_messages / number_of_transmitted messages)]
* FAR ... False Alarm Rate
  [FAR = number_of_mistakenly_wake_ups / number_of_periods_searching_for_data_on_channel]
* MMR ... Missed Message Rate
  [MMR = number_of_mistakenly_missed_wake_up_patterns /
  number_of_periods_with_wake_up_pattern_transmitted_and_searching_for_wake_up_pattern]

Table 7 Characteristics of Digital Data Filter and Data Clock Recovery

The following Specification values are evaluated with ASK 2kBit, ASK 9.6 kBit, FSK 9.6 kBit & D ±35 kHz.
Acceptance Criteria is: MER < 10 %

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
H.1	Data-Rate of received Telegram (nominal)	b	0.5		20	kbit/s		*
H.2	Data-Rate Error of received Telegram (Adjusted Data-Rate vs. Data-Rate of received Telegram)							*
	Sensitivity Loss < 1 dB	Db	-10		10	%	DRE -10% & DC 50% DRE 0% & DC 50% DRE +10% & DC 50%	
H.3	Duty-Cycle Error of manchester coding of received Telegram (Value describes duration of first chip in respect to bit duration)							*
	Sensitivity Loss < 1 dB	tolManchester1	45		55	%	DRE -10% & DC 45% DRE -10% & DC 55% DRE 0% & DC 45% DRE 0% & DC 55% DRE +10% & DC 45% DRE +10% & DC 55%	
	Sensitivity Loss < 3 dB	tolManchester2	35		65	%	DRE -10% & DC 35% DRE -10% & DC 65% DRE 0% & DC 35% DRE 0% & DC 65% DRE +10% & DC 35% DRE +10% & DC 65%	

Table 8 Characteristics of Digital FSK-Demodulator

The following Specification values are evaluated with FSK 9.6kBit & D ±35 kHz .

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
I.1	FSK demodulator center frequency (nominal)	$f_{FSKcenter}$		10.7		MHz		*
I.2	FSK demodulator input range (Offset from nominal IF center frequency, where Signal-Power at output of Matched Data Filter (average of 500 readouts of value in register ASKNP) does not decrease by more than 3dB from Signal-Power at IF center frequency)	$D_{fFSKspan}$	-100		100	kHz	DRE 0% & DC 50% 10 mVeff at Pins LIM-IN- vs. LIM-IN+	*

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
I.3	FSK demodulator input bandwidth (Offset from nominal IF center frequency where sensitivity is not lower than 3dB compared to sensitivity at center frequency)	$D_{fFSKspan}$	-90		90	kHz	DRE 0% & DC 50% RF signal supplied at Pins LIM-IN- vs. LIM-IN+ to avoid influence of IF Filter	*
I.4	Maximum recommended FSK Deviation	f_{FSK-D}			+/-150	kHz	valid for all data rates	*

Table 9 Sensitivity of Receiver

The following Specification values are evaluated for the data-rates given below.
Acceptance criteria is: MER < 10 %

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
J.1	Sensitivity Limit ASK-Mode						DRE 0% & DC 50%	*
	Data Rate 0.5 kbit/s	SASK1		-111	-106	dBm peak		
	Data Rate 2 kbit/s	SASK2		-108	-103	dBm peak		
	Data Rate 9.6 kbit/s	SASK3		-104	-99	dBm peak		
	Data Rate 20 kbit/s	SASK4		-102	-97	dBm peak		
J.2	Sensitivity Limit FSK-Mode						DRE 0% & DC 50%	*
	Data Rate 0.5 kbit/s, deviation D ±1.25 kHz	SFSK1		-102	-97	dBm		
	Data Rate 2 kbit/s, deviation D ±10 kHz	SFSK2		-103	-98	dBm		
	Data Rate 2 kbit/s, deviation D ±35 kHz	SFSK3		-108	-103	dBm		
	Data Rate 9.6 kbit/s, deviation D ±35 kHz	SFSK4		-104	-99	dBm		
	Data Rate 20 kbit/s, deviation D ±50 kHz	SFSK5		-103	-98	dBm		

Table 10 Dynamic Range of Receiver

The following Specification values are evaluated for the data-rates given below.
Acceptance criteria are: MER < 1E-3, FAR < 1E-5, MMR < 1E-4 (Criteria 8 Equal Bits)

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
K.1	Dynamic Range ASK, Modulation Index 100%						DRE 0% & DC 50%	*
	Data Rate 2 kBit/s	DR2,ASK100	-10		-98	dBm peak		
	Data Rate 9.6 kBit/s	DR96,ASK100	-10		-95	dBm peak		
K.2	Dynamic Range ASK, Modulation Index 50%						DRE 0% & DC 50%	*
	Data Rate 2 kBit/s	DR2,ASK50	-45		-92	dBm peak		
	Data Rate 9.6 kBit/s	DR96,ASK50	-60		-89	dBm peak		
K.3	Dynamic Range FSK 9.6 kBit & D ±35 kHz						DRE 0% & DC 50%	*
	0% AM-Modulation	DR96,AM0	-10		-96	dBm		
	90% AM-Modulation, 100 Hz	DR96,AM90	-10		-80	dBm		

Table 11 ASK Sensitivity of Receiver in other Frequency Bands

The following Specification values are evaluated for FSK 2kbit. Acceptance Criteria is: MER < 10 %

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
L.1	Sensitivity Limit **TDA5230** 868.3 MHz, Matching to 868.3 MHz, XTAL=13.4 MHz	S868ASK		-108	-103	dBm peak	DRE 0% & DC 50%	*

* not subject to production test - verified by characterization/design

Table 12 FSK Sensitivity of Receiver in other Frequency Bands

#	Parameter	Symbol	Limit Values			Unit	Test Case	*
			min.	typ.	max.			
M.1	Sensitivity Limit FSK-Mode 868.3 MHz, Matching to 868.3 MHz, XTAL=13.4 MHz						DRE 0% & DC 50%	*
	Data Rate 2 kbit/s, deviation D ±10 kHz	S868FSK1		-100	-95	dBm		
	Data Rate 2 kbit/s, deviation D ±35 kHz	S868FSK2		-108	-103	dBm		
	Data Rate 9.6 kbit/s, deviation D ±35 kHz	S868FSK3		-103.5	-98.5	dBm		
	Data Rate 20 kbit/s, deviation D ±50 kHz	S868FSK4		-102	-97	dBm		

* not subject to production test - verified by characterization/design

4.2 Timing Diagrams

4.2.1 Serial Input Timing

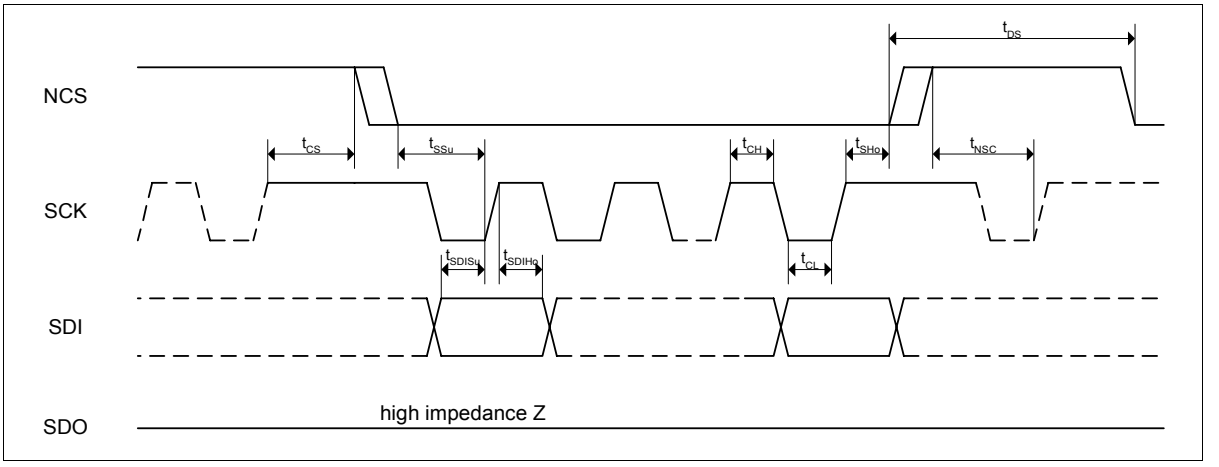

Figure 70 Serial Input Timing

4.2.2 Serial Output Timing

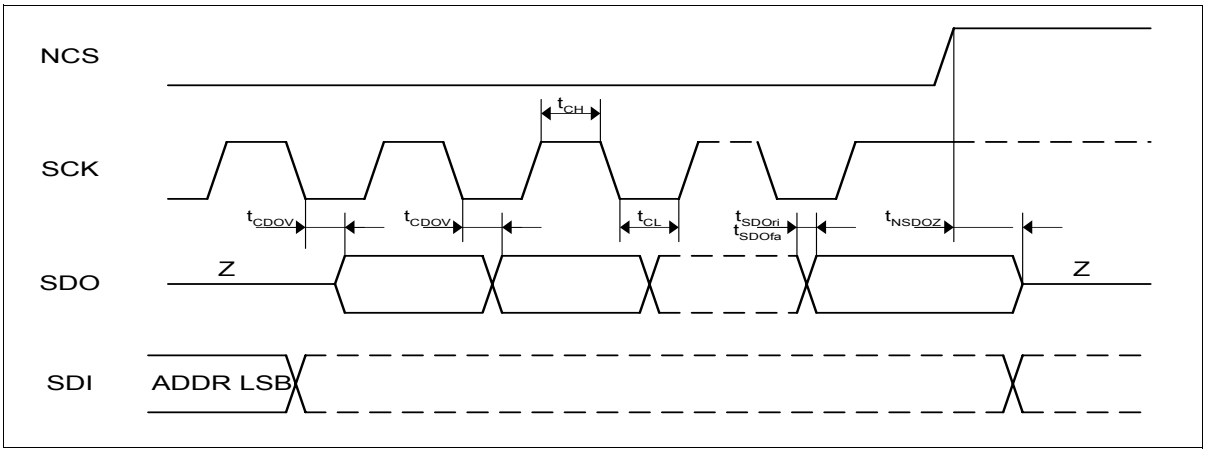

Figure 71 Serial Output Timing

4.3 Test Circuit, Evaluation Board V2.1

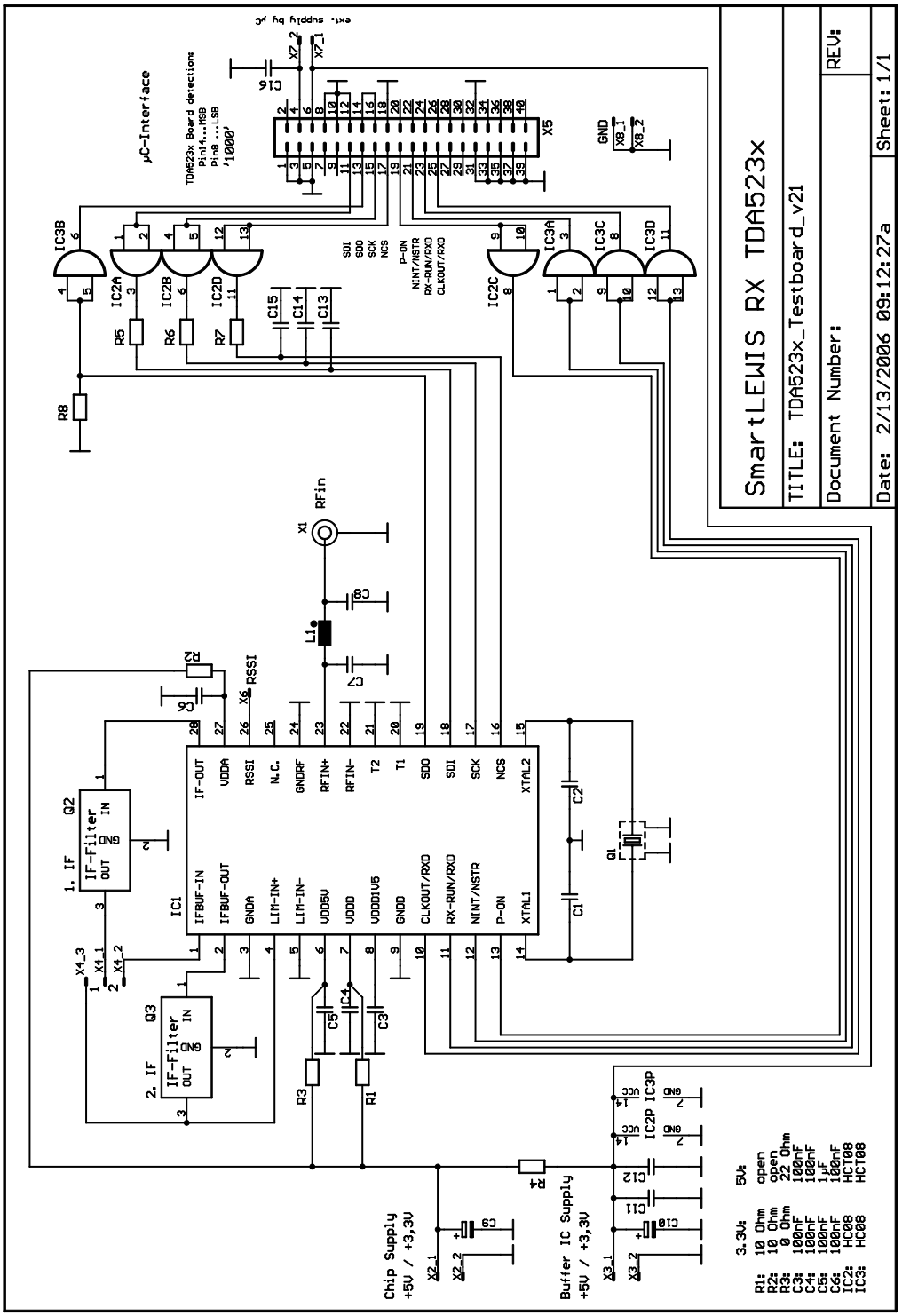

Figure 72 Test Circuit Schematic

4.4 Test Board Layout - Evaluation Board V2.1

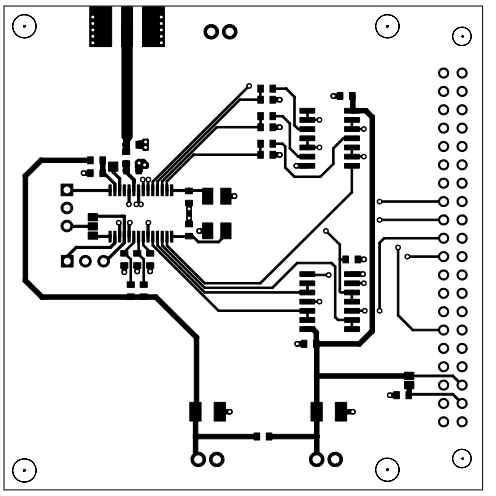

Figure 73 Test Board Layout , Top View

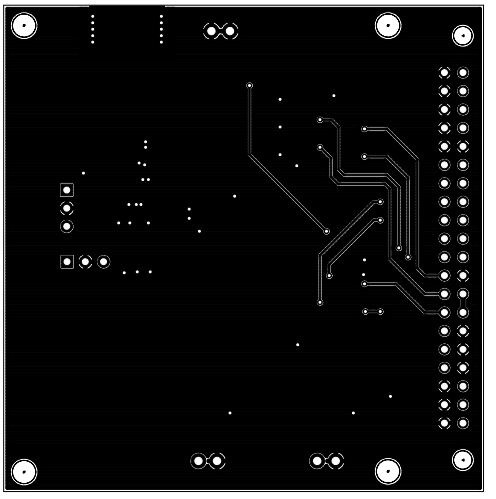

Figure 74 Test Board Layout , Bottom View

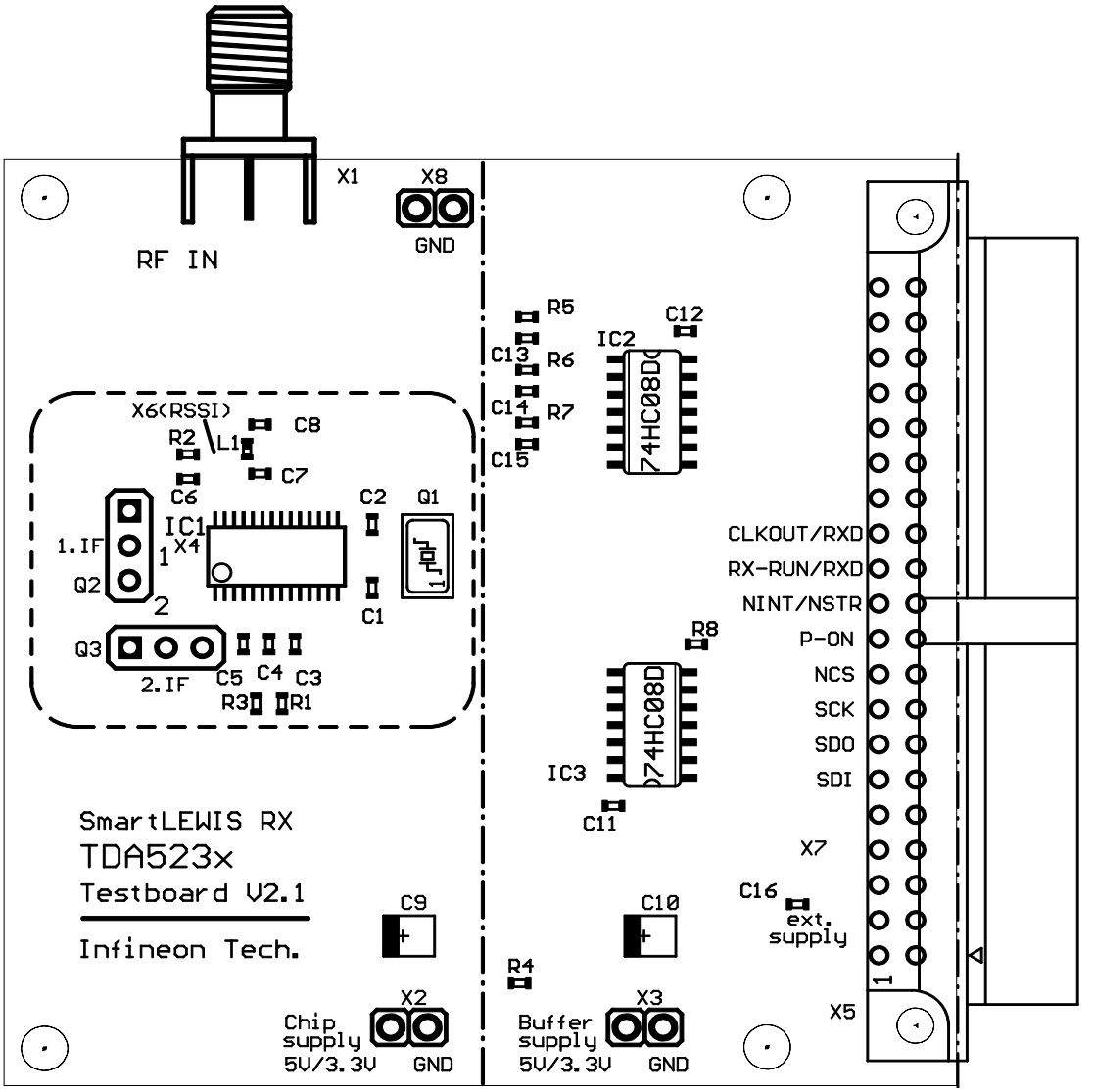

Figure 75 Test Board Layout, Component View

4.5 Bill of Materials

Pos.	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark
1	IC1	**TDA5230/ TDA5231**	PG-TSSOP-28	SMD		Infineon	
2	R1	10 Ohm/ open	0603		+/-5%		3.3 V / 5 V environment
3	R2	10 Ohm/ open	0603		+/-5%		3.3 V / 5 V environment
4	R3	0 Ohm/ 22 Ohm	0603		+/-5%		3.3 V / 5 V environment
5	C1	3.9 pF	0603	C0G	+/-0.1 pF		crystal oscillator load
6	C2	3.9 pF	0603	C0G	+/-0.1 pF		crystal oscillator load
7	C3	100 nF	0603	X7R	+/-10%		
8	C4	100 nF	0603	X7R	+/-10%		
9	C5	100 nF / 1 µF	0603	X7R / X5R	+/-10%		3.3 V / 5 V environment
10	C6	100 nF	0603	X7R	+/-10%		
11	C7	1.8 pF	0603	C0G	+/-0.1 pF		Matching for 315 MHz
		1.2 pF	0603	C0G	+/-0.1 pF		Matching for 434 MHz
		open	0603	C0G	+/-0.1 pF		Matching for 868 MHz
12	C8	open	0603	C0G	+/-0.1 pF		Matching for 315 MHz
		open	0603	C0G	+/-0.1 pF		Matching for 434 MHz
		1.5 pF	0603	C0G	+/-0.1 pF		Matching for 868 MHz
13	C9	10 µF	293B	Tantal	+/-10%		
14	L1	68 nH	0603	Simid0603-C	+/-2%	EPCOS	Matching for 315 MHz
		47 nH	0603	Simid0603-C	+/-2%	EPCOS	Matching for 434 MHz
		27 nH	0603	Simid0603-C	+/-2%	EPCOS	Matching for 868 MHz
15	Q1	15.2671875 MHz	NX5032SD	C0= 1.3 pF C1= 5.0 fF	CL=12 pF	NDK, (Frischer Electronic), EXS00A-03513	SMD-crystal for 315.0 MHz (Hi-Side LO Injection)
		13.225625 MHz	NX5032SD	C0= 1.3 pF C1= 4.8 fF	CL=12 pF	NDK, Frischer Electronic, EXS00A-3512	SMD-crystal for 433.92 MHz (Lo-Side LO Injection)
		13.4 MHz	NX5032SD	C0= 1.3 pF C1= 3.7 fF	CL=12 pF	NDK, Frischer Electronic, EXS00A-3514	SMD-crystal for 868.3 MHz (Lo-Side LO Injection)
16	Q2	10.7 MHz (BW=280 kHz)		SFELF10M7F A00-B0		Murata	1. IF Filter

Pos.	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark
Interface / optional							
17	IC2	74HC08 / 74HCT08	SO14	SMD			AND gates (3.3 V / 5 V environment)
18	IC3	74HC08 / 74HCT08	SO14	SMD			AND gates (3.3 V / 5 V environment)
19	R4	0 Ohm	0603		+/-5%		common supply for TDA523x and buffer ICs
20	R5	100 Ohm	0603		+/-5%		
21	R6	100 Ohm	0603		+/-5%		
22	R7	100 Ohm	0603		+/-5%		
23	R8	10 kOhm	0603		+/-5%		
24	C10	10 µF	293B	Tantal	+/-10%		
25	C11	100 nF	0603	X7R	+/-10%		
26	C12	100 nF	0603	X7R	+/-10%		
27	C13	10 pF	0603	X7R	+/-10%		
28	C14	10 pF	0603	X7R	+/-10%		
29	C15	10 pF	0603	X7R	+/-10%		
30	C16	100 nF	0603	X7R	+/-10%		
31	Q3	10.7 MHz (BW=280 kHz)		SFELF10M7FA00-B0		Murata	2. IF-Filter, optional
32	X1	SMA socket		PCB mounting			RF input
33	X2	2 pins					chip supply
34	X3	2 pins					buffer supply
35	X4	3 pins	soldering jumper				IF filter selection (default: connect 1 filter)
36	X5	2x20 pins	female connector coded				Connection to PC / µC / Interface
37	X6	1 pin	measurement point				RSSI
38	X7	2 pins	soldering jumper				select external supply by µC(default: closed)
39	X8	2 pins					GND
40	Board material 0.8mm FR4 with 35 µm copper on both sides						

5 Package Outlines

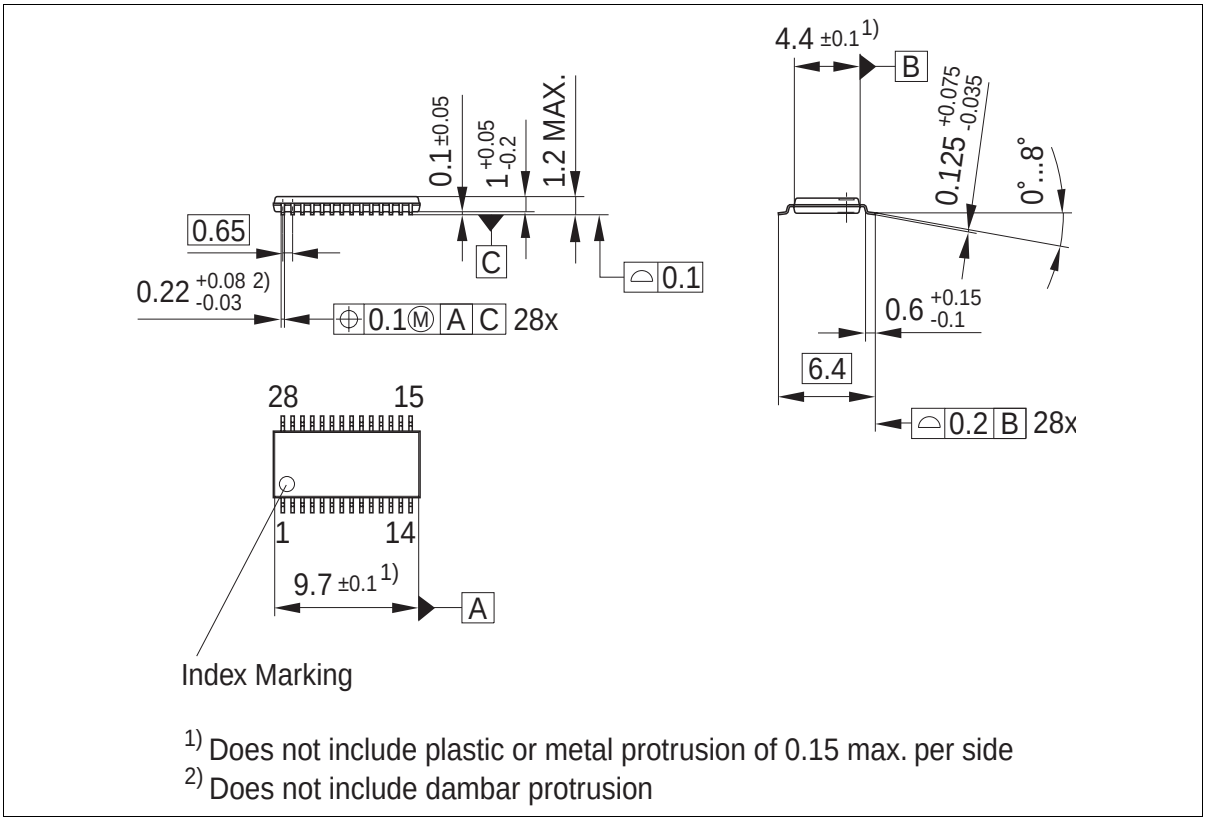

Figure 76 PG-TSSOP-28-1 Package Outlines

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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