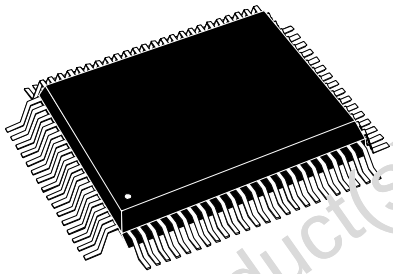
STV2050A

AUTOMATIC MULTISCAN DIGITAL CONVERGENCE PROCESSOR

- Multiscan 1H, 2H, HDTV and SVGA applications
- 6 Convergence channels
- 14-bit embedded DACs
- 1 Focus channel
- Second order interpolation in vertical direction
- Digital filtering in horizontal direction
- On-chip PLL
- On-chip video pattern generator
- Automatic compensation of temperature drift and aging of external components
- Pattern and synchronisation signals for optional optical sensor support
- Adjustable horizontal and vertical size
- Up to 7 different data sets
- Self-controlled power-on sequence



Package: PQFP80
Power Supply: 3.3 V
Tape and Reel: STV2050ATR

Figure 1. Functional Block Diagram

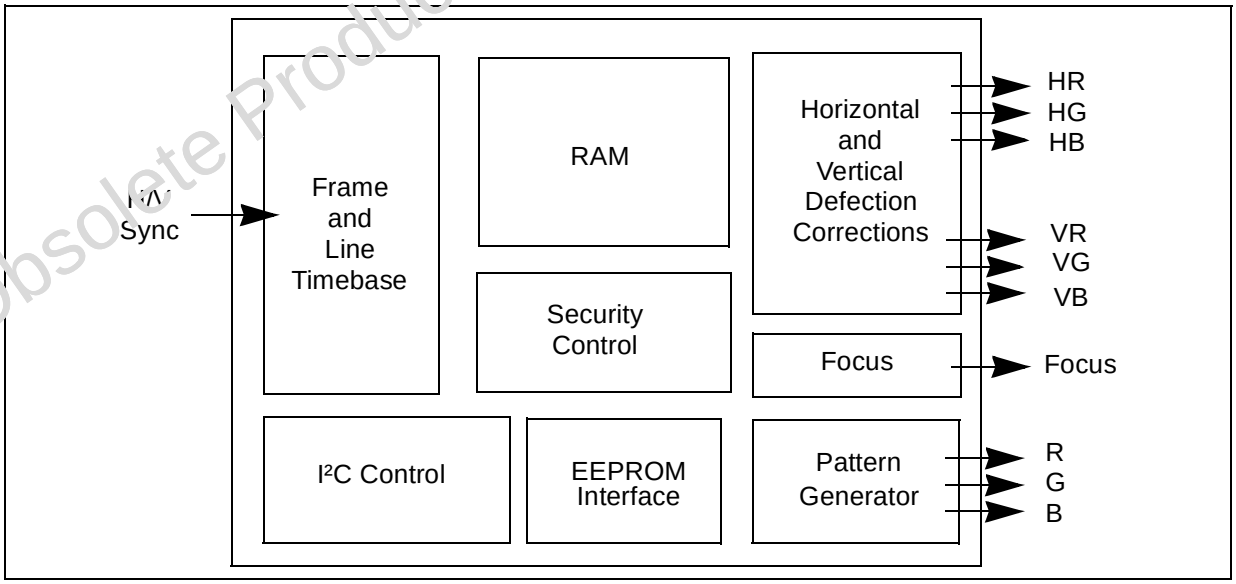


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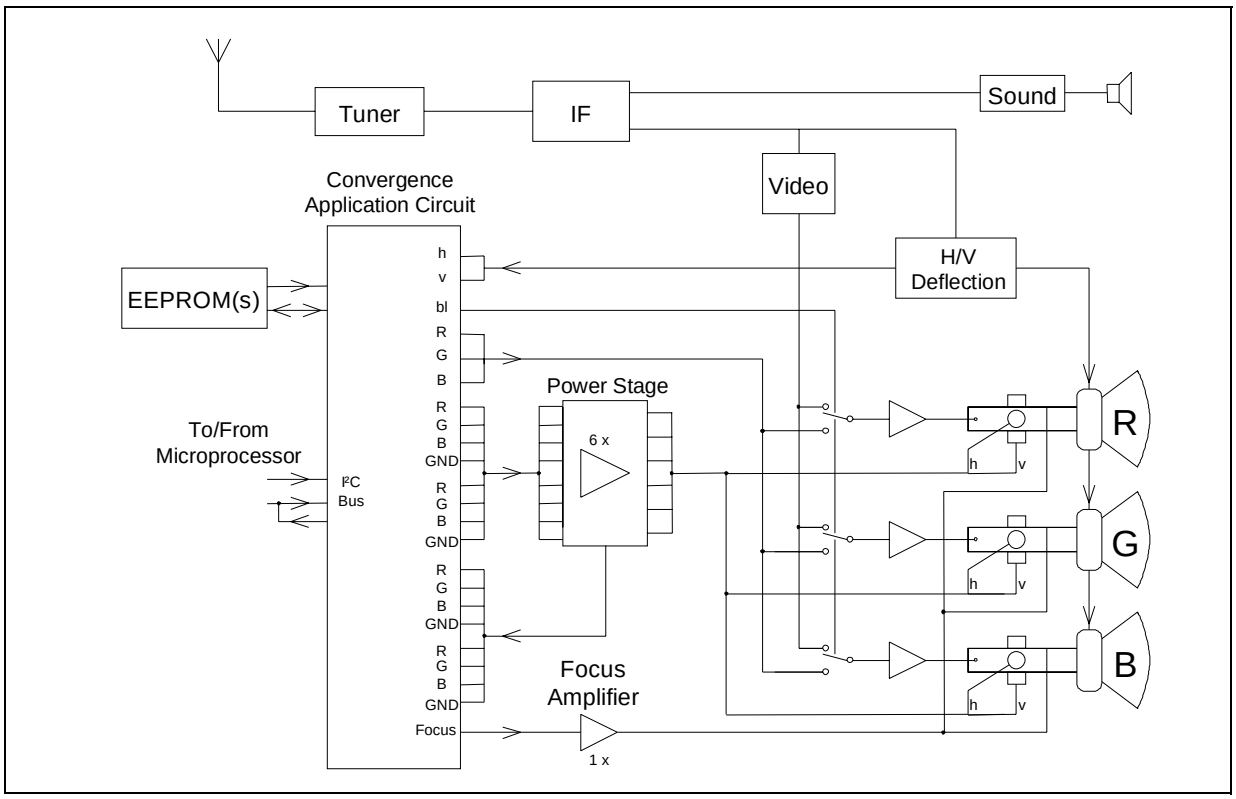
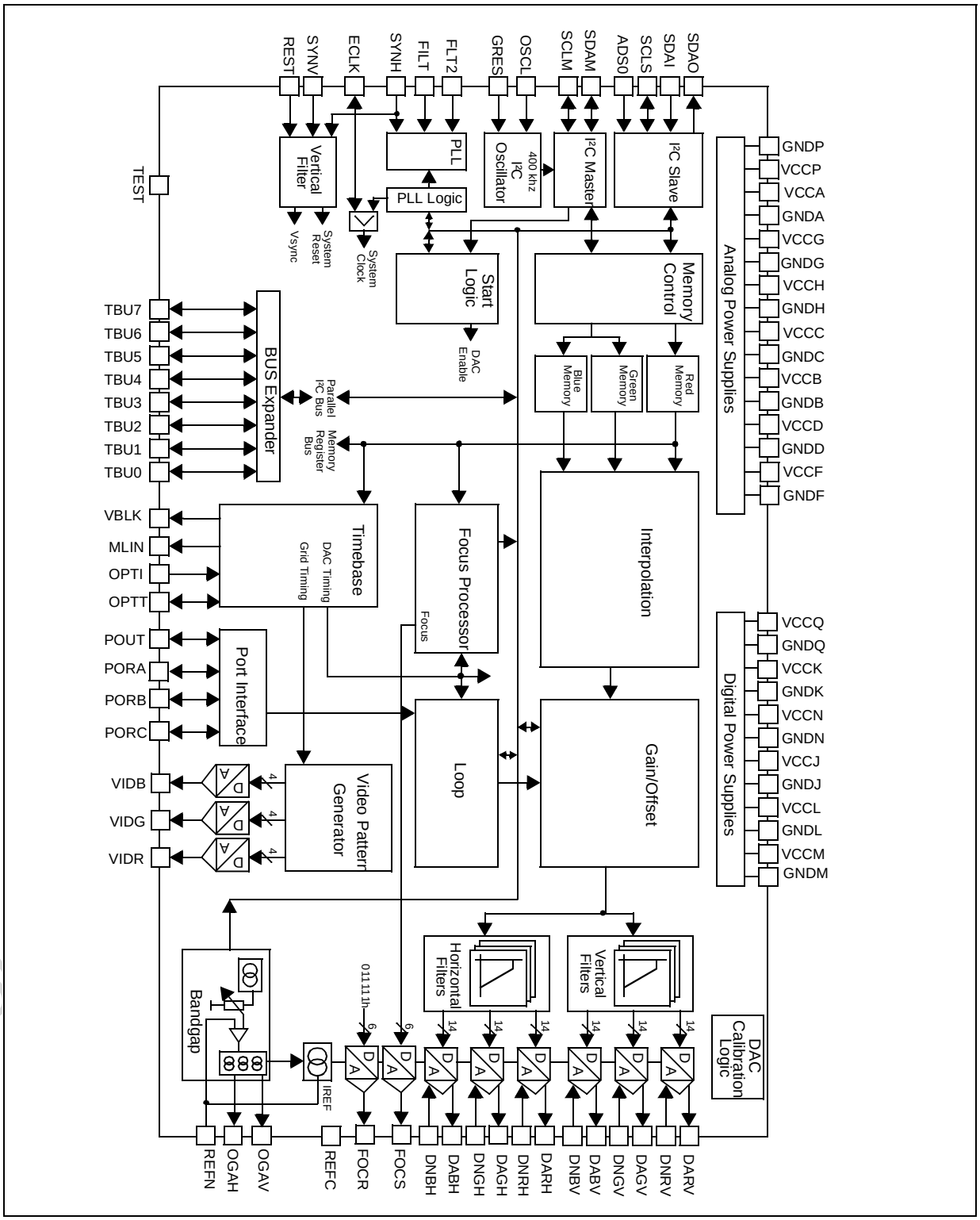
Figure 2. TV Set Convergence System Diagram



1.2 DEVICE BLOCK DIAGRAM

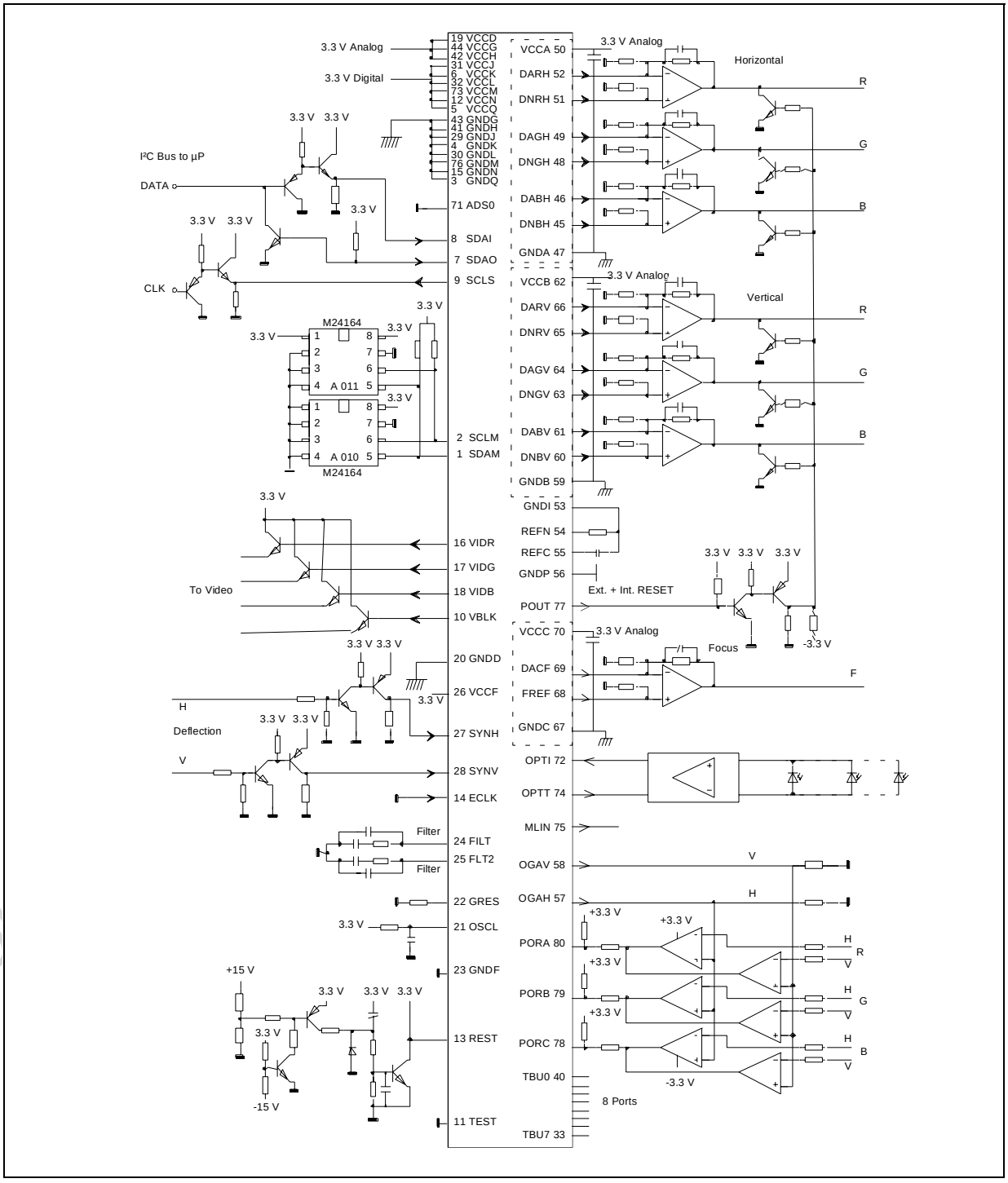
Figure 3. STV2050A Block Diagram



1.3 APPLICATION CIRCUIT

An application circuit with 2nd EEPROM, Electrical Offset and Gain Adjustment Loop and Optical Sensors is shown in the following figure.

Figure 4. Application Circuit



1.4 PIN DESCRIPTION AND PINOUT DIAGRAM

The following legend applies to the Pin Description Table below:

X = Undefined HZ = High Impedance

"0" = Low Level Output "1" = High Level Output

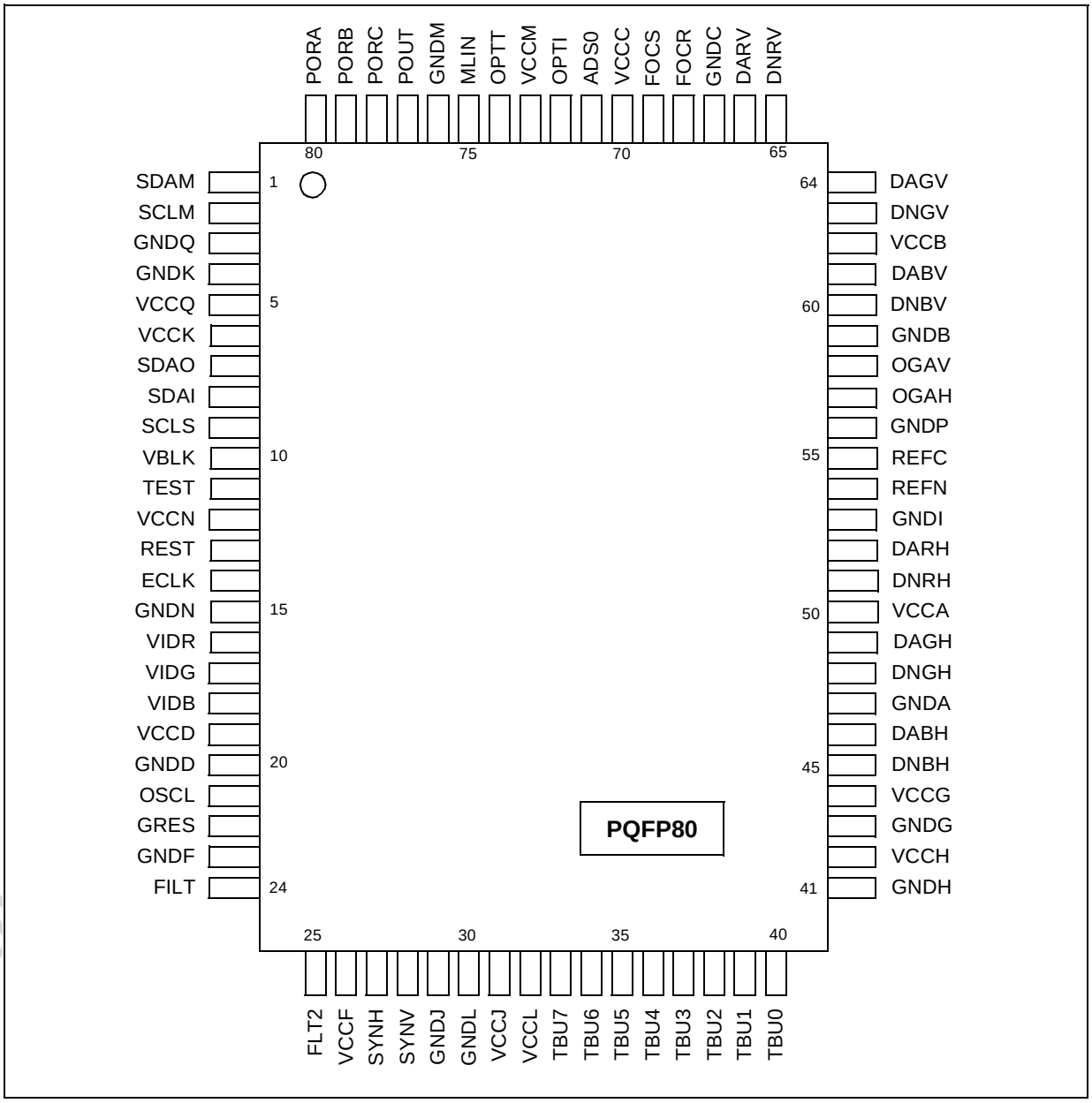
Table 1. Pin Description

Pin No.	Pin Name	Reset Status and Remarks	Description
1	SDAM	HZ	Master Bus: "Data"
2	SCLM		Master Bus: "Clock"
3	GNDQ		Digital Supply: Ground
4	GNDK		Digital Supply: Ground
5	VCCQ		Core / RAM Digital Supply: 3.3 V
6	VCCK		Core / Digital Supply: 3.3 V
7	SDAO	"0"	Slave Bus: "Data" output
8	SDAI		Slave Bus: "Data" input
9	SCLS		Slave Bus: "Clock"
10	VBLK		Video Pattern Blanking
11	TEST	Must be grounded	Reserved
12	VCCN		Shield Supply Digital Supply: 3.3 V
13	REST	"0"	Reset
14	ECLK	Must be grounded	Reserved
15	GNDN		Digital Supply: "Ground"
16	VIDR	0 Volts	Video Pattern Output: "Red"
17	VIDG	0 Volts	Video Pattern Output: "Green"
18	VIDB	0 Volts	Video Pattern Output: "Blue"
19	VCCD		Video Generator Supply: 3.3 V
20	GNDD		Video Generator Supply: Ground
21	OSCL	HZ	RC for internal oscillator
22	GRES	HZ	R for internal oscillator
23	GNDF		PLL Supply: Ground
24	FILT	HZ	Filter for PLL
25	FLT2	HZ	Filter for PLL
26	VCCF		Supply PLL: 3.3 V
27	SYNH		Horizontal Synchronization input
28	SYNV		Vertical Synchronization input
29	GNDJ		Digital Supply: Ground
30	GNDL		Digital Supply: Ground
31	VCCJ		Core Digital Supply: 3.3 V
32	VCCL		Ring / Buffer Digital Supply: 3.3 V
33	TBU7	X	I²C BUS Expander
34	TBU6	X	I²C BUS Expander
35	TBU5	X	I²C BUS Expander
36	TBU4	X	I²C BUS Expander

Pin No.	Pin Name	Reset Status and Remarks	Description
37	TBU3	X	I²C BUS Expander
38	TBU2	X	I²C BUS Expander
39	TBU1	X	I²C BUS Expander
40	TBU0	X	I²C BUS Expander
41	GNDH		Analog Supply: Ground
42	VCCH		D/A Interface Analog Supply: 3.3 V
43	GNDG		Analog Supply: Ground
44	VCCG		Analog Supply: 3.3 V
45	DNBH	HZ	Horiz. Convergence Output: Blue, negative
46	DABH	HZ	Horiz. Convergence Output: Blue, positive
47	GNDA		Horiz. Convergence Output Supply: Ground
48	DNGH	HZ	Horiz. Convergence Output: Green, negative
49	DAGH	HZ	Horiz. Convergence Output: Green, positive
50	VCCA	HZ	Horiz. Convergence Output Supply: 3.3 V
51	DNRH	HZ	Horiz. Convergence Output: Red, negative
52	DARH	HZ	Horiz. Convergence Output: Red, positive
53	GNDI		Floating GND for bandgap filter
54	REFN	Reference Current Code 0(hex)	I_{REF} Loop for H&V Convergence & Focus
55	REFC	X	Filter pin for I_{REF} current
56	GNDP		I_{REF} GND for Bandgap
57	OGAH	HZ	Horiz. Reference output for electrical loop
58	OGAV	HZ	Vert. Reference output for electrical loop
59	GNDB	HZ	Vert. Convergence Output Supply: Ground
60	DNBV	HZ	Vert. Convergence Output: Blue, negative
61	DABV	HZ	Vert. Convergence Output: Blue, positive
62	VCCB		Vert. Convergence Output Supply: 3.3 V
63	DNGV	HZ	Vert. Convergence Output: Green, negative
64	DAGV	HZ	Vert. Convergence Output: Green, positive
65	DNRV	HZ	Vert. Convergence Output: Red, negative
66	DARV	HZ	Vert. Convergence Output: Red, positive
67	GNDC		Focus Supply: Ground
68	FOCR		Focus Reference Output
69	FOCS		Focus Signal Output
70	VCCC		Focus Supply
71	ADS0		I²C Slave Bus Address Selection
72	OPTI		Input for optical sensor support
73	VCCM		Ring / Inputs Digital Supply: 3.3 V
74	OPTT	Input	I pin: Latched at measuring line or with sys. clock; O pin: Push/pull, output can be switched to high impedance
75	MLIN	"0"	Measuring Line Signal Output
76	GNDM		Digital Supply: Ground

Pin No.	Pin Name	Reset Status and Remarks	Description
77	POUT	HZ	Protection Pin Control
78	PORC	Input	Normally used for electrical loop feedback detection. Can also be set as an inpout or an output.
79	PORB		
80	PORA		

Figure 5. Pinout Diagram



2 STRUCTURE OF THE PROGRAMMING SYSTEM

2.1 DATA STORAGE

The STV2050A is a programmable device. Some of the data, mainly the convergence parameters, must be able to be easily changed during TV set alignment or by the user, and must be memorized when the TV set is switched off in order to be recovered when switched back on. This data must therefore be stored in EEPROM.

The STV2050A has an **embedded RAM** for storing data used “in real time” at a high speed.

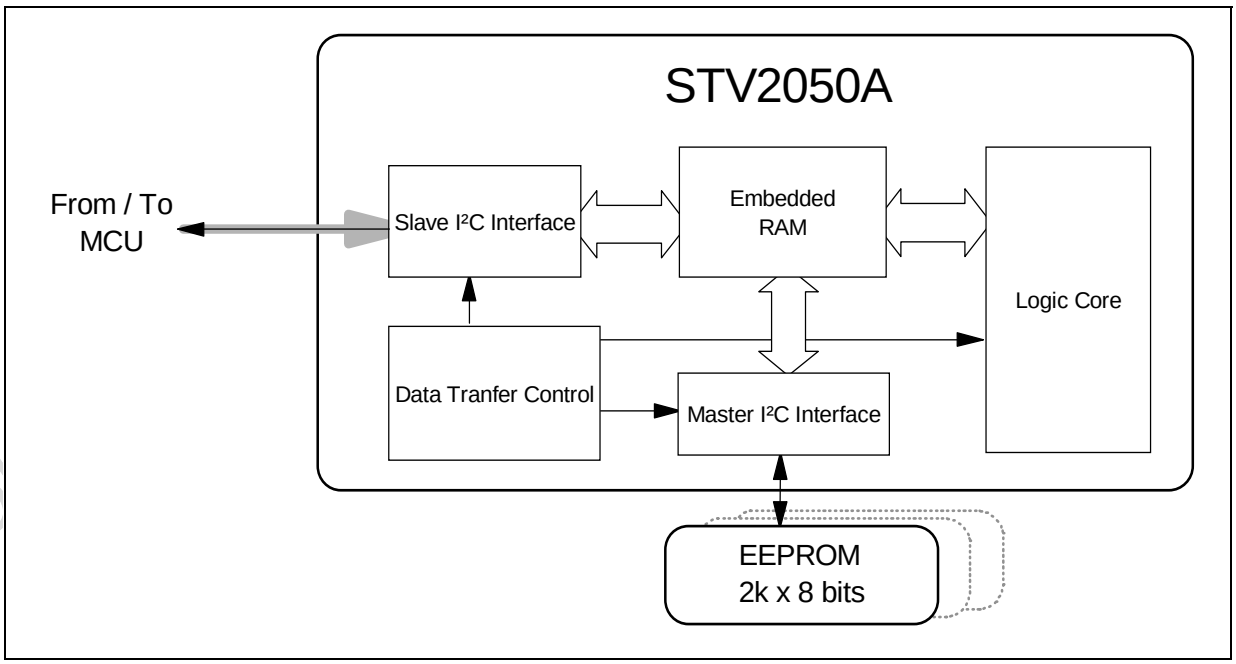
In order to simplify the microcontroller software, and to ensure a quick startup, the STV2050A directly controls one or more (or up to seven) EEPROMs.

The STV2050A has 2 ports for I²C connections:

– The first one is used only for “**SLAVE**” connections: it is used to interface with a microcontroller in order to control the IC (customer adjustments,...). The microcontroller can write and read the embedded RAM via this slave port.

– The second one is used only for “**MASTER**” connections: it is used to interface the STV2050A with the EEPROM that stores the convergence data and some user adjustments. The transfer of data between the EEPROM and the embedded RAM is fully managed by the STV2050A.

Figure 6. I²C BUS Data Transfer



2.2 OVERVIEW OF EMBEDDED RAM ORGANIZATION

The RAM consists of 3 banks:

The first one, the “Red and I²C Bank”, uses 24-bit words. The two other banks, the “Green Bank” and “Blue Bank”, both use 22-bit words. Each bank has 208 words with addresses from 00(hex) to CF(hex).

These 3 x 208 words are allocated to the “dynamic” convergence parameters. (Refer to Section 4.1 "CONVERGENCE CORRECTION VALUES" on page 18.)

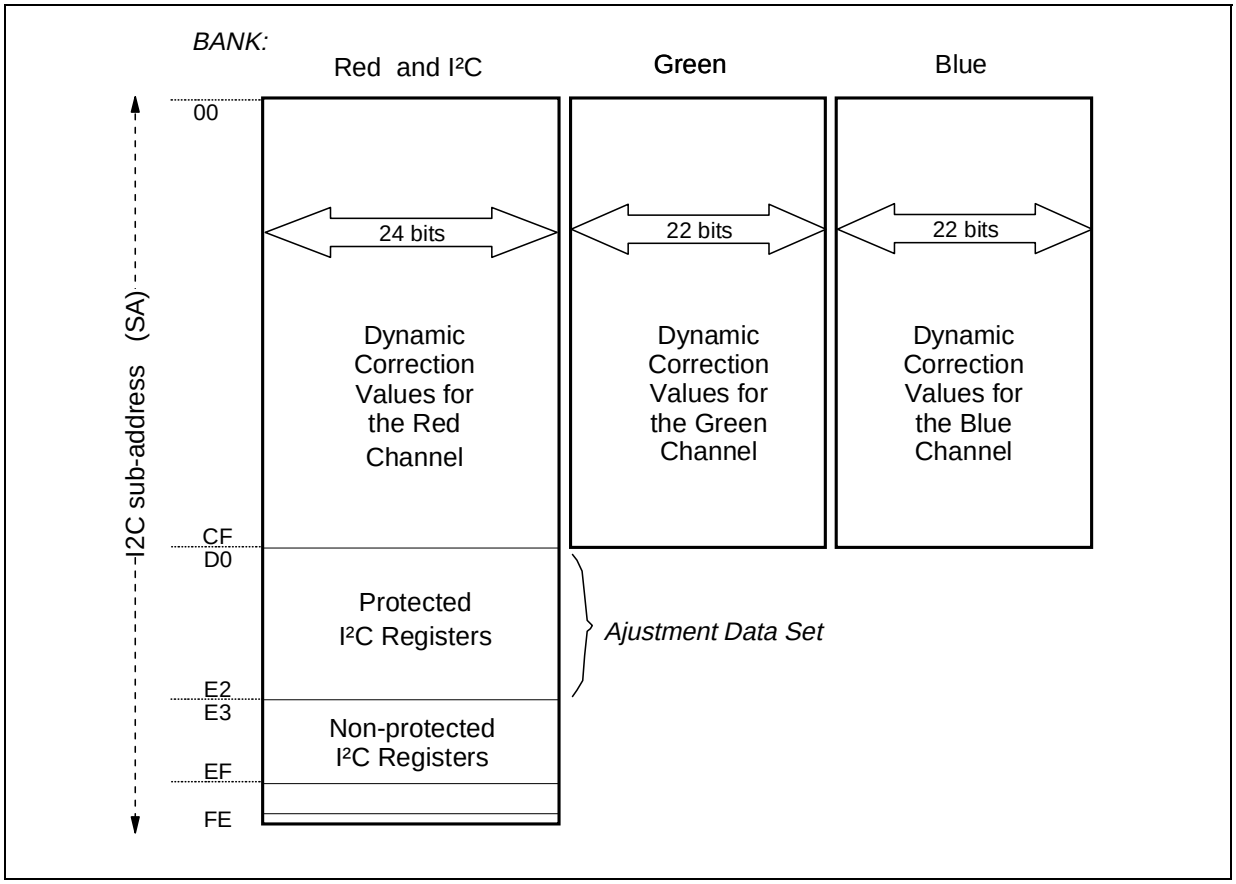
The “Red and I²C Bank” has 33 additional words: addresses from D0(hex) to EF(hex) and FE(hex). These words are used to buffer the I²C Bus registers.

As shown in this figure, each word can be pointed to by a sub-address (SA). Thus, each sub-address points to 24- (or 22-, depending on the bank) bit wide words. A word virtually consists of three bytes (24-bits) named D0, D1 and D2 as shown in the following figure. The bit order is named as follows: D0[7] is the MSB and D2[0] is the LSB

	MSB															LSB								
	D0 Byte								D1 Byte								D2 Byte							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Note: Bit D0[7:6] is not physically implemented in the “Green” and “Blue” banks.

Figure 7. Color Banks



Note: Bits 22 and 23 of the “Red and I²C bank” may be used for general purposes. They are stored together with the convergence data in the external EEPROM.

2.3 ADJUSTMENT DATA SETS

The set of data stored at addresses D0 to E2 is called an ADS (Adjustment Data Set).

The STV2050A can store up to three ADSs in one standard EEPROM. Refer to Section 6 "MASTER I²C BUS INTERFACE" on page 28.

3 SLAVE I²C BUS INTERFACE

3.1 FEATURES

The I²C interface is controlled by 4 pins:

3.1.1 ADS0: IC Address and PLL Mode

The level at this pin corresponds to bit 1 in the first byte in bus transmissions.

– If ADS0 is connected to GND, the analog outputs will be automatically switched on after the reset sequence, and once the internal PLL is activated.

– If the pin is connected to VCC, the DACs will remain in high impedance. The internal PLL is inhibited, and the IC must use an external PLL.

3.1.2 SCLS Bus Clock

The polarity and timing for this pin comply with I²C Bus specifications.

3.1.3 SDAI Bus Data Input

The polarity and timing for this pin comply with I²C Bus specifications.

3.1.4 SDAO Bus Data Output

The polarity reversal and timing for this pin comply with I²C Bus specifications.

Abbreviations used:

S	=	Start condition
P	=	Stop condition
DA	=	Device address
DR	=	Device address for read
DW	=	Device address for write
SA	=	Sub-address
D0, D1,... Dn	=	Data bytes

The slave accepts the following DA subaddresses depending on the hardware configuration defined on pin ADS0.

ADS0	0 (grounded, internal PLL only) DR = 39, DW = 38 1 (3.3 Volt, external PLL only) DR = 3B, DW = 3A

For the 00 to CF address range (RAM), an autoincrement function can be enabled using the AIE (Auto Increment Enable) bit in the E7 register.

AIE	0 = Autoincrement disabled 1 = Autoincrement enabled

If the autoincrement function is enabled, the internal address is automatically incremented after 3 bytes are either written or read. When the autoincrement counter reaches the CF address, the counter stops counting and any additional data will be written to or read from the CF address.

3.2 COLOR BANK SELECTION

As previously mentioned, the embedded RAM is mapped in 3 banks called the “Red and I²C Bank”, “Green Bank” and the “Blue Bank”. A bank is selected using the CBS[1:0] (Color Bank Selection) bits located in the E7 register address.

CBS[1:0]	00 = Red and I²C bank selected 01 = Green bank selected 10 = Blue bank selected 11 = Red and I²C bank selected

However, sub-addresses D0 to EF and FE (physically mapped in the “Red and I²C Bank”) are independent of the actual bank selection.

3.3 WRITE COMMANDS

Three formats of write commands are supported:

– **5-byte write commands to any valid sub-address**

S DW SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at SA+1 after the command, otherwise it is still at SA.

– **2-byte write commands for defining a sub-address cursor position or for changing the current sub-address without transmitting data.**

S DW SA P

The sub-address is at SA after the command.

– **Auto-increment write commands for sub-address range 00 to CF**

If the auto-increment function is enabled, the internal address counter is incremented each time 3 bytes are written:

S DW SA_i D_i0 D_i1 D_i2 $D_{i+1}0$ $D_{i+1}1$ $D_{i+1}2$... Dn P

otherwise every group of 3 bytes is written to SA and the sub-address does not change.

S DW SA_i D_i0 D_i1 D_i2 D_i0 D_i1 D_i2... ... Dn P

When a group of three data bytes within the 00 to E2 address range has been received, the slave will store them in the appropriate embedded RAM location. Only complete groups of three data bytes are stored. I²C registers start to be updated when the first data byte is received. Only complete bytes are written.

All write commands which do not comply with the formats described above are rejected.

3.4 READ COMMANDS

Read commands may access the IC internal RAM as well as all I²C registers. Read commands in the 00 to CF range read from the RAM bank that is defined by the two CBS bits that have been previously transmitted to the E7 register by a write command.

Addresses in the D0 to E2 range are mapped to the corresponding section of the red color RAM if the RRP bit in the EF register is '0'. Otherwise the corresponding internal register values are transmitted.

If the SA is in the 00 to CF address range, the position of the cursor is implicitly defined by the SA. An access to any other SAs will switch off the cursor. It will be switched on again if an address in the 00 to CF range is selected.

Three formats of read commands are supported:

– **Random read commands from any valid IC internal address**

S DW SA S DR SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at the SA+1 after the command, otherwise it is still at the SA.

– **Read commands from the actual internal address**

S DR SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at the SA+1 after the command, otherwise it is still at the SA.

– **Auto-increment read commands from addresses within the 00 to CF address range with random start address.**

S DW SA S DR SA D0 D1 D2..... Dn P

If the auto-increment function is enabled, the internal address counter is incremented after 3 bytes are read, otherwise the SA is always read and the internal address does not change.

When the last byte of the CF address has been transmitted, the IC internal auto-increment address counter stops counting and the CF value will be read out again.

3.5 I²C I/O LINES

Digital filters suppress pulses that are less than 1 or 2 clock pulses at the SDAI and SCLS inputs.

4 RAM ALLOCATION

4.1 CONVERGENCE CORRECTION VALUES

The convergence correction values are either dedicated to each correction point of each red/blue/green channel, or common for all points of each channel. (Refer to Section 9 "CONVERGENCE" on page 45.)

The values are grouped into 2 families:

– Dynamic correction values

– Common correction values

4.1.1 Dynamic Correction Values

The dynamic values are stored as described in Section 2.2 "Overview OF EMBEDDED RAM ORGANIZATION" on page 13.

For each Red, Green and Blue channel, the following can be stored in the embedded RAM:

– 13 horizontal "dynamic" correction values on 10 bits, plus 1 parity bit

– Up to 16 vertical "dynamic" correction values on 10 bits, plus 1 parity bit

For each correction point there is one corresponding word in the 00(hex) to CF(hex) sub-address range. Bits are stored in the corresponding “Red Bank”, “Green Bank” and “Blue Bank” as follows:

	MSB																								LSB
	BYTE D0								**BYTE D1**								**BYTE D2**							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
			Horizontal Correction[9:0]												Vertical Correction[9:0]									

– Bit D1[3] is the horizontal correction parity bit

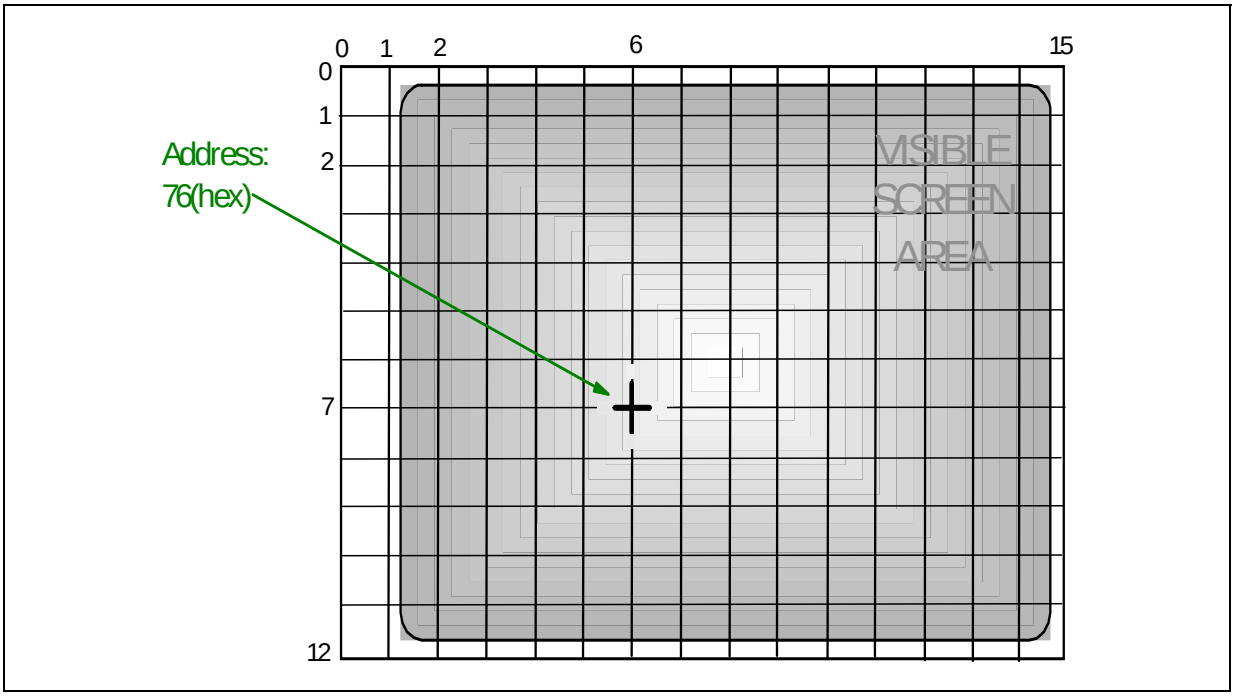
– Bit D1[2] is the vertical correction parity bit

– Bits D1[3:2] are generated by the STV2050A. Their value can be read out only.

Note: The STV2050A automatically checks the parity bits of each convergence value before applying them to the DACs. Refer to Section 14 "SECURITIES" on page 62.

The sub-address corresponds to the coordinates of the point on the screen where the vertical and horizontal lines meet, as shown in the following figure:

Figure 8. Addressing a Correction Point



4.1.2 Common Correction Values

The common correction values are stored in the “adjustment data sets” of the Red and I²C channel. See Figure 7 "Color Banks" on page 14 and Section 9.1 "GLOBAL ADJUSTMENTS - COMMON PARAMETERS" on page 45.

4.2 I²C REGISTERS

All I²C registers are implemented in the “Red and I²C Bank” of the embedded RAM. As it can be useful to store some of the I²C register content in the EEPROM, the embedded RAM allocation is divided into two parts:

– From sub-address D0 to E2 (included), contents can be stored in the EEPROM, and can then be restored,

– From sub-addresses E3 to EF and FE, contents are lost when the STV2050A is switched off.

4.2.1 Registers Storable in the EEPROM

	MSB							LSB																
	BYTE D0								BYTE D1								BYTE D2							
SA	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D0	RFH[7:0]								GFH[7:0]								BFH[7:0]							
D1	RFV[7:0]								GFV[7:0]								BFV[7:0]							
D2	ORH[7:0]								OGH[7:0]								OBH[7:0]							
D3	ORV[7:0]								OGV[7:0]								OBV[7:0]							
D4	x	PDC	PDB	PDA	x	POC	POB	POA	X	PLT	GOS	HVM	GAV[1:0]		GAH[1:0]		X	X	X	X	X	X	X	X
D5	PRS	0	AMS[0		BGA[4:0]				PMH	PMV	X	X	X	X	MLE		MLN[8:0]							
D6	PBH[3:0]				PBV[3:0]				HBE	HAE	HVB[5:0]						VBE	VAE	VVB[5:0]					
D7	x	HGP[6:0]							TVH	TVV	BPH[5:0]						FAS	STA	BPV[5:0]					
D8	ACW	x	HGD[5:0]						ACL[1:0]		HRD[5:0]						AFS[1:0]		ASP[2:0]			FSO	HIF[1:0]	
D9	VGP[7:0]								VGP	VFP	VGD[5:0]						VFP[7:0]							
DA	IIE	IFA	x	ICV[5:0]					VST[7:0]								FSB[7:0]							
DB	DCT[8]	HDP[6:0]							DCT[7:0]								DCB[7:0]							
DC	CRH[7:0]								CGH[7:0]								CBH[7:0]							
DD	CRV[7:0]								CGV[7:0]								CBV[7:0]							
DE	FV1[5:0]								FV2[5:0]								FV3[5:0]							
DF	OLE	GLE	FIN	DIO	DIG	x	x	x	NOM[7:0]								TOL[7:0]							
E0	RCH[3:0]				RCV[3:0]				GCH[3:0]				GCV[3:0]				BCH[3:0]				BCV[3:0]			
E1	SRH[7:0]								SGH[7:0]								SBH[7:0]							
E2	SRV[7:0]								SGV[7:0]								SBV[7:0]							

4.2.2 Registers Not Storable in the EEPROM

	MSB							LSB																
	BYTE D0								**BYTE D1**								**BYTE D2**							
ADD	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
E3	STL	X	X	GCD	DHV	PPL	CDO	CDN	STV2050A code = 30(hex)								S01	S19	RESERVED				S02	S03
E4	X	PDC	PDB	PDA	X	POC	POB	POA	X	PLT	GOS	HVM	GAV [1:0]		GAH [1:0]		S01	S19	MSY	ELO	X	PIC	PIB	PIA
E5	OPI	ODS	OOS	ODT	X	X	X	X	S09 [3:0]				S10 [3:0]				S01	S19	S05	S11	S12 [3:0]			
E6	X	X	X	X	X	X	X	X	S13[7:0]								S14[7:0]							
E7	AIE	X	X	X	X	X	CBS [1:0]		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TE1
E8	MVR[7:0]								MVG[7:0]								MVB[7:0]							
E9	EEPRO-Madd [2:0]			X	X	X	ADS[1:0]		RWM [2:0]			X	HAM[3:0]				S01	S19	X	X	STX[3:0]			
EA	X	X	X	X	VDC	COV[2:0]			GCP	VHV	X	PAS[4:0]					X	X	X	X	X	X	X	X
EB	X	X	HO1 [5:0]						HG1[3:0]				X	X	HO2[5:0]						HG2[3:0]			
EC	X	X	VO1[5:0]						VG1[3:0]				X	X	VO2[5:0]						VG2[3:0]			
ED	X	X	HO3[5:0]						HG3[3:0]				X	X	HO4[5:0]						HG4[3:0]			
EE	X	X	VO3[5:0]						VG3[3:0]				X	X	VO4[5:0]						VG4[3:0]			
EF	X	X	X	X	X	RUE	RU1	RU2	X	X	X	X	TE2	TE3	TE4	RRP	X	X	X	X	X	X	0	0
FE	X	SSE	DTE	0	0	0	0	0	0	0	0	0	0	0	0	0	TBU[7:0]							

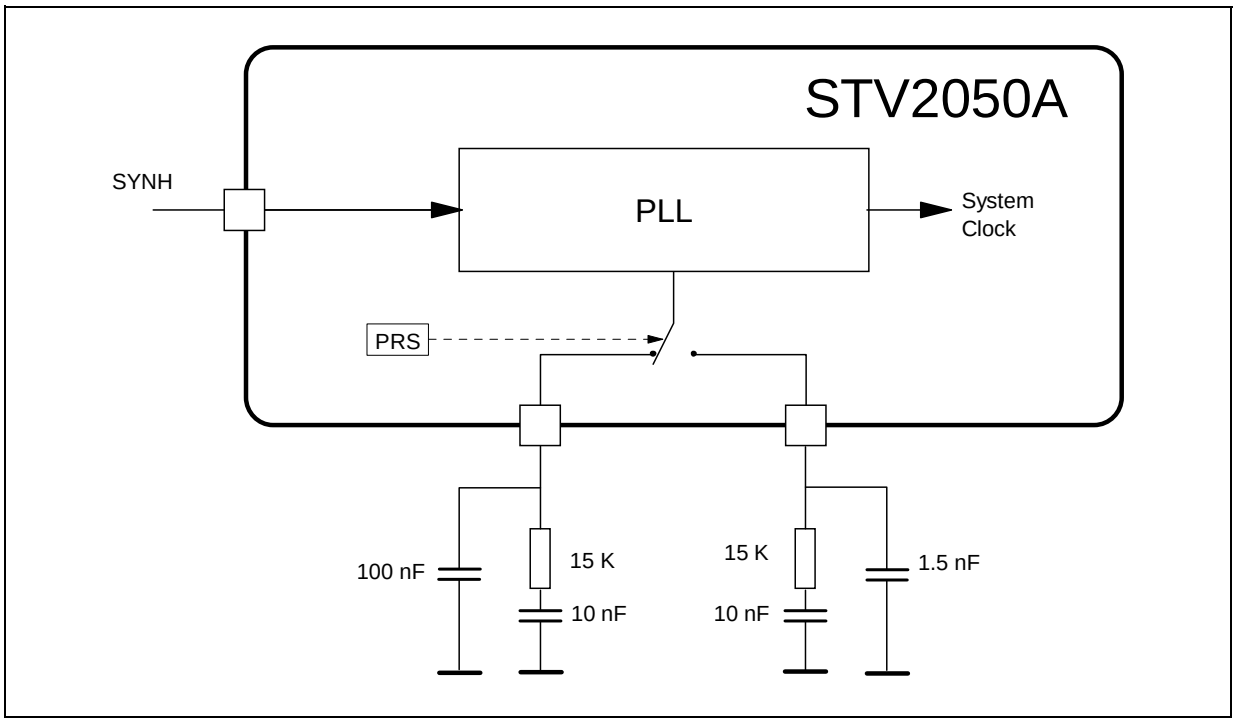
Note: X = Don't care, 0 or 1: The corresponding bit MUST be set to this value for normal operation.

5 TIMEBASES

5.1 LINE LOCKED PLL AND SYSTEM CLOCK

A frequency-multiplying PLL derives the internal ***system clock*** from the incoming signal at the SYNH pin. This signal is derived from horizontal deflection.

Figure 9. Line-Locked PLL and System Clock



The PLL is designed to drive 1H, 2H, HDTV and SVGA applications. Two loop filters can be implemented using the FILT (pin 24) and FLT2 (pin 25) pads. The selection can be forced by the PRS bit in the D5 register.

PRS	0 = FILT selected (2H and above range operation recommended) 1 = FLT2 selected (1H range operation recommended)

The horizontal deflection is often turned off when switching TV set modes. Therefore the PLL provides a base frequency when the external sync signal is missing (both H and V sync signals are missing).

The $N_{(clk/line)}$ ratio between the system clock and the incoming sync signal is calculated using the HGD[5:0] and HRD[5:0] values in the D8 register. (Refer to Section 7.2.1 "Horizontal Grid Adjustment" on page 35):

$$N_{(clk/line)} = 14 * (HGD+1) + 2 * (HRD+1)$$

where: $N_{(clk/line)} < 512$

$HGD > 15$

$HRD > 15$

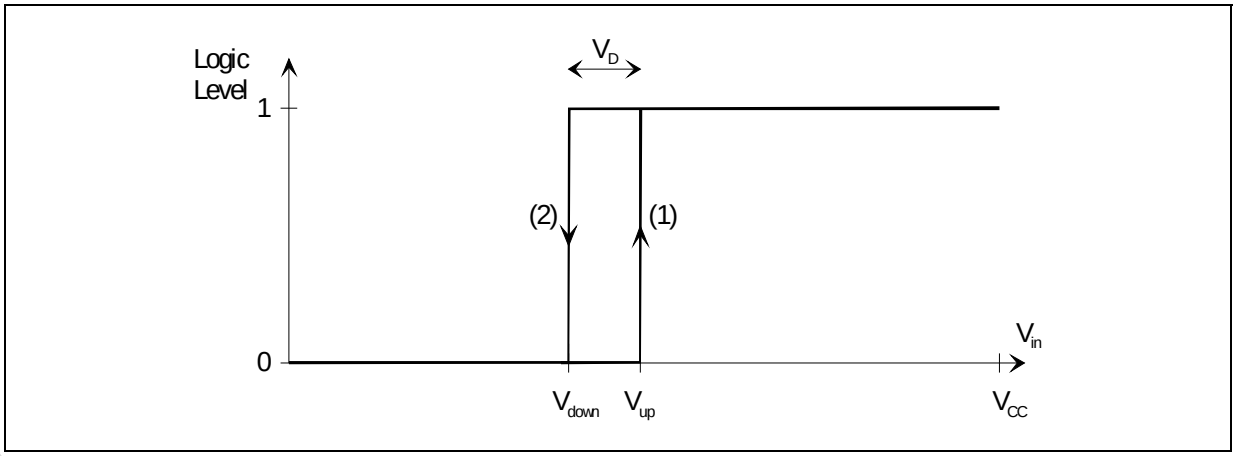
For all modes, in normal operation, the incoming timing signal at the SYNH pin will not have a phase deviation greater than ± 2 µs from line to line. Greater phase deviations may occur when switching modes or changing channels. The PLL is expected to recover from these events and lock within one vertical field of consistent phase that is within the normal horizontal operation limits.

5.2 SYNCHRONIZATION INPUTS

The two synchronization inputs, SYNH (pin 27) and SYNV (pin 28) slice the Line or the Frame Flyback, respectively, via a Schmitt trigger.

This also ensures a very stable detection of the synchronization signals, regardless of the temperature.

Figure 10. Synchronisation Signals



5.3 HORIZONTAL TIMEBASE

The horizontal timing is based on the built-in PLL.

5.3.1 Horizontal DAC Phase

In order to compensate the delay of the external amplifiers and the response time of the convergence coils (t_d), the values for convergence correction are given out prior to the corresponding horizontal video position. The time delay between video position and the output of

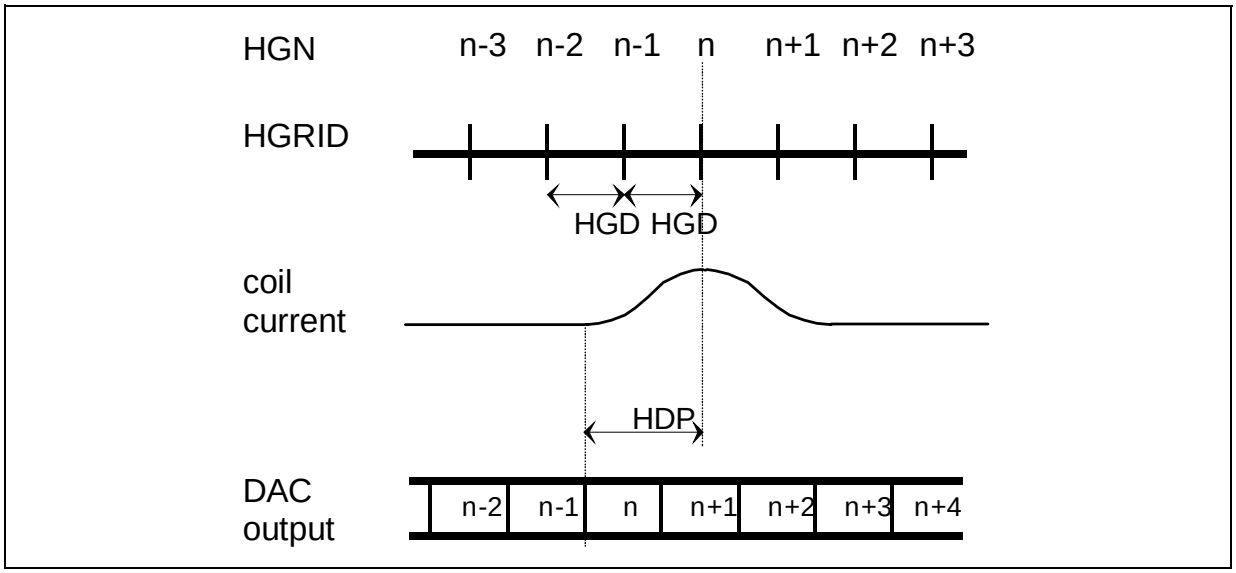
the corresponding convergence correction value is defined by the Horizontal DAC phase HDP[6:0] value in the DB register.

The following range for the horizontal DAC phase is allowed:

$$0 \leq HDP \leq 2 \times HGD$$

The timing of the DAC output leads the most if HDP is equal to zero.

Figure 11. Horizontal DAC Phase



5.3.2 Horizontal Width Adjustment

In order to fit the video pattern into the full visible area of the screen, the width of the pattern may be adjusted. Horizontal width adjustment is done by changing the number of clock cycles between the vertical grid lines during retrace and the visible grid. The timing for the corresponding DAC values is changed accordingly. Refer to Section 7.2.1 "Horizontal Grid Adjustment" on page 35.

5.3.3 Auto-Calibration of DACs

All the DACs of the STV2050A can be automatically calibrated. This feature ensures a high matching stability in both time and temperature. The process involves the sequential calibration of 120 cells.

To ensure optimal results, each cell must be calibrated at least every 4 ms.

The duration of one cell calibration must be greater than 2us. This duration is controlled by the internal “calibration clock”. The calibration clock is generated using a divider of the system clock. (Refer to Section 5.1 "LINE LOCKED PLL AND SYSTEM CLOCK" on page 22). The division ratio is programmable via the ACL[1:0] bits in D8.

ACL[1:0]	00: No calibration 01: Division by 16 10: Division by 32 11: Division by 48

Autocalibration can take place either during the full line, or during the line retrace only. This is controlled by the ACW bit in the D8 register.

ACW	0: During line retrace only 1: During the full line

If the “During Line Retrace Only” autocalibration is selected, the number of DAC cells calibrated during each line retrace is defined by the AFS[1:0] value in the D8 register.

AFS[1:0]	00: 1 cell / line 01: 2 cells / line 10: 3 cells / line 11: 4 cells / line

Two autocalibration modes can be selected by the AMS[0] bit in the D5 register.

AMS[0]	0: The autocalibration process is not synchronized to vertical timing 1: The autocalibration is synchronized to vertical IC timing. The counter which selects the DAC cells that are to be calibrated is reset on each frame retrace.

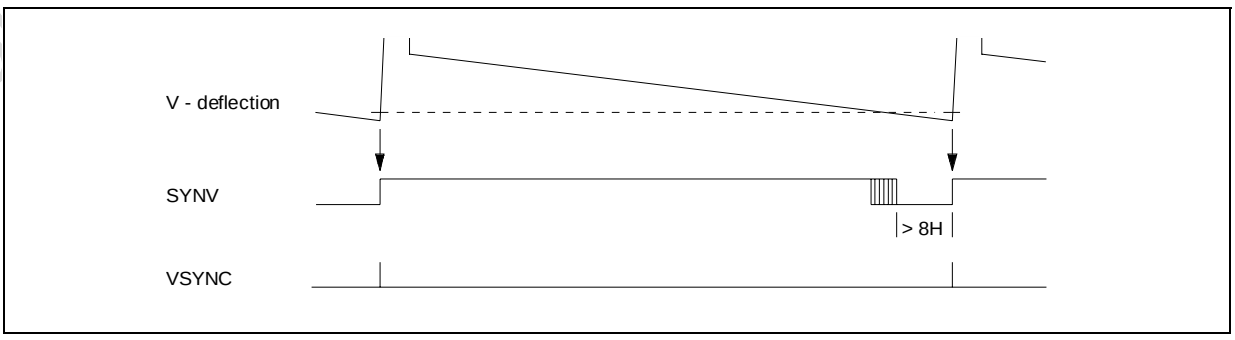
The time interval for auto-calibration is normally centred to the retrace. But it is possible to adjust the start point by programming the ASP[2:0] bits in the D8 register. One step corresponds to one system clock cycle.

5.4 VERTICAL TIME BASE

5.4.1 Vertical Synchronization Signal

The vertical timing is based on the vertical deflection signal. A debounce filter is implemented to prevent interference on the SYNV signal caused by crosstalk, mainly from horizontal deflection. This filter accepts a rising edge of the SYNV signal only when SYNV is 'LOW' for a time ≥ 8 TV lines (determined by 8 pulses at the SYNH input).

Figure 12. Vertical Synchronization Signal



5.4.2 Field Parity Recognition

In the case of a standard STV2050A implementation, synchronization is achieved using signals extracted horizontally (Line Flyback) and vertically (Frame Flyback). Unfortunately, depending on the components and the configuration, the phase relationship between these signals is not the same in every TV chassis. In this case, field parity recognition can be unreliable unless special features are implemented. The STV2050A can achieve perfect field parity recognition using the “Vertical Sync shifT“ (VST).

When the VST[7:0] bits in the DA register are set to the optimum value, the STV2050A distinguishes perfectly between the two fields. This is used to control the interpolation of the convergence values and the video pattern generator according to the interlaced scanning scheme.

The correct VST value can be evaluated by measuring the timing of the vertical pulse. This timing is measured by the STV2050A, and the results are stored in the S13[7:0] and S14[7:0] bits in the E6 register.

In non-interlaced mode, field recognition can be switched off by the IIE bit in the DA register.

IIE	0 = Interlace OFF 1 = Interlace ON

5.4.3 Field Counter

A 4-bit field counter is implemented for controlling the optical alignment procedure. The counter value is stored in the S12[3:0] bits in the E5 register (read only).

This counter will be reset to 0000 at IC power-up and will be incremented after every vertical reset. The counter will overflow from 1111 to 0000. (The counter will not be reset when the E5 register is read.)

5.4.4 Convergence Correction Frame Retrace

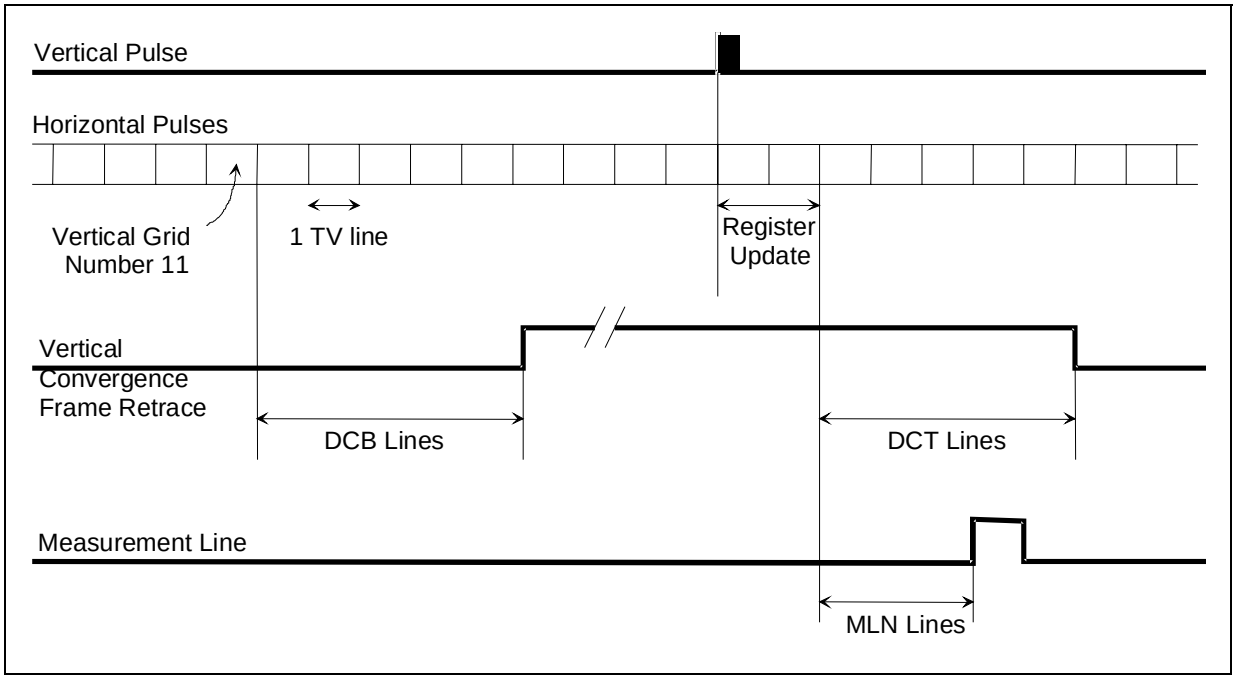
This is the time interval defined as follows:

– Start at grid line number 11 + DCB[7:0] bits in the DB register,

– Stop at 2 TV lines after the frame pulse + DCT[8:0] bits in the DB register;

where DCB and DCT are the number of TV lines.

Figure 13. Vertical Time Base



6 MASTER I²C BUS INTERFACE

A master I²C bus implemented in the STV2050A is used to transfer data between the IC embedded RAM and the external 2K x 8-bit EEPROMs (for example, the 24164 manufactured by ST). The protocol supports up to 7 EEPROM addresses which can be selected using the 3 **EEPROMadd**[2:0] bits in the E9 register.

Master activities are initiated either by an external reset of the STV2050A, or by commands from an external MCU via the Slave I²C bus. The following features are implemented in the Master I²C Bus interface:

– Reset the I²C bus to the EEPROM

– Read a specified data range from EEPROM to RAM

– Write a specified data range from RAM to EEPROM

– Check if an EEPROM register is available

– Power-on sequence

– Security features

– Generate status information

The organization of data in the embedded RAM is completely different from that in the EEPROM register. Therefore, address transformations are required in both directions. This is carried out by the STV2050A in a way that is fully transparent for the user.

The external MCU initiates a master access to the EEPROM by writing a command to the E9 address. This command contains information about the type of access and specifies one of seven EEPROMs (refer to Section 6.6 "DATA TRANSFER BETWEEN RAM AND EEPROM" on page 30).

The embedded RAM contains convergence correction data and one adjustment data set (ADS) to control the various modes of the STV2050A. Three ADSs can be stored in the EEPROM. One of these three sets is selected by the two ADS[1:0] bits in the E9 command to be mapped to the register RAM area inside the IC.

Any command sent from the MCU to the E9 address while the master is active will be lost. Also, the EEPROM address which is included in this command will not be accepted.

Before addressing the E9 register, the MCU should check if the master is active. To do this, the RWM[2:0] bits in the E9 register must be set to “001” (bin). The corresponding status is given on the STX[2] bit.

If any error are detected during the transmission of data on the EEPROM I²C bus, the transmission is stopped and the corresponding STX[3] bit of the status section of the E9 register is set.

Read or Write modes can be selected by setting bit RWM[2] in the E9 register.

RWM[2]	0 = Read mode 1 = Write mode

6.1 READ OPERATION MODES

Two modes of read sequences are implemented by selecting the RWM[1:0] bits.

RWM[1:0]	11 (bin): Read all convergence data and an ADS 10 (bin): Read an ADS only

6.2 WRITE OPERATION MODES

Three modes of write sequences are implemented by selecting the RWM[1:0] bits.

RWM[1:0]	01 (bin): Write all convergence data and one of the three ADSs 00 (bin): Write only one of the ADSs 10 (bin): Write only the “static” (position offset) values

6.3 POWER-ON SEQUENCE

At power-on, the master interface runs a special sequence to build up the convergence correction data and the STV2050A RAM is loaded with data from a user-specified EEPROM.

6.4 SECURITY FEATURE DURING DATA TRANFERS

Since access to an EEPROM register is critical with respect to system performance, all EEPROM access commands in the E9 register, together with the corresponding addresses, are protected by the 2-bit, error-detecting Hamming code. If the circuit detects an error, the Master will not initiate an EEPROM access and an error bit will be set in the status register.

If any errors are detected during the transmission of data on the I²C bus, the transmission is stopped and the corresponding STX[3] bit in the status section of the E9 register is set.

6.5 STATUS INFORMATION

Four STX[3:0] bits are available in the status section of the E9 register. These bits continuously reflect the activity and the error status of the master I²C bus interface.

– STX[3] = ´TRANSMISSION ERROR´
  This bit is set to low if an error in the transmission of an EEPROM access command was detected. It remains low until the next error-free transmission to register E9 is completed.

– STX[2] = ´EEPROM ACCESS FINISHED´
  This bit is set to low when the master I²C-bus interface has completed bus activities. This bit does not display the completion of an EEPROM access. This bit is set high by the master at the start of a new bus sequence or by the slave after reading status register E9.

– STX[1] = ´EEPROM R/W´
  This bit is set to low when the master has initiated an access to the EEPROM. It remains low until the sequence is finished or the sequence is terminated by an access error.

– STX[0] =´EEPROM PROBLEM´
If A Read or Write sequence has been terminated with an access error, the STX[0] bit is set to low. It is set back to high when the master starts the next R/W sequence.

6.6 DATA TRANSFER BETWEEN RAM AND EEPROM

Data is transfered using the following I²C BUS sequence after a bit in the E9 register has been read or written: S DW SA D0 D1 D2 P

Where:

– SA = E9: Selection of the E9 register, EEPROMadd[2:0] is the hardware EEPROM address used by the I²C Master,

– RWM[2:0] selects the Read or Write mode as previously described,

– HAM[2:0]: Hamming code used to protect the D0[7:0] and D1[7:4] data bits. Refer to Section 14.2 "HAMMING ENCODING" on page 62.

The total transfer lasts approximately 200 ms if the I²C master clock is operating at 70 kHz.

	MSB							LSB																
	BYTE D0								BYTE D1								BYTE D2							
ADD	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
E9	EEPRO-Madd [2:0]			X	X	X	ADS[1:0]		RWM [2:0]			X	HAM[3:0]				X	X	X	X	STX[3:0]			

6.7 MASTER CLOCK FREQUENCY

The I²C Master uses its own timebase with a local oscillator. The frequency is fixed by external filter (R1/C and R2) as shown in Figure 14 "Master I²C Clock" on page 31.

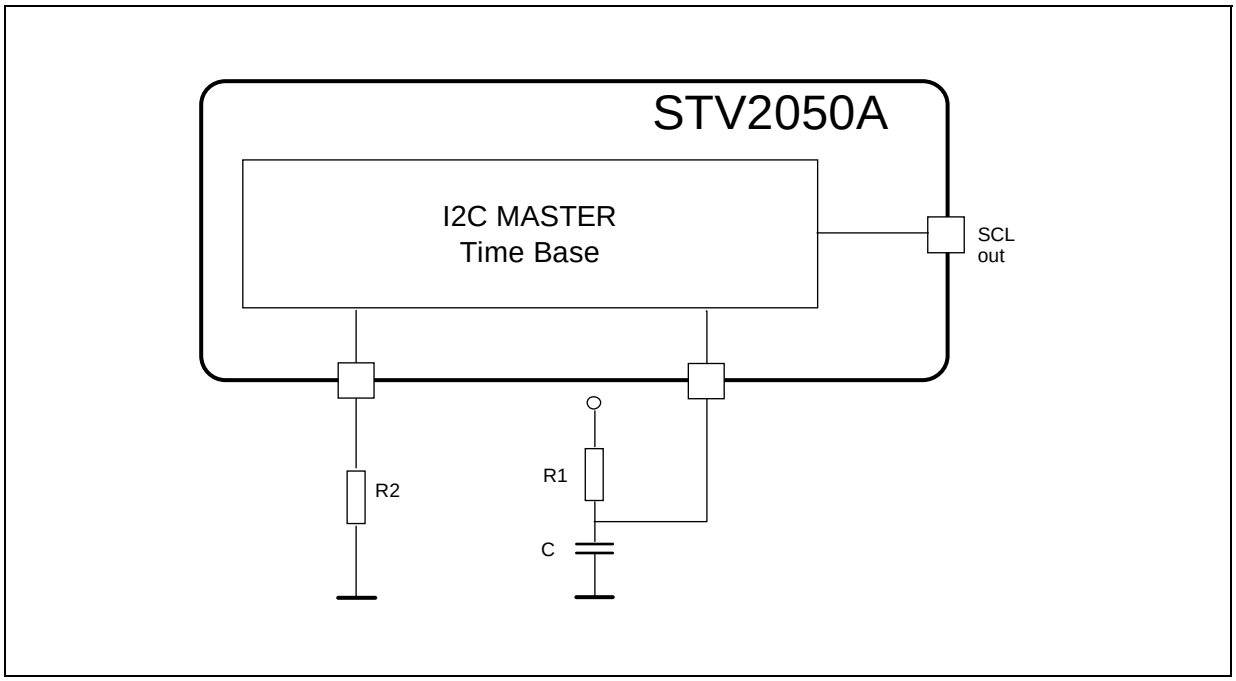
Typical values are:

– R1 = 82 kΩ

– R2 = 10 kΩ

– C = 33 pF

Figure 14. Master I²C Clock



7 VIDEO PATTERN GENERATOR

The STV2050A provides a built-in video pattern generator for convergence adjustments. The RGB signals are generated by 4-bit DACs with a voltage output. The FBLK signal is used to switch the RGB source inside the TV set. The FBLK is a fixed-voltage output. The video pattern generator delivers five types of video patterns:

– **Cross-Hatch Grid**:
  Displays the physical locations corresponding to the stored correction values. Refer to Section 7.2 "CROSS-HATCH GRID" on page 35.

– **Cursor**:
  A crosshair is displayed at the place corresponding to the current addressed memory location.

– **Border Lines**:
  Used to adjust the convergence at the horizontal and vertical edges of the visible screen area. Refer to Section 7.4 "BORDER LINES" on page 37.

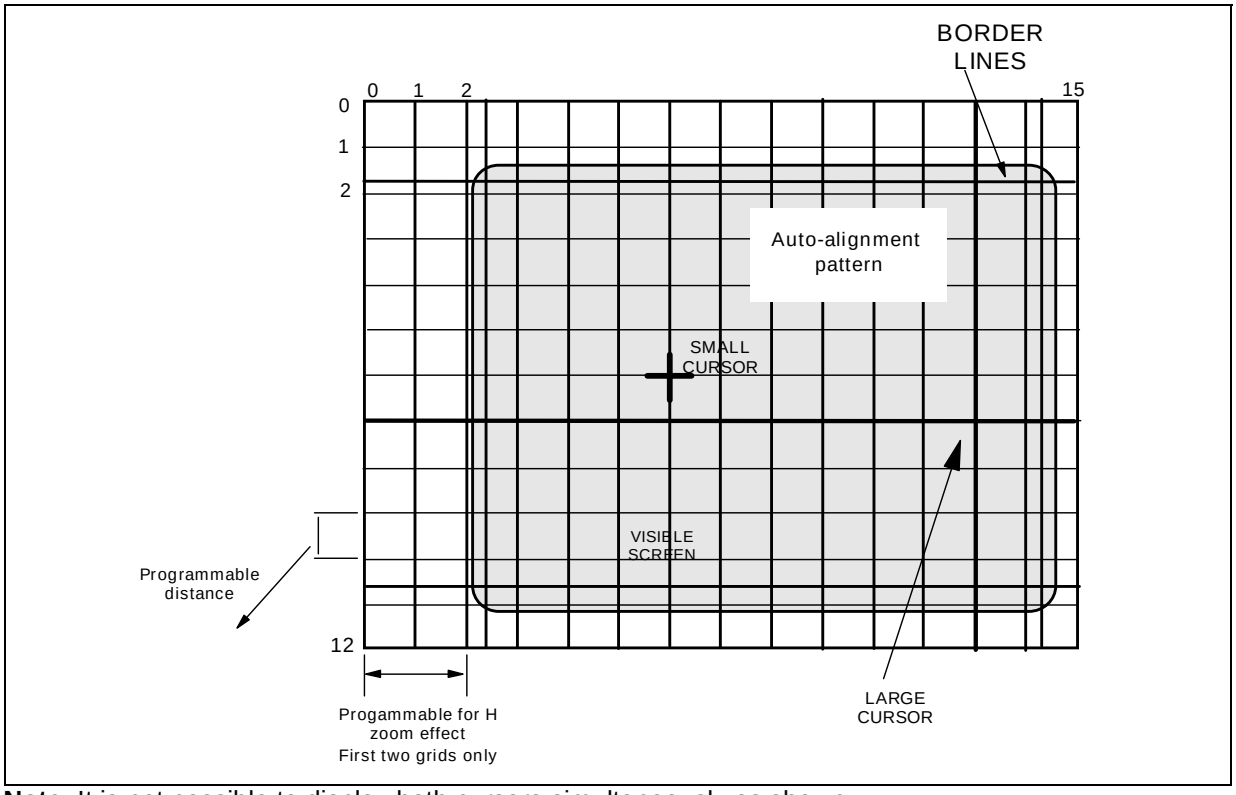
– **Gain Adjustment Lines**:
  Used to easily adjust the gain of the convergence channels and to optimize interlace mode.

– **Auto-alignment Pattern**:
  Supports an auto-alignment procedure.

The video generator also produces the control signals for the optional optical loop functions.

The patterns can be modified using several parameters in the registers of the STV2050A.

Figure 15. Auto-alignment Pattern



Note: It is not possible to display both cursors simultaneously as shown.

7.1 GENERAL FUNCTIONS

7.1.1 Pattern Selection

The color components (RGB) for the video pattern can be separately switched on and off by the COV[2:0] bits in the EA register. If the control bit for one color is set to 0, the corresponding DAC output is switched to 0V.

COV[2]	0: Red = Off 1: Red = On
COV[1]	0: Green = Off 1: Green = On
COV[0]	0: Blue = Off 1: Blue = On

The type of the pattern is selected by the PAS[4:0] bits in the EA register.

PAS[4]	0: Auto-alignment Pattern Off 1: Auto-alignment Pattern On
PAS[3]	0: Small Cursor 1: Large Cursor
PAS[2]	0: Cursor Off 1: Cursor On

PAS[1]	0: Grid Off 1: Grid On
PAS[0]	0: Border Off 1: Border On

The FBLK output is switched to ´high´ voltage when at least one color is activated by the COV bits in the EA register when the STA bit in the D7 register is activated. If no color is selected, the FBLK output is switched to ´low´ voltage. For other features of the FBLK pin, refer to Section 8.4 "FAST BLANKING" on page 43.

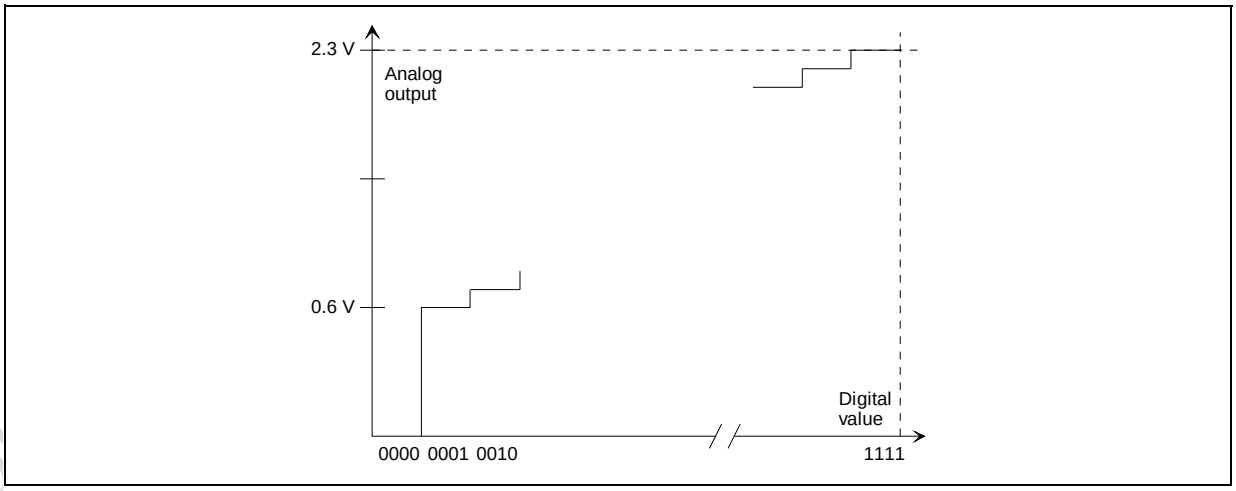
The video signal representing a vertical line (grid, border, cursor) has the shape of a pulse with a width of one system clock cycle.

7.1.2 Pattern Visibility Adjustment

Since the bandwidth of the RGB signal path is limited, horizontal and vertical lines may appear on the screen with different brightness levels. To compensate for this effect, it is possible to adjust the brightness values for the horizontal line (PBH[3:0]) bits and the vertical line (PBV[3:0]) bits in the D6 register of the video pattern.

The video brightness has 4-bit resolution. The 0(hex) value corresponds to the 0.0 V output from the video DACs. The 1(hex) value corresponds to a typical 0.6 V output. All other steps are equidistant.

Figure 16. Pattern Visibility Adjustment



If the PBH bit is set to zero, the amplitude of the auto-alignment pattern is determined by the PBV bit.

Using the VDC bit in the EA register, the frequency compensation of the video DACs can be adapted according to the system clock.

VDC	0: Low Current 1: High Current

7.2 CROSS-HATCH GRID

The convergence values are adjusted and stored for an array of 16 x 13 points. These points can be displayed by the grid lines of the video generator. The deflection correction at the grid points corresponds to the digitally stored values. Several programming features are used to adapt the grid, and therefore the convergence adjustment, to the needs of the application. All parameters for the grid are included in the data set stored in the internal RAM.

7.2.1 Horizontal Grid Adjustment

The horizontal distance of the grid lines is determined by the values of the HGD[5:0] and HRD[5:0] bits in the D8 register. Refer to Figure 17 "Horizontal Grid Adjustment" on page 35.

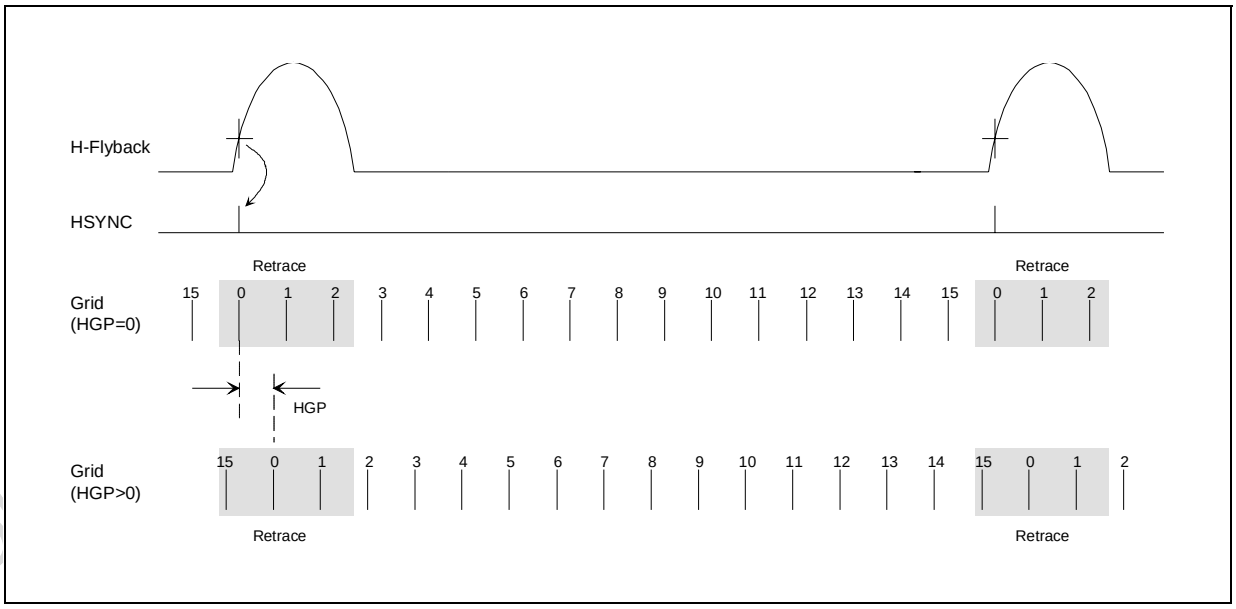
Between each grid line, a minimum of 16 system clock cycles is required for calculating the convergence. (Refer to Section 5.1 "LINE LOCKED PLL AND SYSTEM CLOCK" on page 22). The geometrical distance between two vertical grid lines can be modified by adding clock cycles between the visible grid lines (HGD) or by adding clock cycles during the horizontal retrace (HRD).

– HGD: horizontal grid distance during active line.

– HRD: horizontal grid distance during line retrace.

The left-right position is controlled by the HGP[6:0] bits in the D7 register.

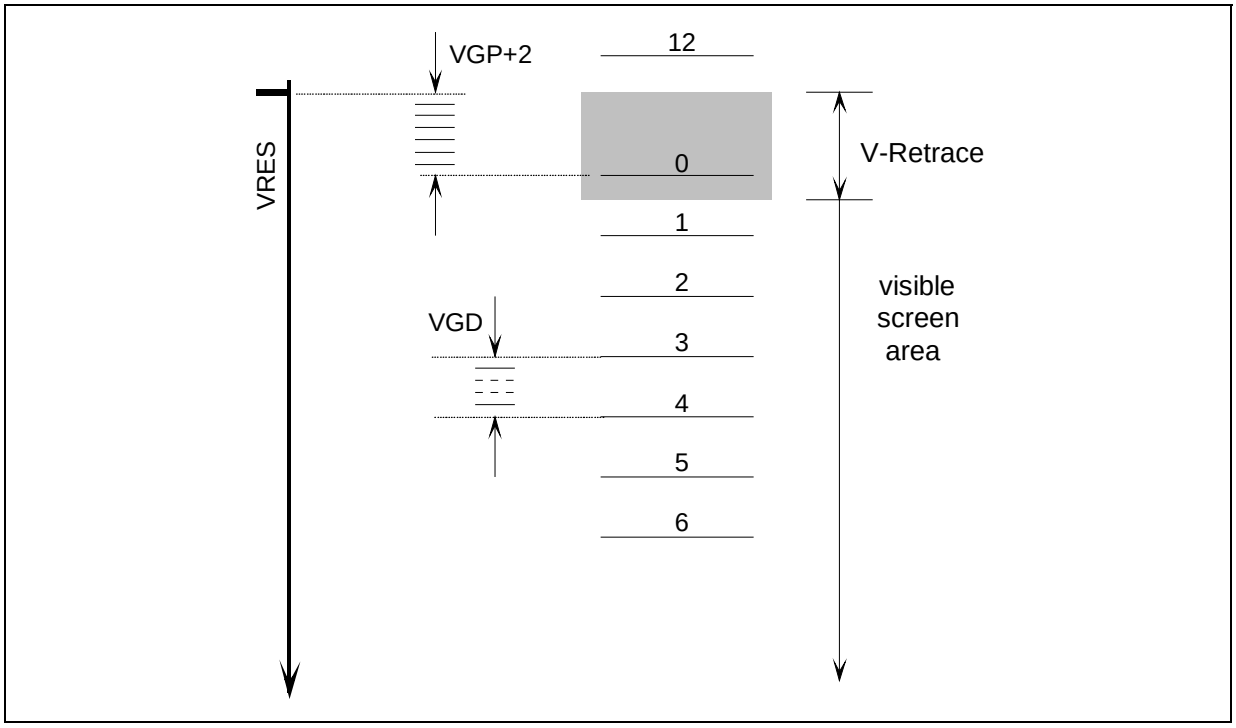
Figure 17. Horizontal Grid Adjustment



7.2.2 Vertical Grid Adjustment

In the same way, the vertical grid adjustment is done using the VGP[8:0] and VGD[5:0] bits in the D9 register.

Figure 18. Vertical Grid Adjustment



If the VGP bit is programmed to 0, the grid starts with the first line following the two lines that are reserved for the register update procedure.

The allowed range for the VGP is included between the 0 and 511 video lines.

7.3 CURSOR

7.3.1 Cursor Size

The cursor is available in different shapes. The shape is selected by the PAS[3] cursor-type bit in the EA register.

PAS[3]	0: Small Cursor 1: Large Cursor

7.3.2 Cursor Position

The position of the cursor is determined by the most recent write command on the I²C bus.

The embedded RAM addresses of dynamic convergence correction values correspond directly to grid positions on the screen. They represent cursor positions as well.

If the CPV (Cursor Position Vertical) value exceeds the 0...C(hex) range, the cursor is not displayed.

If a new write address is within the accepted grid range (after having exceeded the range), the cursor pattern is re-displayed (unless the cursor display is turned off).

7.4 BORDER LINES

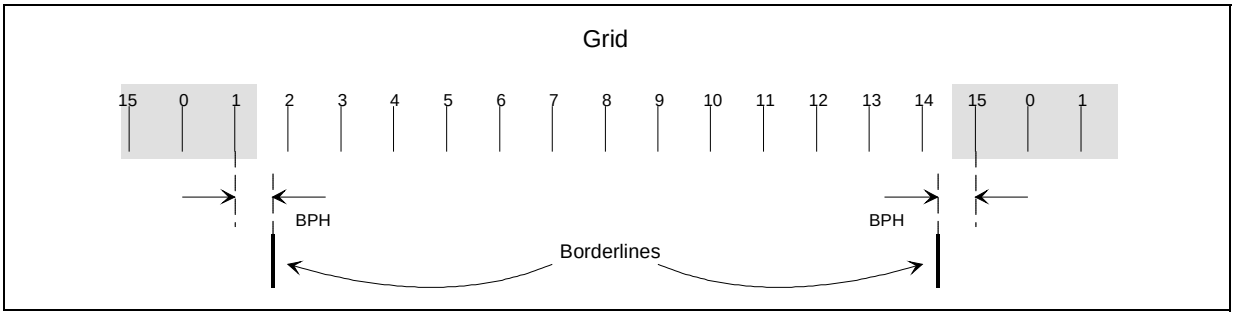
Convergence adjustments at the edges of the screen are more difficult because the grid points which are involved are not visible. Therefore, additional horizontal and vertical border lines are implemented for making adjustments at these positions.

7.4.1 Border Lines: Left / Right

The horizontal position of the border lines is programmable by the BPH[5:0] bits in the D7 register.

00h	The position of the border lines is identical to the vertical grid lines at horizontal grid positions 1 and 15
01h to 1Fh	The border lines move toward the centre of the screen in increments of BPH clock cycles. The range for the shift of the border line is one horizontal grid distance.

Figure 19. Border Lines



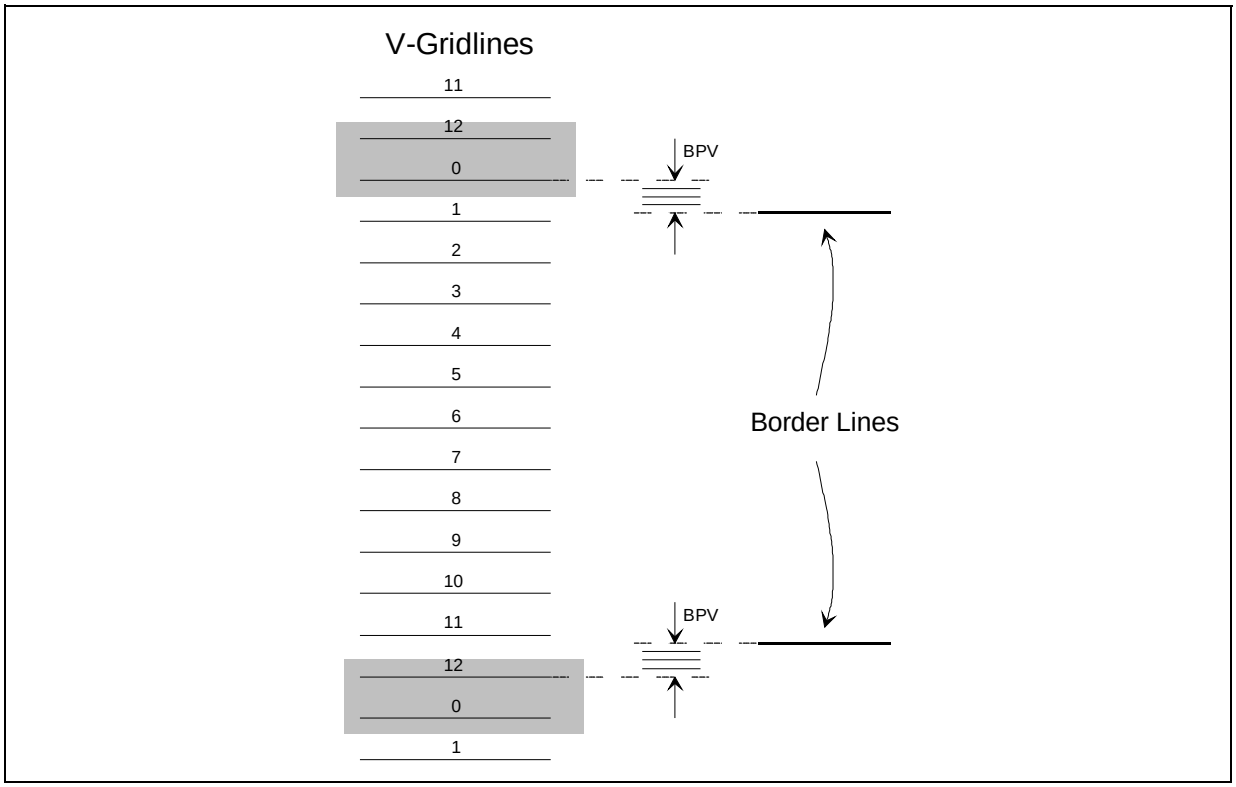
Note: The BPH bit must be smaller than the HGD bit.

7.4.2 Border Lines: Bottom / Top

The vertical position of the border lines depends on bits BPV[5:0] in register D7.

00h	The position of the horizontal border lines is identical to the horizontal grid lines at positions 0 and 12.
01h to 1Fh	The horizontal border lines move toward the centre of the screen by BPV video lines. The allowed range for the BPV value is one vertical grid distance.

Figure 20. Vertical Border Lines



Note: The value of the BPV bit must be smaller than that of the VGD bit.

7.5 GAIN ADJUSTMENT LINES

The “Gain Adjustment Lines” pattern is used mainly for 2 purposes:

– To calibrate the convergence currents in order to achieve a consistent geometrical correction on the screens of a series of PTVs,

– To have an easy visual adjustment of the interlace mode.

The cursor has two different shapes, one for the adjustment of the vertical gain and another for the adjustment of the horizontal gain.

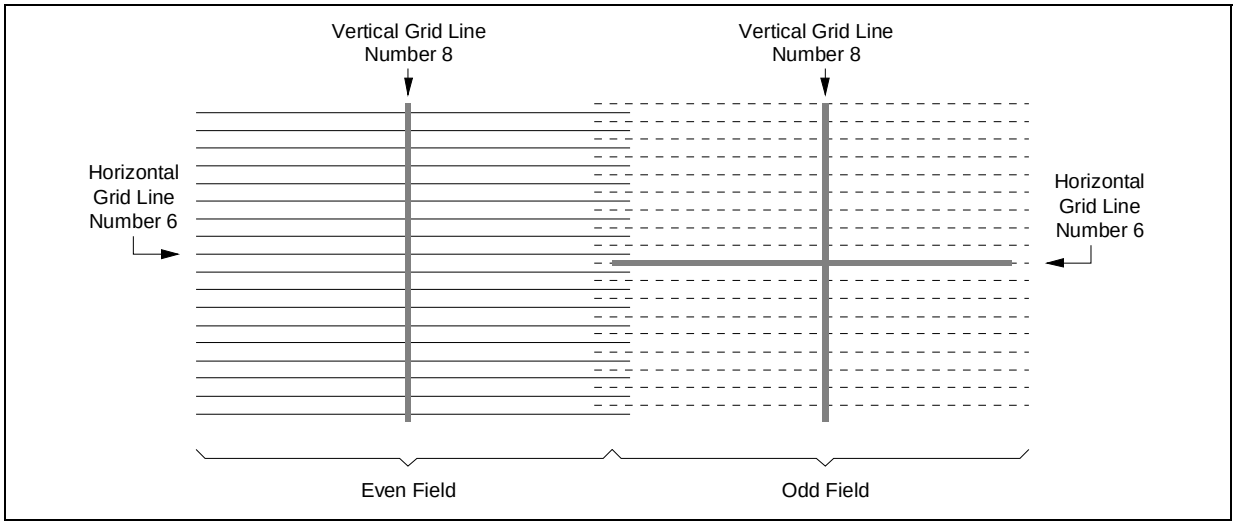
The video pattern for the gain cursor is defined in the EA register.

GCP	0: Gain cursor video pattern off 1: Gain cursor video pattern on
VHV	0: Horizontal gain cursor video pattern 1: Vertical gain cursor video pattern

7.5.1 Video Pattern for Horizontal Gain Cursor

The horizontal gain cursor can be used for adjusting the horizontal convergence channels. The video pattern in the odd field is identical to the video pattern of the large cursor displayed at the centre of the visible grid.

Figure 21. Video Pattern for Horizontal Gain Cursor

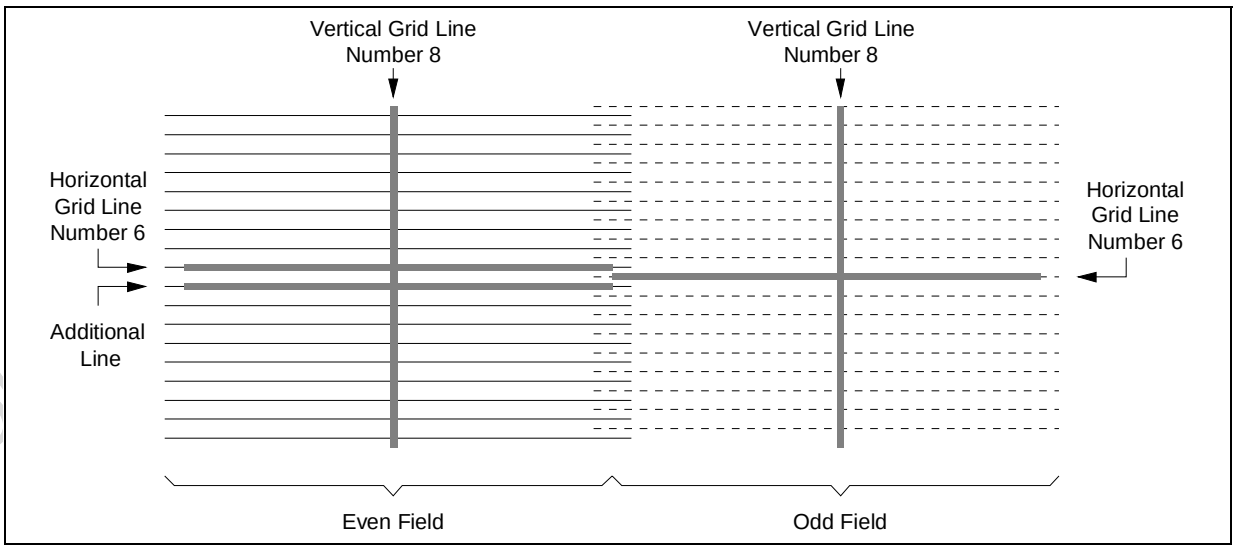


Note that these controls only modify the video signals. They have no effect on the convergence signals. The dedicated controls of the convergence signals are described in Section 9.7 "MANUFACTURING, AFTER-SALES SERVICE, LAB TRIAL MODES" on page 49.

7.5.2 Video Pattern for Vertical Gain Cursor

The video pattern for the vertical gain cursor is identical to video pattern for the horizontal gain cursor (displayed at the centre of the visible grid), except for one horizontal line which is added only in the even TV field.

Figure 22. Video Pattern for Vertical Gain Cursor



7.6 AUTO-ALIGNMENT PATTERN

The auto-alignment pattern is a rectangular, highlighted part of a screen with a constant brightness (horizontal brightness). See Figure 23 "Auto-alignment Video Pattern" on page 40.

The On/Off is controlled by the PAS[4] bit in the EA register

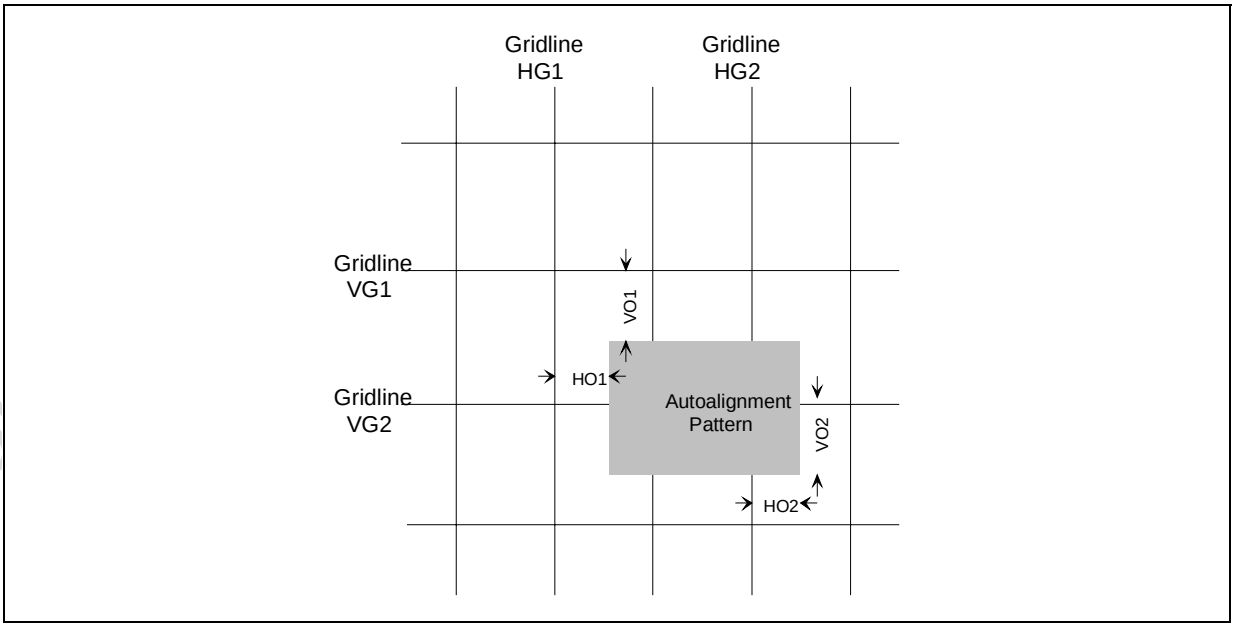
PAS[4]	0: Auto-alignment pattern off 1: Auto-alignment pattern on

The size and the position of the pattern can be controlled by the EB and EC registers. The pattern is defined by its horizontal and vertical start and stop values: HO1, HG1, HO2, HG2, VO1, VG1, VO2 and VG2.

HG1[3:0]	Grid number of horizontal pattern start
HO1[5:0]	Offset of horizontal pattern start (number of clock cycles, 1 grid max.)
HG2[3:0]	Grid number of horizontal pattern end
HO2[5:0]	Offset of horizontal pattern end (number of clock cycles, 1 grid max.)
VG1[3:0]	Grid number of vertical pattern start
VO1[5:0]	Offset of vertical pattern start (number of video lines, 1 grid max.)
VG2[3:0]	Grid number of vertical pattern end
VO2[5:0]	Offset of vertical pattern end (number of video lines, 1 grid max.)

Offset position values must be one grid distance smaller than the vertical grid numbers for start or stop positions.

Figure 23. Auto-alignment Video Pattern



The pattern may be defined so that an end value is less than the start value. In this case, the window will wrap around through the retrace without any interruptions (two or four rectangles will be highlighted on the screen).

The auto-alignment pattern signal is influenced by the horizontal or vertical blanking function.

8 BLANKING OF VIDEO SIGNALS

The output of the RGB signals can be set to 0V during the horizontal and vertical retrace. The function is controlled by the D6 register. The horizontal and vertical retrace blanking function can be enabled independently.

8.1 HORIZONTAL BLANKING

The HBE bit in the D6 register is used to enable/disable the horizontal blanking.

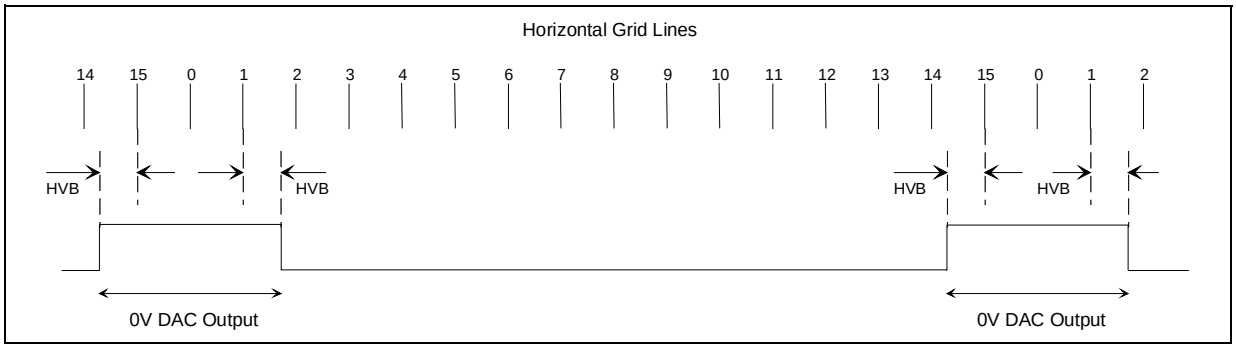
HBE	0: Horizontal Blanking Off 1: Horizontal Blanking On

The start and end edge positions are determined by the HVB[5:0] bits in the D6 register.

If the horizontal blanking is enabled, the video outputs are set to 0V from the HVB clock cycles before grid line number 15 until the HVB clock cycles after grid line number 1. The useful range for the HVB is one horizontal grid distance. This function is similar to the border line function.

If '0' is programmed, grid lines no. 15 and no. 1 are not blanked.

Figure 24. Horizontal Grid Lines



Note: If the HVB values are greater than the HGD values, unexpected effects will appear on the screen.

8.2 VERTICAL BLANKING

The enable/disable control is the VBE bit in the D6 register.

VBE	0: Vertical Blanking Off 1: Vertical Blanking On

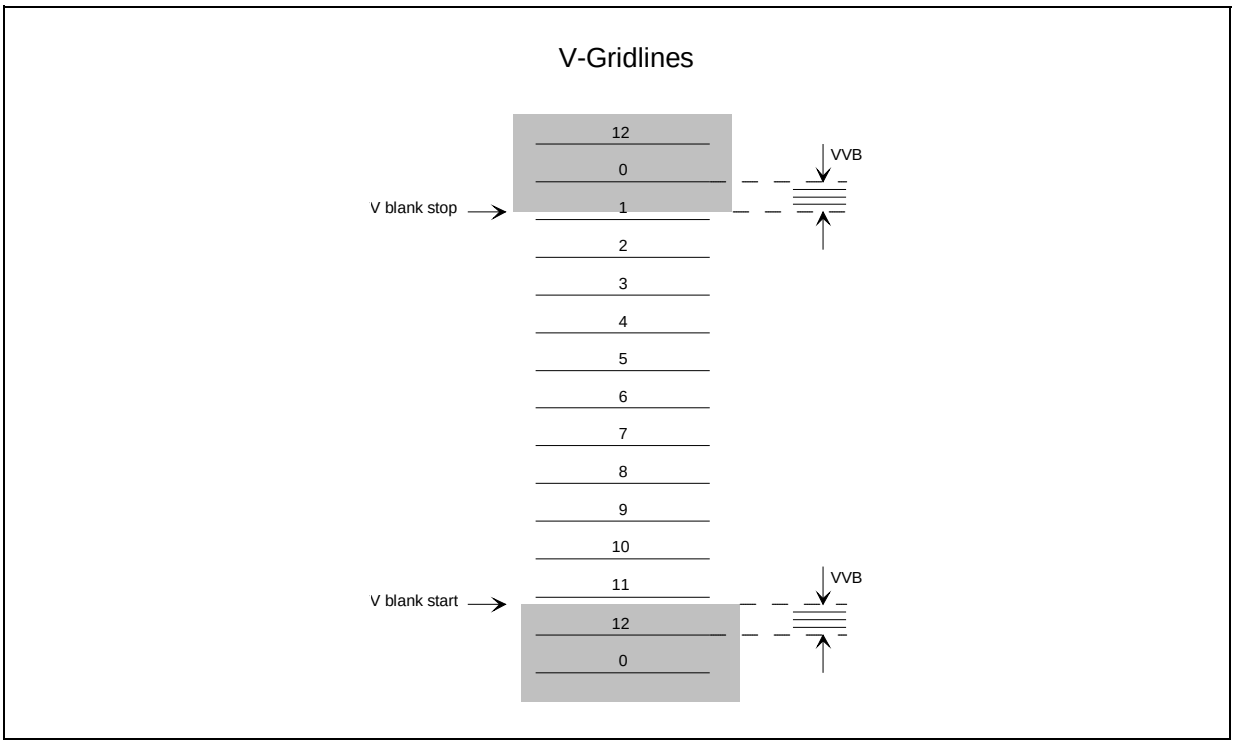
The start and end edge positions are determined using the VVB[5:0] bits in the D6 register.

The video blanking function ends when the programmed number of VVB video lines, following vertical grid line no. 0, are finished **and** the next video line following the end of the DAC retrace mode (DCT) has begun.

The VVB range is one vertical grid distance. The function works the same as the border line function. If '0' is programmed, grid lines no. 0 and no. 12 are not blanked. If the values pro-

grammed for VVB are greater than those of the VGD, unexpected effects will appear on the screen.

Figure 25. Vertical Blanking



8.3 BLANKING FOR AUTO-ALIGNMENT PATTERN

The blanking for the auto-alignment pattern and for the other video pattern are linked to the same timing which is defined by the HVB and VVB bits as described in the following sections.

HAE	0: Horizontal blanking off 1: Horizontal blanking on
VAE	0: Vertical blanking off 1: Vertical blanking on

8.4 FAST BLANKING

The FBLK pin is used to provide a fast switching signal that selects the source of the video signal to be displayed on the screen. Features are controlled by the D7 register.

STA	0: FBLK depends on the TVH, TVV and FAS bits (see below) 1: FBLK is forced to 1, if a pattern color is enabled by the COV bits. (Refer to Section 7.1.1 "Pattern Selection" on page 33)
TVH	Blanking of TV picture in horizontal direction 0: Blanking off 1: Blanking on

TVV	Blanking of TV picture in vertical direction 0: Blanking off 1: Blanking on
FAS	0: Normal TV picture only 1: The normal TV picture is overlapped by the video pattern

The TVH and TVV bits are designed to be used, for example, in front projection applications. They are used to cut off TV video information at the left and right edges, as well as at the top and the bottom of the projection area that belongs to the overscan region in standard TV sets.

9 CONVERGENCE

The STV2050A generates convergence values from parameters which are stored in the embedded RAM after having being loaded down from the EEPROM. These parameters can be:

– Common for the entire screen area for each color. They are called “common values”. They are used for global adjustments, as they have the same effect on all the convergence values of the same color and in the same direction (horizontally or vertically).

They are used mainly:

– To pre-adjust the geometry and convergence, as well as to reduce the necessary action on each separate point,

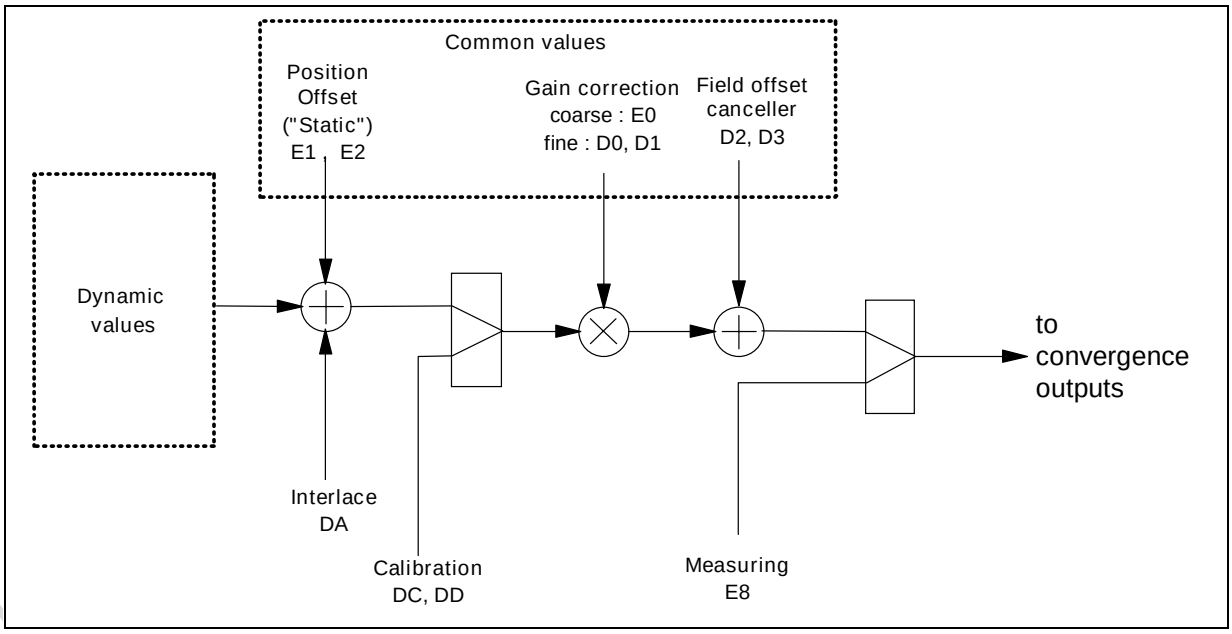
– To compensate the tolerances of the offset and gain for the external components.

– Dedicated to each value of the net of 16 points horizontally by 13 points horizontally. They are called “dynamic values”,

– Added as an offset frame by frame (interlacing),

– Forced to special values in alignment modes or during startup and security modes.

Figure 26. Convergence Values Computation Path



9.1 GLOBAL ADJUSTMENTS - COMMON PARAMETERS

Three sets of parameters are available for each red, green and blue channel for each horizontal and vertical direction:

– Position offset,

– Gain correction,

– Offset canceller.

9.1.1 Position Offset (also called “static”)

This value is added to each dynamic value of the corresponding channel. It is used to reach an optimal dynamic value range, and to make a first rough correction.

E1 Register: Horizontal

SRH[7:0]	Red Channel
SGH[7:0]	Green Channel
SBH[7:0]	Blue Channel

E2 Register: Vertical

SRV[7:0]	Red Channel
SGV[7:0]	Green Channel
SBV[7:0]	Blue Channel

The Position offset values are in two’s complement.

9.1.2 Gain Correction

This gain value is applied to the sum of the dynamic value and the position offset (see Figure 26 "Convergence Values Computation Path" on page 45). It is mainly used for compensating the amplification spread of the external components. (Also refer to Figure 31 "Electrical Loop Block Diagram" on page 55).

The gain value is divided into 2 ranges, coarse and fine correction.

E0 Register: Coarse

RCH[3:0]	Red horizontal
RCV[3:0]	Red vertical
GCH[3:0]	Green horizontal
GCV[3:0]	Green vertical
BCH[3:0]	Blue horizontal
BCV[3:0]	Blue vertical

D0 Register: Fine horizontal

RFH[7:0]	Red Channel
GFH[7:0]	Green Channel
BFH[7:0]	Blue Channel

D1 Register: Fine vertical

RFV[7:0]	Red Channel
GFV[7:0]	Green Channel
BFV[7:0]	Blue Channel

9.1.3 Field Offset Canceller

This offset value is totalled after the gain correction. Its purpose is mainly to cancel the differential offset between all channels (see refer to Section 11 "ELECTRICAL LOOP" on page 55).

D2 Register: Fine horizontal

ORG[7:0]	Red Channel
OGH[7:0]	Green Channel
OBH[7:0]	Blue Channel

D3 Register: Fine vertical

ORV[7:0]	Red Channel
OGV[7:0]	Green Channel
OBV[7:0]	Blue Channel

The Field offset values are in two's complement.

Note: During the vertical retrace, the field offset canceller values are the only correction values available on the convergence outputs. Refer to Section 9.6 "NORMAL TV OPERATION MODE" on page 48.

9.2 DYNAMIC VALUES

Dynamic values are stored in register addresses 00 to CF in the three red, blue and green banks. For their allocation, refer to Section 4.1 "CONVERGENCE CORRECTION VALUES" on page 18.

The dynamic values can be adjusted from -512 to +511

	Binary Code MSB --> LSB
-512	'00 0000 0000'
0	'10 0000 0000'
+512	'11 1111 1111'

9.3 INTERLACE

The interlace correction value is defined by the ICV[5:0] bits in the DA register.

This value is added to each convergence value in the field chosen by the IFA bit in the DA register.

The interlace mode is enabled by the IIE bit in the DA register.

IIE	0 = No interlace 1 = Interlace mode

9.4 CALIBRATION

Calibrations can be carried out during manufacturing, or during the normal TV operating mode using the automatic self-alignment procedure via the electrical loop. Refer to Section 11 "ELECTRICAL LOOP" on page 55.

9.5 INTERPOLATION

The 10-bit dynamic correction values are expanded by interpolation to 14 precision bits.

The interpolation of the correction values stored in the embedded RAM produces correction values for the lines between the grid lines.

9.5.1 Vertical Filter

A vertical interpolation is performed by the STV2050A in order to provide a smooth correction transition between the stored points. A complex algorithm is implemented in order to improve the interline geometrical aspect, even when not aligned during chassis production or by the end user.

9.5.2 Horizontal Filter

For each of the three convergence correction channels, an interpolation filter is implemented to calculate the correction values between horizontally-adjacent correction values. Different configuration options are programmable using the D8 register.

HIF[1:0]	00: Filter is not active 11: Filter is not active 01: Filter is a 3-tap FIR filter (2 values per grid) 10: Filter is a 5-tap FIR filter (4 values per grid)
FSO	0: Filter is switched off during horizontal retrace 1: Filter is running continuously

The positions of the calculated additional correction values are timed independently for the visible grid and the retrace grids.

Since operating the filters will increase the DAC frequency by a factor of 2 and 4 respectively, it may be necessary to switch off the filters during the horizontal retrace if the retrace time is short and the line frequency is high. In this case, the filter input data, coming from the vertical interpolation, will be fed directly to the convergence DACs. In any case, this data is processed by the filters in parallel to avoid any discontinuity when the filters are switched back into the data paths.

9.6 NORMAL TV OPERATION MODE

The following bits must remain at logical “1” in the E3 register as defined by the default values during reset:

– the CDO bit (refer to Section 9.8 "CONVERGENCE OUTPUTS" on page 51),

– the CDN bit (refer to Section 9.7 "MANUFACTURING, AFTER-SALES SERVICE, LAB TRIAL MODES" on page 49).

During normal operation mode, the convergence outputs deliver a signal computed as shown in Figure 26 "Convergence Values Computation Path" on page 45.

However, during the convergence frame retrace defined by the DCB and DCT values as described in Section 5.4.4 "Convergence Correction Frame Retrace" on page 26, only the field offset canceller values are output. This is used to reduce the power in the convergence amplifiers.

9.7 MANUFACTURING, AFTER-SALES SERVICE, LAB TRIAL MODES

9.7.1 Output of Field Offset Values

This mode is used to output the field offset values defined in the D2 and D3 registers.

It is controlled by the CDN bit in the E3 register.

CDN	0: Offset values 1: Normal operation

9.7.2 Gain and Offset Measuring Line

This mode is used as a manual control of the measuring line used, for example, in the electrical loop. (Refer to Section 11.1 "PRINCIPLE OF OPERATION" on page 55.)

During the gain measuring line:

– The dynamic values are replaced for each channel by the CRH[7:0] and CRV[7:0] bits for red, CGH[7:0] and CGV[7:0] bits for green and CBH[7:0] and CBV[7:0] for blue in the DC and DD registers for horizontal and vertical values, respectively,

– The polarity of these latter values may be changed using the PMH and PMV bits in the D5 register for horizontal and vertical values, respectively,

– The gain value is stored in the E0 register for the coarse value, but the fine values are stored in the MVR[7:0] bits for red, MVG[7:0] bits for green and MVB[7:0] bits for blue in the E8 register.

During field offset measuring lines, the value applied to the DACs for each channel are given by MVR[7:0] for red, MVG[7:0] for green, MVB[7:0] for blue in register E8

The manual measuring line mode is enabled using the MLE bit in the D5 register.

MLE	0: Manual measuring line disabled 1: Manual measuring line enabled

This may be programmed when the measuring line is inserted using the MLN[8:0] bits in the D5 register.

This signal is made available on pin 75 (MLIN).

The insertion type is selected using the GOS bit in the D4 register.

GOS	0: Field offset canceller 1: Gain compensation

The direction is selected by the HVM bit in the D4 register.

HVM	0 = Vertical 1 = Horizontal

9.7.3 Gain Cursor Mode

See Figure 27 "Gain Cursors" on page 51.

This mode is normally used in conjunction with the corresponding video pattern. (Refer to Section 7.5 "GAIN ADJUSTMENT LINES" on page 38).

The STV2050A can generate a special convergence signal (cursor) controlled by the GCD bit in the E3 register.

GCD	0 = Cursor Off 1 = Cursor On

The cursor action is selected by the DHV bit in the E3 register.

DHV	0 = Horizontal Cursor 1 = Vertical Cursor

During the gain measuring lines:

– The dynamic values are replaced for each channel by the CRH[7:0] and CRV[7:0] bits for red, CGH[7:0] and CGV[7:0] bits for green and CBH[7:0] and CBV[7:0] for blue in the DC and DD registers for horizontal and vertical values, respectively.

– The polarity of these latter values may be changed using the PMH and PMV bits in the D5 register for horizontal and vertical values, respectively.

– The gain value is stored in the E0 register for the coarse value, but the fine values are stored in the MVR[7:0] bits for red, MVG[7:0] bits for green and MVB[7:0] bits for blue in the E8 register.

In vertical cursor mode, the resulting values applied to the DACs are first positive, then inverted on the following TV line. In horizontal mode, the values are inverted at each TV line.

9.7.4 Field Offset Cursor Mode

See Figure 27 "Gain Cursors" on page 51.

This mode is normally used in conjunction with the corresponding video pattern. (Refer to Section 7.5 "GAIN ADJUSTMENT LINES" on page 38.)

The STV2050A can generate a special convergence signal (cursor) controlled by the GCD bit in the E3 register.

GCD	0 = Cursor Off 1 = Cursor On

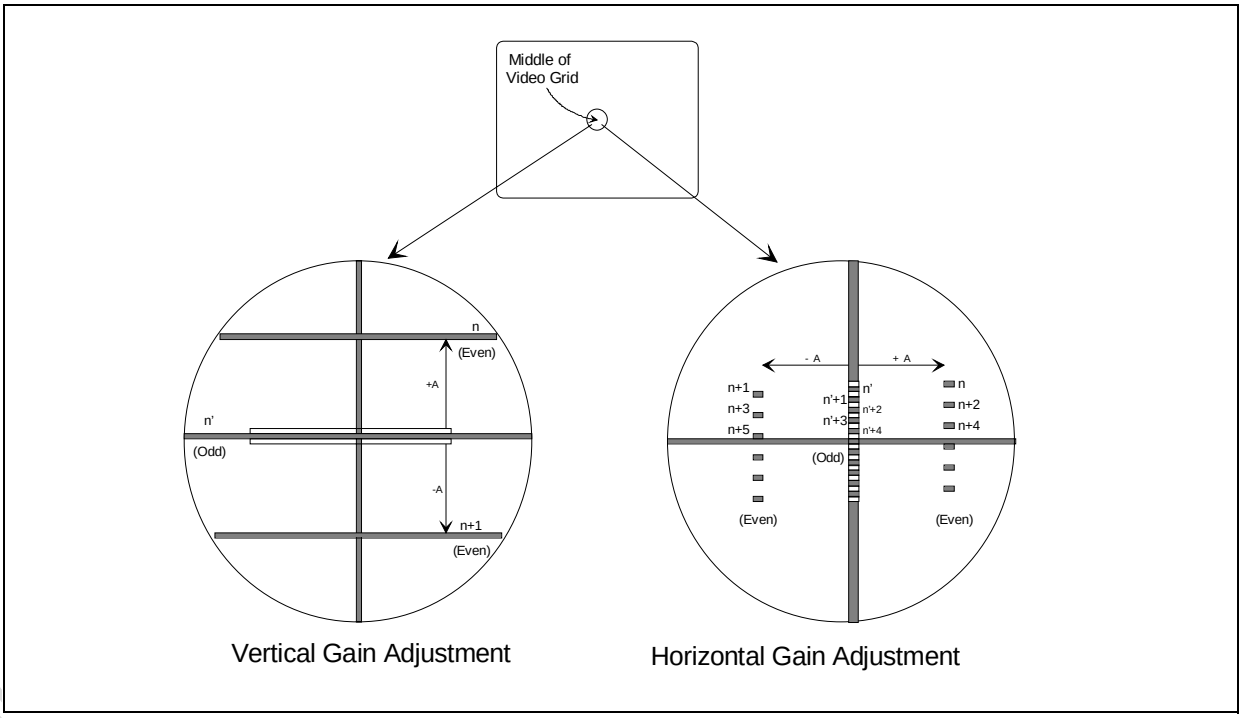
TThe cursor action is selected by the DHV bit in the E3 register.

DHV	0 = Horizontal Cursor 1 = Vertical Cursor

During field offset measuring lines, the values applied to the DACs for each channel are given by the MVR[7:0] bits for red, MVG[7:0] bits for green and MVB[7:0] bits for blue in the E8 register.

In vertical cursor mode, the resulting values applied to the DACs are first positive, then inverted on the following TV line. In horizontal mode, the values are inverted at each TV line.

Figure 27. Gain Cursors

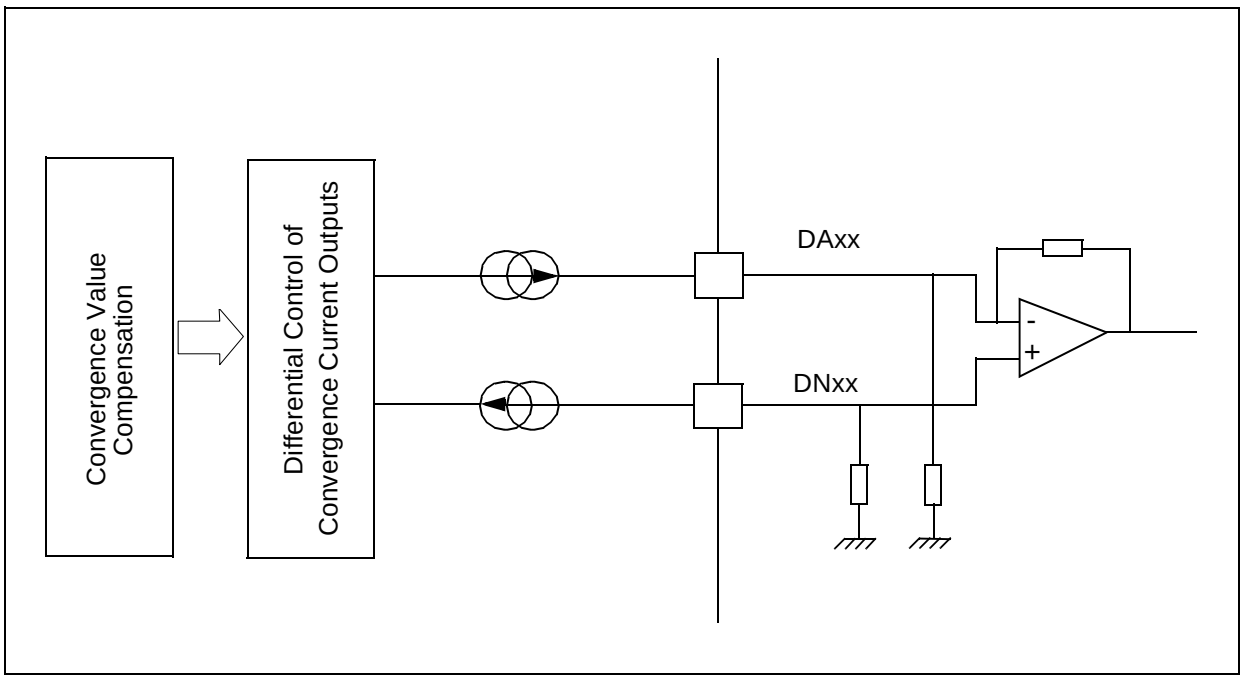


When using this mode, the STV2050A must be correctly set in order to recognize the interlaced field. The IIE bit in the DA register must be set to 1.

9.8 CONVERGENCE OUTPUTS

The values of the six convergence channels are converted by 14-bit DACs with a differential current output.

Figure 28. Convergence Channel Structure



Calibrated sources are used to generate the reference current for all CONVERGENCE and FOCUS DACs.

The reference current is defined as $\frac{Iref}{2}$. (Refer to Section 13 "CURRENT REFERENCE" on page 61.)

The outputs can be disabled using the CDO bit in the E3 register.

CDO	0: High impedance 1: Normal operation.

Notes:

1. The CDO bit is a common control for the convergence AND the focus outputs.
2. The CDN bit must be set to 1 for normal operation. Refer to Section 9.7 "MANUFACTURING, AFTER-SALES SERVICE, LAB TRIAL MODES" on page 49.

In order to perform a “soft” start of the convergence to avoid damaging the amplifiers, a “Soft Switch On” of the DACs is carried out digitally by applying a reduced digital gain (reduction by factor 2) for at least 1 field after the DACs have been switched on from high impedance to normal operation (using the CDO bit) or when the DACs have been previously switched to the offset values by the slave bus.

10 DYNAMIC FOCUS

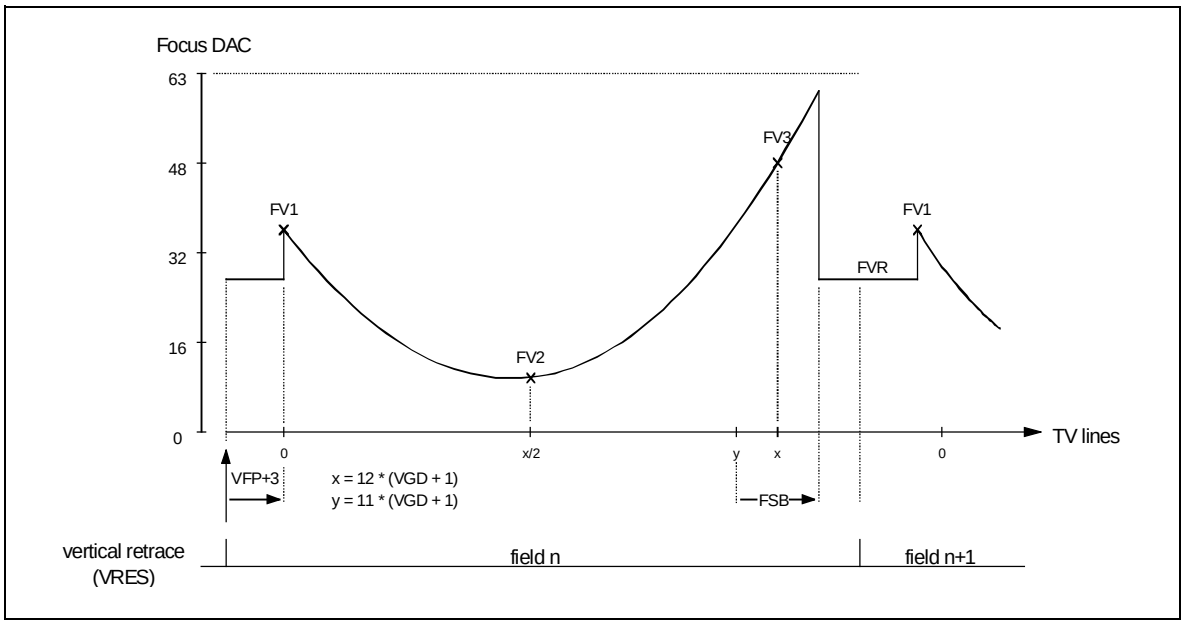
10.1 PARABOLA CURVE

The focus function delivers a current with 6-bit resolution, which is constant for horizontal lines. In vertical direction, the current has the shape of a second order parabola.

The parabola is defined by three points, FV1, FV2 and FV3, whose values correspond to the FV1[5:0], FV2[5:0] and FV3[5:0] values which are stored in the DE register.

The position of these last 3 points is a multiple of (VGD+1). See Figure 29 "Focus Parabola" on page 53. The parabola is therefore linked to the value of the Vertical Grid Distance.

Figure 29. Focus Parabola



The focus DAC will provide a programmable constant value in the FVR[5:0] bits in the DE register at the bottom of the screen and during vertical retrace.

The start of the retrace value is programmable using the FSB[7:0] bits in the DA register as shown above.

The position is indicated by the VFP[8:0] bits in the D9 register.

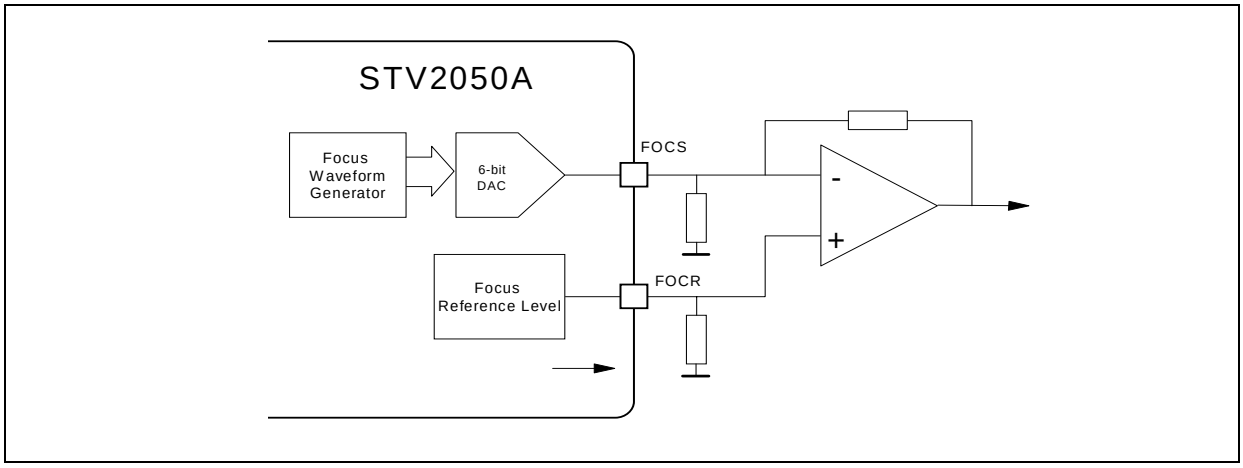
Notes:

1. If VRES becomes active before the number of lines for the FSB have been counted, the parabola will be terminated and replaced by the FVR retrace value.
2. The hardware is not equipped with a safeguard device against DAC range overflow. This may occur if the FV2 bit is near the max. positive or negative value and the parabola is not symmetrical to the FV2 centre value. Also, large values for the FSB have to be taken into account.

10.2 FOCUS OUTPUTS

The focus output signal is delivered on the FOCS pin. This output is normally used together with a static reference generated on the FOCR pin. This static reference corresponds to the mid-range code value.

Figure 30. Focus Outputs



11 ELECTRICAL LOOP

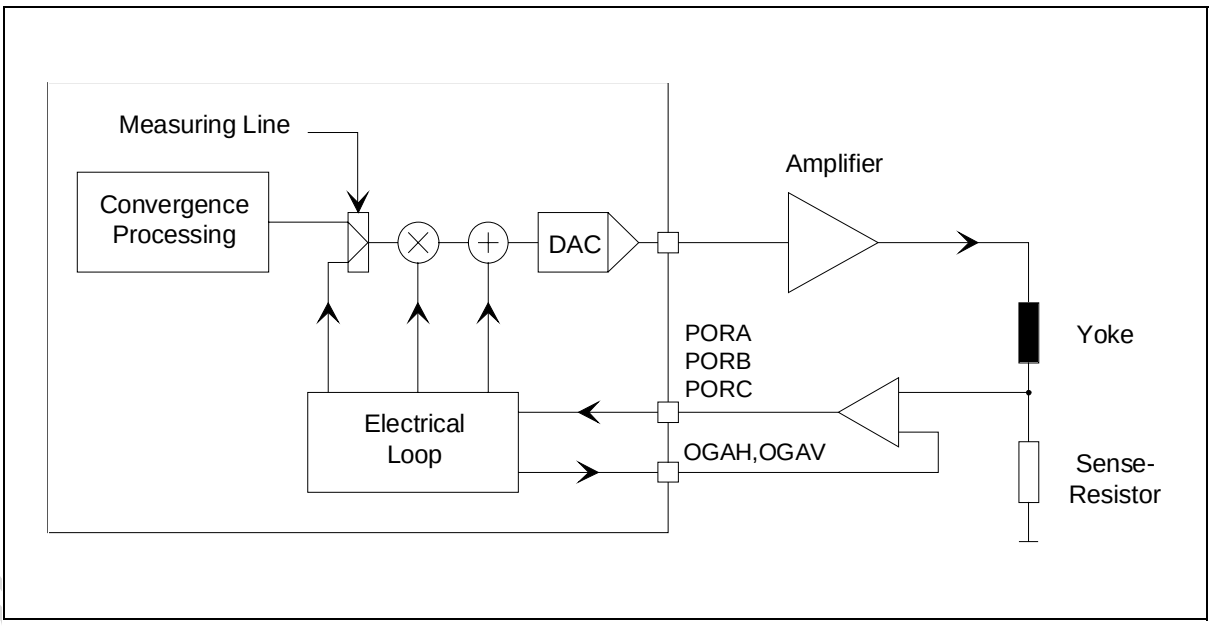
11.1 PRINCIPLE OF OPERATION

It is possible to multiply convergence values with a digital gain value and add a digital offset value to the convergence values during convergence signal processing (see Figure 26 "Convergence Values Computation Path" on page 45). This can be used to compensate offset current and gain differences of the external convergence amplifiers. However, aging and temperature can cause drifting, and the correction values may have to be adjusted. In order to avoid a manual after-sales re-alignment, the STV2050A can perform an automatic update of the field offset canceller values, as well as for the gain correction values.

For this purpose a measuring line in the invisible part of the picture (for example, during the frame retrace procedure) can be used to provide measurement values at convergence outputs. (Refer to Figure 31 "Electrical Loop Block Diagram" on page 55.)

Offset current and gain values of the amplifiers are measured with comparators, which are connected to the PORA, PORB, PORC port pins of the IC. The reference values are available on the OGAH and OGAV pins.

Figure 31. Electrical Loop Block Diagram



Once the measurement is carried out, the convenient field offset canceller and gain compensation corrections for the convergence values can be controlled by either an embedded process (“internal loop”), or by an external MCU, when the internal loop is disabled.

The loop is activated using the STL bit in the E3 register.

STL	0 = Internal Loop enabled 1 = Internal Loop disabled

A measuring line is inserted in each frame for measuring either the offset or the gain of the amplifiers. Therefore, the compensation procedure has to run through the offset/gain measurement and horizontal/vertical channels sequentially. The right comparator is activated by the timing of the signals on the OGAV and OGAH pins. (Refer to Figure "" on page 8).

Programming is possible when the measuring line is inserted using the MLN[8:0] bits in the D5 register.

11.2 LOOP PARAMETER REGISTER

Parameters for the internal loop circuit are defined in the DF register.

Offset and gain compensation can be enabled separately using the OLE and GLE bits.

OLE	0 = Offset Loop activated 1 = Offset Loop disabled
GLE	0 = Gain Loop activated 1 = Gail Loop disabled

If the FIN bit in the DF register is ‘high’, the device only carries out one single measurement during the first time that the compensation is carried out.

FIN	0: No exception for first loop cycle 1: First loop cycle with fixed parameters for fast operation

The comparison sign of the PORA, PORB and PORC pins can be programmed by using the DIO bit for the offset and the DIG bit for the gain in the DF register.

DIG	0: The level on the port is ‘high’ if the convergence current is too high 1: The level on the port is ‘low’ if the convergence current is too high.

The number of measurements that are evaluated for selecting a new compensation value is determined by the NOM[7:0] bits in the DF register.

Number of deviating results among the NOM measurements that do not lead to a change of the actual compensation value is determined by the TOL[7:0] bits in the DF register.

11.3 LOOP STATUS REGISTER

All functions for the port control and the gain range control that are influenced by the compensation loop are available via the I²C E4 register. This register is used if the gain and/or offset loop is handled by an external MCU. The IC internal loop has its own registers which are mapped to the E4 address in the event of read access to this address.

– The PIA, PIB and PIC bits indicate the status of the PORA, PORB and PORC ports respectively.

– The ELO bit indicates if the electrical loop is ready (=1) or not (=0).

11.4 OPERATION OF THE ELECTRICAL LOOP

The electrical loop is started by the STV2050A reset procedure following the readout of the EEPROM and the updating of the IC registers once the convergence outputs are enabled (the S02 and S03 bits in the E3 register are set to 1).

If loop operation is enabled with the OLE and GLE bits, the loop sets the RU1 and RU2 bits to Low in the EF register which disables the RAM updating the D0*...D3* and E4 registers.

The **ELO** bit in the E4 register is set to High by the IC reset, which indicates to external MCUs that the first offset/gain compensation is not yet completed.

If enabled, the offset and the gain compensation procedures are repeated endlessly. If the offset compensation is enabled by the OLE bit, the measuring line is switched to offset mode (GOS = 0) and the compensation procedure is done sequentially for horizontal (HVM=1) and vertical (HVM=0) channels.

If the gain compensation is enabled by the GLE bit, the measuring line is switched to gain mode (GOS=1) and the compensation procedure is carried out for horizontal (HVM=1) and vertical (HVM=0) channels.

When the compensation for all channels is completed for the first time, the ELO bit is set to Low in order to supply this information to external MCUs.

The activity of the internal loop circuit has to be interrupted if the convergence DACs are disabled (which can be detected at the S02 and S03 bits) or if the STL bit in the E3 register is High or if the GLE and the OLE bits are Low.

11.5 OUTPUT/INPUT PADS

5 pins are dedicated for the electrical loop: PORA, PORB, PORC, OGAH and OGAV.

However, these pins can be used for other purposes and are all programmable.

11.5.1 PORA, PORB and PORC Pins

These pins can be set as either input or output pins using the corresponding PDA, PDB and PDC bits in the E4 register.

PDA, PDB or PDC	0 = Input 1 = Output

If the ports are set as an input, the value on the port is sampled with the timing set by the PLT bit in the E4 register.

PLT	0: by the system clock 1: at the end of the measuring line

If the ports are set as an output, the value on the port is given by the value of the POA, POB or POC bits in the E4 register.

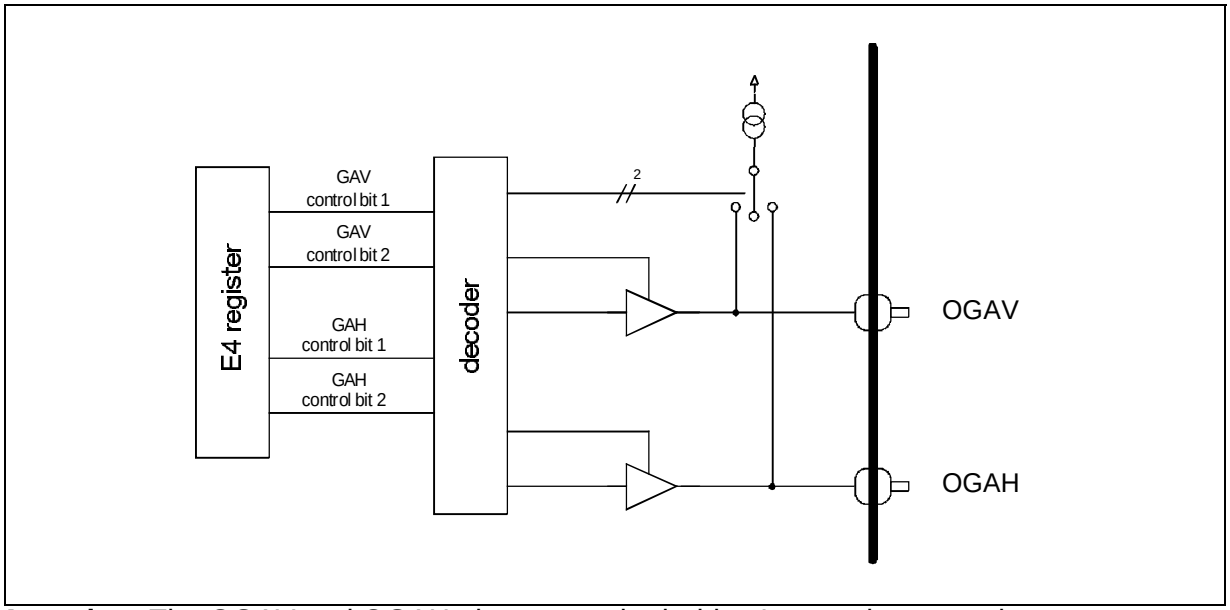
11.5.2 OGAH and OGAV Pins

The OGAH (pin 57) and OGAV (pin 58) pins are multi-level output pins. In addition to the normal digital output function (logical “0” and “1”), they can drive a very stable current and can be switched to high impedance. The stable current and the high impedance can be used to generate the reference voltage across a grounded resistor for the gain and offset detection comparators.

Each pad is controlled by two corresponding bits in the E4 register.

GAH[1:0]	0 0 = High impedance 0 1 = “0” 1 0 = Iref 1 1 = “1”
GAV[1:0]	0 0 = High impedance 0 1 = “0” 1 0 = Iref 1 1 = “1”

Figure 32. E4 Register

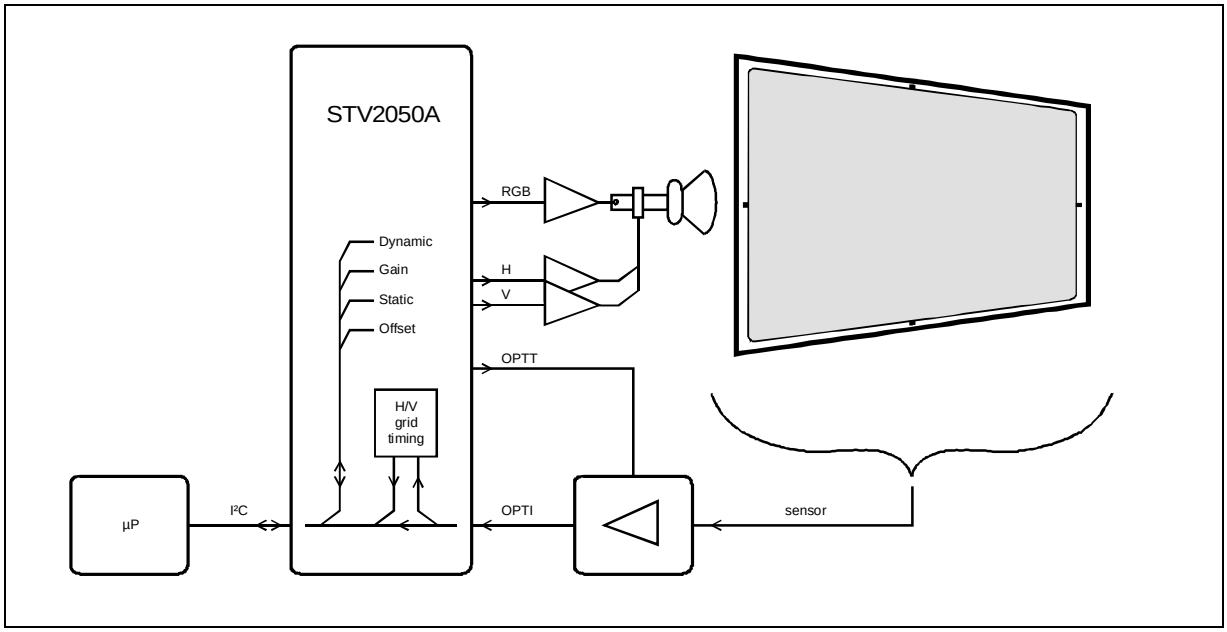


Attention: The OGAV and OGAH pins cannot both drive I_{REF} at the same time.

12 OPTICAL LOOP

12.1 PRINCIPAL OF OPERATION

Figure 33. Optical Loop



The STV2050A can deliver a dedicated video pattern known as an “auto-alignment pattern”. This pattern is rectangular-shaped, and its width, height and brightness are programmable. Refer to Section 7.6 "Auto-alignment Pattern" on page 40.

The presence or absence of this pattern can be detected by optical sensors; for example, by a camera in the production line, or photo detector diodes placed around the Projection screen.

The STV2050A can read the status of the sensors within a programmable time limit. The results are made available in the E5 register, allowing the MCU to run a routine for making the necessary corrections.

Two pins are dedicated to the optical loop:

– The OPPT pin is a port normally used as an output, and can deliver a logical electrical signal with a programmable time limit.

– The OPTI pin is an input port for logical 0 or 1 levels. This port is sampled by the STV2050A to indicate the status of the sensor.

12.2 OPTT SENSOR PORT CONTROL

The OPTT sensor port can be programmed as an input or as an output by the ODS in the E5 register.

ODS	0 = OPTT is an input 1 = OPTT is an output

12.2.1 OPTT Pin used as an Input

The status of OPTT is available in S05 in register E5.

S05	0: < 0.7 V on OPTT 1: > 2.6 V on OPTT

12.2.2 OPTT Pin used as an Output

The OPTT output can either be forced to the electrical “1” level, or can be programmed in the same way as the auto-alignment pattern. This is carried out by the OOS bit in the E5 register.

OOS	0: Data output = the ODT bit in the E5 register 1: Programmable timing

In the latter case, the timing of the OPPT signal typically overlaps the auto-alignment pattern. The final signal is used to control the OPTI and OPTT port functions. The timing for the signal is defined by the ED and EE registers.

HG3	Grid number of horizontal start
HO3	Offset of horizontal start (number of clock cycles, 1 grid max.)
HG4	Grid number of horizontal end
HO4	Offset of horizontal end (number of clock cycles, 1 grid max.)
VG3	Grid number of vertical start
VO3	Offset of vertical start (number of video lines, 1 grid max.)
VG4	Grid number of vertical end
VO4	Offset of vertical end (number of video lines, 1 grid max.)

Offset values larger than one grid distance or invalid vertical grid numbers for start or stop position will cause unexpected results at the OPTT_PATTERN signal.

The OPTT_PATTERN signal is not influenced by the horizontal or vertical blanking function.

12.3 OPTI SENSOR STATUS PORT

The level applied to the OPTI pin can be read using the S11 bit in the E5 register.

The OPTI level can be ANDed with the window defined on the OPTT using the OPI in the E5 register.

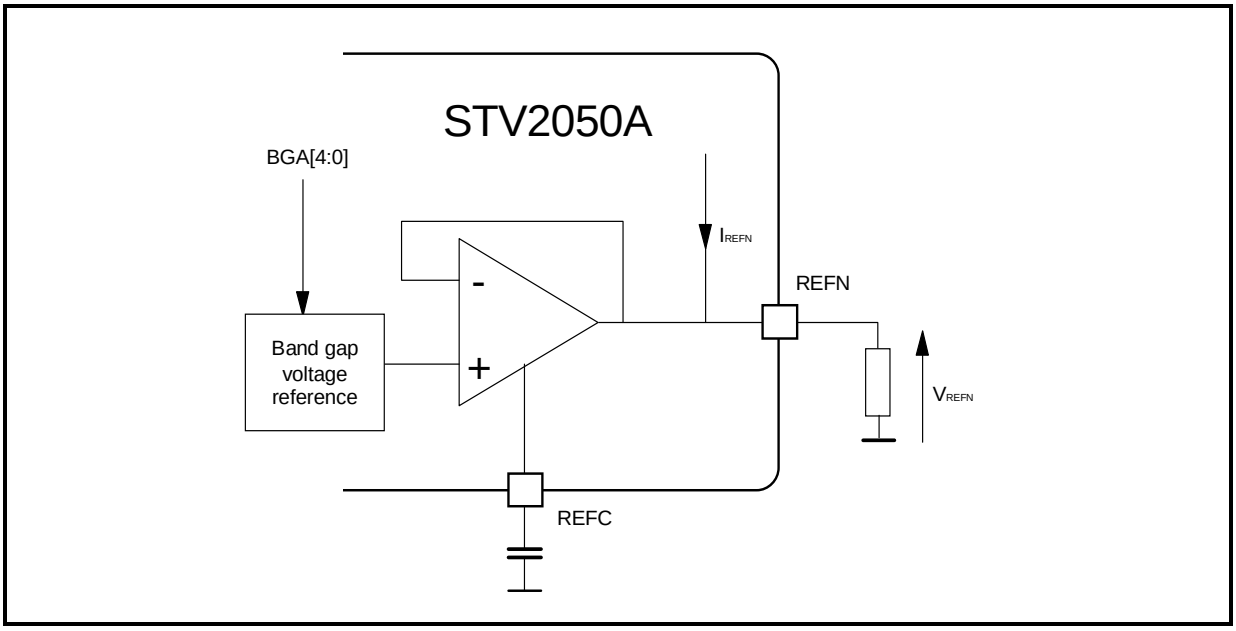
OPI	0: S11 = OPTI AND window 1: No windowing

13 CURRENT REFERENCE

The STV2050A delivers accurate and stabilized currents used to drive the convergence and focus functions. It has an embedded voltage reference (band gap), which is used to generate a reference current (I_{refN})

The nominal voltage on the REFN pin is 500 mV. The Irefn current must be adjusted to 500 uA. This is obtained by using a temperature stable external resistor of 1 kΩ. The reference voltage may be adjusted by using the BGA[4:0] bits in the D5 register.

Figure 34. Current and Voltage References



14 SECURITIES

14.1 OVERVIEW

The STV2050A can prevent overcurrents in the convergence coils, or poor programming, using the following controls:

– At power-on reset, or after a reset, all analog outputs are disabled, and the STV2050A waits until at least 2 pulses of each horizontal and vertical signals are received.

– As long as the internal set-up is not achieved, the outputs remain disabled. The setup duration is typically 2 field periods.

– When setup is achieved, the DAC outputs are not fully released and the values are reduced 50% during one field.

– The transfer between EEPROM and embedded RAM of the data stored in register E9 is protected by a Hamming code.

– During normal operating mode, each convergence value stored in the embedded RAM is checked by a parity checker before it is applied to the DACs. If a parity error occurs, the S19 bit in the E3, E4, E5 and E9 resisters are set as follows.

S19	0: Parity OK 1: Parity error

An error flag is available in read mode through the slave I²C BUS.

14.2 HAMMING ENCODING

The E9 register contains certain values which are protected by a Hamming code: :EEPROMadd[2:0], ADS[1:0] and RWM[2:0]. The Hamming code is stored in the HAM[3:0] bits in the E9 register.

	MSB															LSB							
	D0 BYTE								D1 BYTE								D2 BYTE							
ADD	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
E9	EEPRO-Madd [2:0]			X	X	X	ADS[1:0]		RWM [2:0]			X	HAM[3:0]				X	X	X	X	X	X	X	X

To initiate access to an EEPROM, the MCU must generate this code. A simple method is to store the values in a single temporary byte TMP[7:0] and to compute each bit of the Hamming HAM[3:0] bits as follows:

MSB							LSB
TMP BYTE							
7	6	5	4	3	2	1	0
EEPROMadd [2:0]			ADS[1:0]		RWM [2:0]		

HAM[0] = TMP[4] XOR TMP[3] XOR TMP[2] XOR TMP[1] XOR TMP[0]

HAM[1] = TMP[6] XOR TMP[5] XOR TMP[4] XOR TMP[2] XOR TMP[0]

HAM[2] = TMP[7] XOR TMP[5] XOR TMP[2] XOR TMP[1]

HAM[3] = TMP[7] XOR TMP[6] XOR TMP[4] XOR TMP[3]

14.3 SECURITY OUTPUT

The POUT output can be considered as an open drain from a functional point of view, that is to say that it can have two electrical states: high impedance or pull-down to the ground.

It can be used, for example, to force all external amplifiers to a secured biasing. Refer to Figure "" on page 8.

The electrical status of this output is controlled by the PPL bit in the E3 register.

PPL	0: Normal operation 1: High impedance

During normal operation it is pulled down to ground:

– if the STV2050A detects a malfunction such as a parity check error or power on reset error.

– until the power-on reset is released.

Otherwise, POUT is set to high impedance. In this case, the logical status of the POUT pin can be read using the S02 bit in the E3 register.

15 BOOT SEQUENCE

At startup, or following a reset on pin 13, the STV2050A will:

– Immediately disable all the outputs (forced to the “zero current” value, in order to protect the application against over-currents in the coils for example),

– Wait until the HSYNC and VSYNC signals are available on pins 27 and 28 respectively. (At least 2 VSYNC pulses are required). If one signal is missing, the STV2050A remains in Stand-by mode.

– Use the I²C master to read the EEPROMadd[2:0] data bits in the EEPROM having the hardware address 010 (bin). The EEPROMadd[2:0] bits represent the address of the EEPROM which will be used to setup the STV2050A during the boot sequence,

Note: This is particularly suitable when it is necessary to recover the last configuration used before switching off for example.

– Use the I²C master to download all convergence data and registers (from the selected EEPROM, as explained before),

– Wait for up to 2 fields after all the data has been downloaded and enable the outputs.

16 IC STATUS REGISTERS

Some registers of the STV2050A can be read via the I²C slave bus in order to indicate the updated status of the IC. The update is enabled using the RUE bit in the EF register.

RUE	0: No update 1: Update enabled

The update timing of registers D0 to D3 is determined by the RU1 bit in the EF register.

RU1	0: No update 1: Update after vertical reset

The update timing of the E4 register is determined by the RU2 bit in the EF register.

RU2	0: No update 1: Update after vertical reset

The S01 bit in the E3 or E4 or E5 or E9 registers:

– Power-on reset status

S01	0: Reset successfully achieved 1: Reset ongoing

The S02 bit in the E3 register:

– Security output (POUT) status

S02	0: “0” (pull down to ground) 1: High impedance

17 BUS EXPANDER

The 8 digital outputs (TBU0 to TBU7) can be used as a bus expander (output only) if DTE register EF is set to "1". Each output can be set to logical “0” or “1” using the corresponding TBU[7:0] bits in the FE register.

18 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDMAX}				3.6	V
T_{AMB}	Ambient temperature operating range	10		70	°C
T_{STORE}	Storage temperature range	-25		125	°C

19 RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
P_{TOT}	Power dissipation			450	mW

20 ELECTRICAL CHARACTERISTICS

T_A= 25 °C, unless otherwise specified.

V_{DD} = 3.3 V, external components as shown in Figure 4 "Application Circuit" on page 8.

20.1 GENERAL

Parameter	Min.	Typ.	Max.	Unit	Conditions
Average current on		100		mA	

20.2 CURRENT REFERENCE

Parameter	Min.	Typ.	Max.	Unit	Conditions
Adjustable voltage range			0.45	V	BGA[4:0] = 00 (hex)
	0.55			V	BGA[4:0] = 1F (hex)
Temperature drift (10°C to 70°C)		45		I_{PPM} / °C	

20.3 VIDEO PATTERN OUTPUTS

20.3.1 DACs for RGB

Parameter	Min.	Typ.	Max.	Unit	Conditions
Resolution		4		bit	
Output voltage		70	200	mV	Code 0000b applied, I_{OUT} < 0.1 mA
	0.4	0.6	0.8	V	Code 0001b applied, I_{OUT} < 0.1 mA
	1.9	2.3	2.7	V	Code 1111b applied, I_{OUT} < 0.5 mA
DNL		±0.1	±0.25	LSB	Except code 0000b
INL		±0.2	±0.5	LSB	Except code 0000b
Matching between DACs		3	10	%	Max. code applied; Ref signal for 10% is the channel of RGB with the max signal value
Rise time (10...90%)		5	20	ns	From code 0(hex) to F(hex)
Fall time (10...90%)		2	10	ns	From code F(hex) to 0(hex)
Delay between video DACs (50%)		4		ns	

20.3.2 FBLK Output

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output voltage low			0.4	V	2 mA input
Output voltage high	2.4			V	2 mA output
Rise/Fall time (10...90%)			10	ns	15 pF load

20.4 FOCUS DACs

20.4.1 Focus Reference

Symbol	Parameter	Min	Typ	Max.	Unit	Conditions
$I_{FOCRFOCR}$	Focus reference current on pin FOCR	-7	$\frac{3}{4} \cdot I_{refn}$	+7	%	
	Temperature drift of output current		±150		I_{PPM} / °C	0°C to 70°C

20.4.2 Focus Signal

Symbol	Parameter	Min	Typ	Max.	Unit	Conditions
	Highest output current on pin FOCS	-7	$\frac{3}{2} \cdot I_{refN}$	+15	%	Max. code (3F hex) applied, V_{OUT} = 0.5 V
	Smallest output current on pin FOCS		0.5	5	µA	Min. code (00 hex) applied
	Output current matching on pin FOCS versus FOCR	-5		+5	%	Mid-code (20 hex) applied, V_{OUT} = 0.5 V
	Focus DAC DNL (FOCS pin)		± 0.2	± 0.7	LSB	
	Focus DAC INL (FOCS pin)		± 0.2	± 1	LSB	
	Operating range			1.5	V	
	Voltage Rise/Fall time (10...90%)		2		ms	1.33 kΩ, 15 pF load

20.5 CONVERGENCE DACS

Parameter	Min.	Typ.	Max.	Unit	Conditions
Resolution		14		bit	
Max. output current	-0.5	2. IrefN	+0.5	%	Max. code applied
Min. output current			1	lsb	Code 00h applied
Operating range	0	100	500	mV	
DNL		±1	± 2	LSB	Max. V_{OUT} = 100 mV
INL		± 2	± 4	LSB	Max. V_{OUT} = 100 mV
Autocalibration adjustment refresh interval			5	ms	
Horizontal line frequency	15		50	kHz	
Horizontal line retrace time	TBD		12	µs	
Internal parasitic capacitance on each DAC output			15	pF	
Signal / Noise ratio		90		dB	300 Hz to 500 kHz, df = 1 kHz Max. code (3FFF)
Temperature drift of full scale output current		35	60	| ppm / ×C |	Including bandgap temperature drift

20.6 PLL

Parameter	Min.	Typ.	Max.	Unit	Conditions
Number of System Clock pulses per line	250		512		

20.7 MASTER I²C TIME BASE

Parameter	Min.	Typ.	Max.	Unit	Conditions
SCL Frequency	65		85	kHz	Recommended filter

20.8 HORIZONTAL AND VERTICAL SYNCHRONIZATION INPUTS

Parameter	Min.	Typ.	Max.	Unit	Conditions
Threshold V_{UP}	1.4		1.8	V	
Threshold difference V_{DOWN} - V_{UP}		0.130		V	
Temperature drift of V_{UP}			90	mV	Const. supply voltage Ambient temp. 10×-70×C

20.9 TBU OUTPUTS

Parameter	Min.	Typ.	Max.	Unit	Conditions
Output voltage at low level (logical “0”)			0.4	V	2 mA input current
Output voltage at high level (logical “1”)	2.4			V	2 mA output current

20.10 ELECTRICAL LOOP PADS

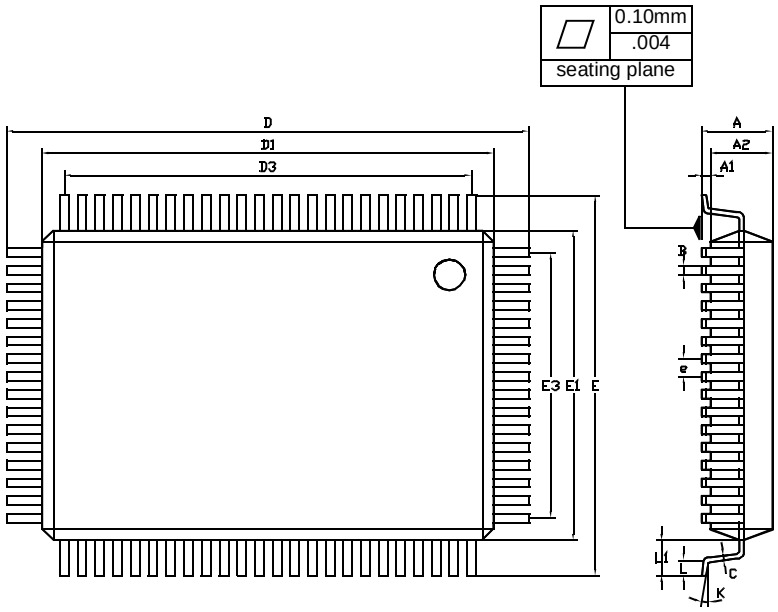
Parameter	Min.	Typ.	Max.	Unit	Conditions
Output voltage at low level (logical “0”)			0.4	V	2 mA input current
Output voltage at high level (logical “1”)	2.4			V	2 mA output current
Leakage current at high impedance			1	µA	$0 < V_{OUT} < V_{DD}$
Output current (GAH = 10 bin.)	-0.5	Irefn	+0.5	%	2 kΩ load, Max voltage = 1V
Temperature drift of Ref current			± 60	ppm /×C	2 kΩ load, including the temperature drift of the bandgap
Input logical “0”			0.7	V	
Input logical “1”	2.6			V	

Notes:

1. PORA..C Input level can be latched in measuring line or with sys. clock.
2. PORA..C and OPTT input have digital inputs.
3. OPTI is only an input pin.
4. MLIN is only an output pin. It sends a pulse during the measuring line(M_Line, see ‘gain range control’). The signal can be used to gate the comparators at the PORT A...C pins or to switch time constants.

21 PACKAGE MECHANICAL DATA

Figure 1. 80-Pin Plastic Quad Flat Package

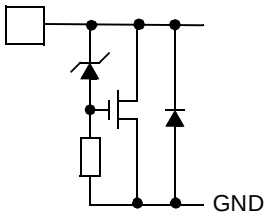


PQFP080

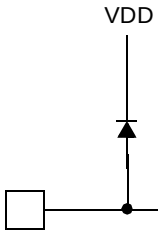
Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.40			0.724	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.80			0.031	
K	0°		7°			
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
	Number of Pins					
N	80		ND	24	NE	16

22 ELECTRICAL PIN CONFIGURATION

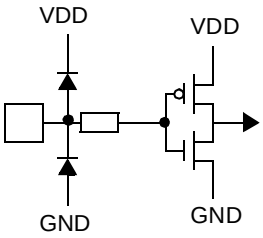
Pin	Name
19	VCCD
26	VCCF
42	VCCH
44	VCCG
50	VCCA
62	VCCB
70	VCCC



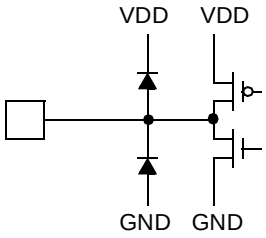
Pin	Name
41	GNDH
47	GNDA
67	GNDC



Pin	Name
8	SDAI
9	SCLS
11	TEST
13	REST
27	SYNH
28	SYNV
71	ADS0
72	OPTI

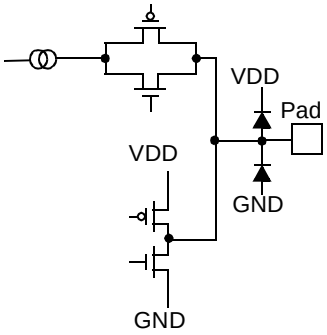


Pin	Name
7	SDAO

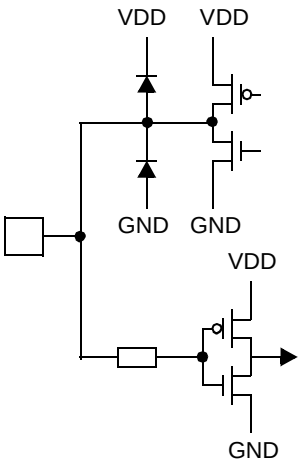


Pin	Name
54	REFN

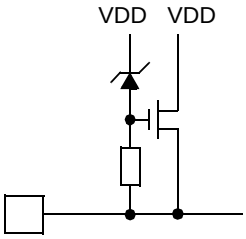
Pin	Name
57	OGAH
58	OGAV



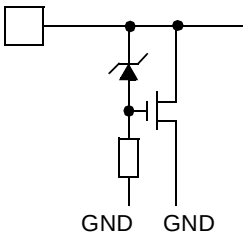
Pin	Name
1	SDAM
2	SCLM
10	VBLK
33	TBU0
34	TBU1
35	TBU2
36	TBU3
37	TBU4
38	TBU5
39	TBU6
40	TBU7
74	OPTT
75	MLIN
78	PORC
79	PORB
80	PORA



Pin	Name
3	GNDQ
15	GNDN
30	GNDL

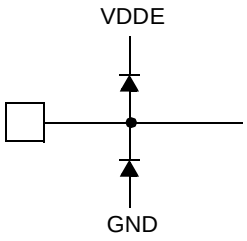


Pin	Name
5	VCCQ
6	VCCK
12	VCCN

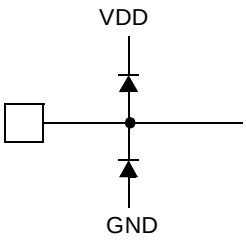


STV2050A - ELECTRICAL PIN CONFIGURATION

Pin	Name
31	VCCJ
32	VCCL
73	VCCM



Pin	Name
4	GNDK
20	GNDD
29	GNDJ
59	GNDB
76	GNDM



23 I²C BUS REGISTER VARIABLE GLOSSARY AND REGISTER LOCATION

A

B

C

D

E

F

G

H

I

M

N

O

P

R

S

T

24 INDEX OF I²C BUS REGISTERS

F

G

H

I

M

N

O

P

R

S

T

V