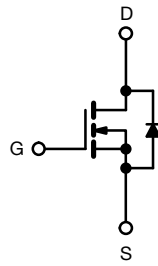
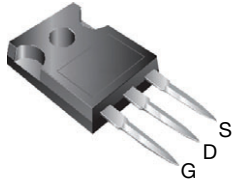


## EL Series Power MOSFET

**TO-247AC**


N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

|   |                 |      |
|---|-----------------|------|
| $V_{DS}$ (V) at $T_J$ max.              | 650             |      |
| $R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C | $V_{GS} = 10$ V | 0.53 |
| $Q_g$ max. (nC)                         | 222             |      |
| $Q_{gs}$ (nC)                           | 25              |      |
| $Q_{gd}$ (nC)                           | 36              |      |
| Configuration                           | Single          |      |

### ORDERING INFORMATION

|                                 |                  |
|---------------------------------|------------------|
| Package                         | TO-247AC         |
| Lead (Pb)-free and halogen-free | SiHG47N60AEL-GE3 |

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


| PARAMETER   | SYMBOL           | LIMIT          | UNIT |
|---|------------------|----------------|------|
| Drain-source voltage                                      | $V_{DS}$         | 600            | V    |
| Gate-source voltage                                       | $V_{GS}$         | $\pm 30$       |      |
| Continuous drain current ( $T_J = 150$ °C)                | $V_{GS}$ at 10 V | $T_C = 25$ °C  | A    |
|   |                  | $T_C = 100$ °C |      |
| Pulsed drain current <sup>a</sup>                         | $I_{DM}$         | 140            |      |
| Linear derating factor                                    |                  | 3.0            | W/°C |
| Single pulse avalanche energy <sup>b</sup>                | $E_{AS}$         | 691            | mJ   |
| Maximum power dissipation                                 | $P_D$            | 379            | W    |
| Operating junction and storage temperature range          | $T_J, T_{stg}$   | -55 to +150    | °C   |
| Reverse diode $dv/dt$ <sup>d</sup>                        | $dv/dt$          | 50             | V/ns |
| Soldering recommendations (peak temperature) <sup>c</sup> | For 10 s         | 260            | °C   |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7.0$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C



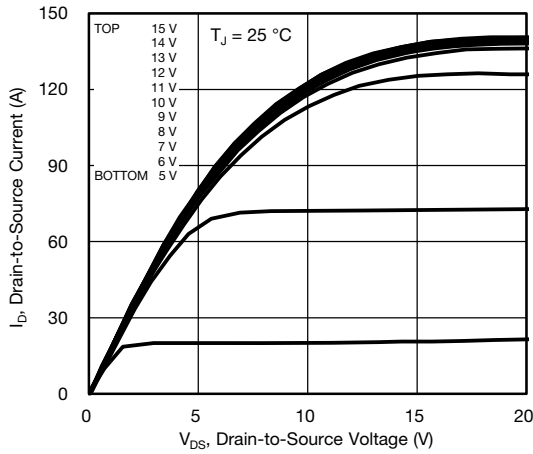
| THERMAL RESISTANCE RATINGS       |                   |      |      |      |
|----------------------------------|-------------------|------|------|------|
| PARAMETER                        | SYMBOL            | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient      | R <sub>thJA</sub> | -    | 40   | °C/W |
| Maximum junction-to-case (drain) | R <sub>thJC</sub> | -    | 0.33 |      |

| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                  |   |  |   |       |       |      |     |     |
|---|----------------------------------|---|--|---|-------|-------|------|-----|-----|
| PARAMETER   | SYMBOL                           | TEST CONDITIONS   |  | MIN.  | TYP.  | MAX.  | UNIT |     |     |
| <b>Static</b>   |                                  |   |  |   |       |       |      |     |     |
| Drain-source breakdown voltage                                  | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA  |  | 600   | -     | -     | V    |     |     |
| V <sub>DS</sub> temperature coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA   |  | -   | 0.67  | -     | V/°C |     |     |
| Gate-source threshold Voltage (N)                               | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA   |  | 2.0   | -     | 4.0   | V    |     |     |
| Gate-source leakage   | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V  |  | -   | -     | ± 100 | nA   |     |     |
|   |                                  | V <sub>GS</sub> = ± 30 V  |  | -   | -     | ± 1   | μA   |     |     |
| Zero gate voltage drain current                                 | I <sub>DSS</sub>                 | V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V  |  | -   | -     | 1     | μA   |     |     |
|   |                                  | V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C   |  | -   | -     | 10    |      |     |     |
| Drain-source on-state resistance                                | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 23.5 A                          | -   | 0.053 | 0.065 | Ω    |     |     |
| Forward transconductance <sup>a</sup>                           | g <sub>fs</sub>                  | V <sub>DS</sub> = 20 V, I <sub>D</sub> = 23.5 A   |  | -   | 29    | -     | S    |     |     |
| <b>Dynamic</b>  |                                  |   |  |   |       |       |      |     |     |
| Input capacitance   | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 100 V,<br>f = 1 MHz   |  | -   | 4600  | -     | pF   |     |     |
| Output capacitance  | C <sub>oss</sub>                 |   |  | -   | 186   | -     |      |     |     |
| Reverse transfer capacitance                                    | C <sub>rss</sub>                 |   |  | -   | 7     | -     |      |     |     |
| Effective output capacitance, energy related <sup>a</sup>       | C <sub>o(er)</sub>               |   |  | V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V |       | -     |      | 121 | -   |
| Effective output capacitance, time related <sup>b</sup>         | C <sub>o(tr)</sub>               |   |  | V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V |       | -     |      | 635 | -   |
| Total gate charge   | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V  | I <sub>D</sub> = 23.5 A, V <sub>DS</sub> = 480 V | -   | 111   | 222   | nC   |     |     |
| Gate-source charge  | Q <sub>gs</sub>                  |   |  | -   | 25    | -     |      |     |     |
| Gate-drain charge   | Q <sub>gd</sub>                  |   |  | -   | 36    | -     |      |     |     |
| Turn-on delay time  | t <sub>d(on)</sub>               | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 23.5 A,<br>V <sub>GS</sub> = 10 V, R <sub>g</sub> = 22 Ω  |  | -   | 55    | 110   | ns   |     |     |
| Rise time   | t <sub>r</sub>                   |   |  | -   | 65    | 130   |      |     |     |
| Turn-off delay time   | t <sub>d(off)</sub>              |   |  | -   | 267   | 534   |      |     |     |
| Fall time   | t <sub>f</sub>                   |   |  | -   | 71    | 142   |      |     |     |
| Gate input resistance   | R <sub>g</sub>                   |   |  | f = 1 MHz, open drain                                 |       | 0.3   |      | 0.7 | 1.4 |
| <b>Drain-Source Body Diode Characteristics</b>                  |                                  |   |  |   |       |       |      |     |     |
| Continuous source-drain diode current                           | I <sub>S</sub>                   | MOSFET symbol showing the integral reverse p - n junction diode  |  | -   | -     | 47    | A    |     |     |
| Pulsed diode forward current                                    | I <sub>SM</sub>                  |   |  | -   | -     | 140   |      |     |     |
| Diode forward voltage   | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 23.5 A, V <sub>GS</sub> = 0 V  |  | -   | -     | 1.2   | V    |     |     |
| Reverse recovery time   | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 23.5 A,<br>di/dt = 100 A/μs, V <sub>R</sub> = 400 V   |  | -   | 437   | 874   | ns   |     |     |
| Reverse recovery charge   | Q <sub>rr</sub>                  |   |  | -   | 8.6   | 17.2  | μC   |     |     |
| Reverse recovery current  | I <sub>RRM</sub>                 |   |  | -   | 37    | -     | A    |     |     |

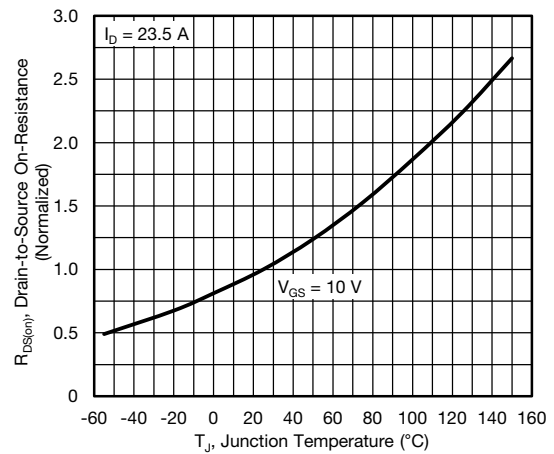
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>

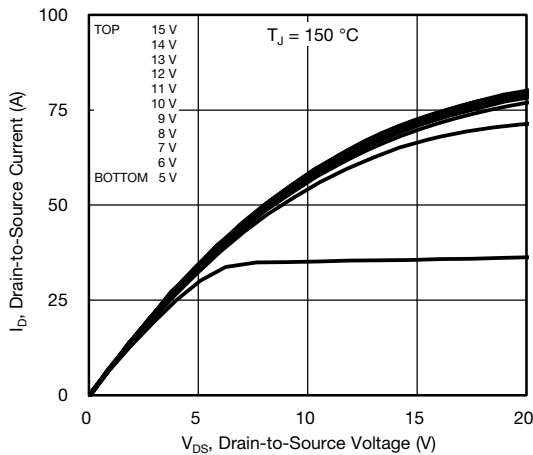
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



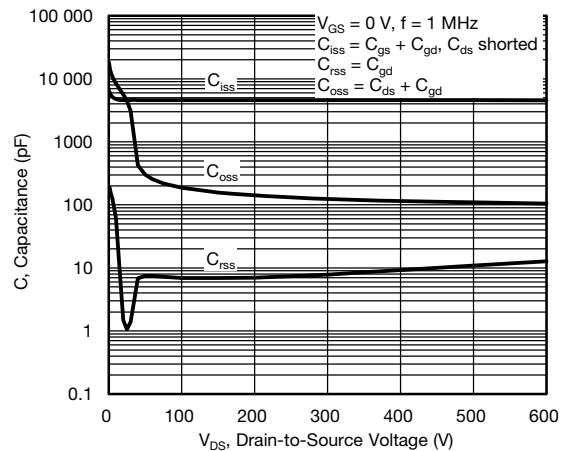
**Fig. 1 - Typical Output Characteristics**



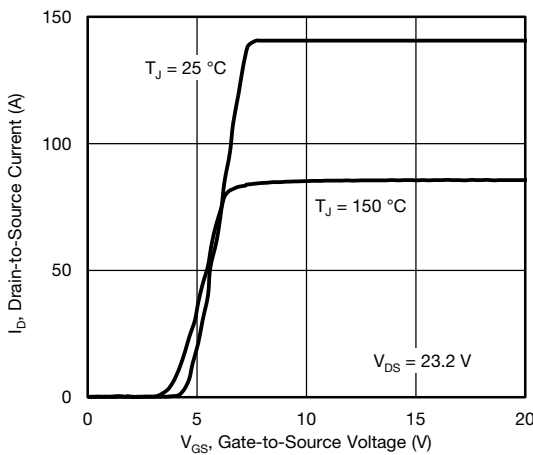
**Fig. 4 - Normalized On-Resistance vs. Temperature**



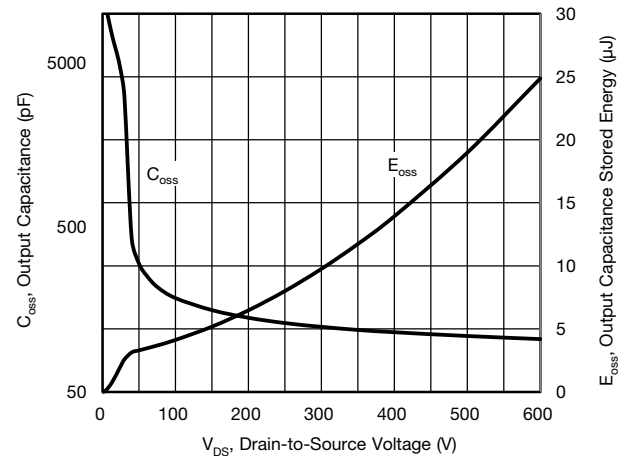
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

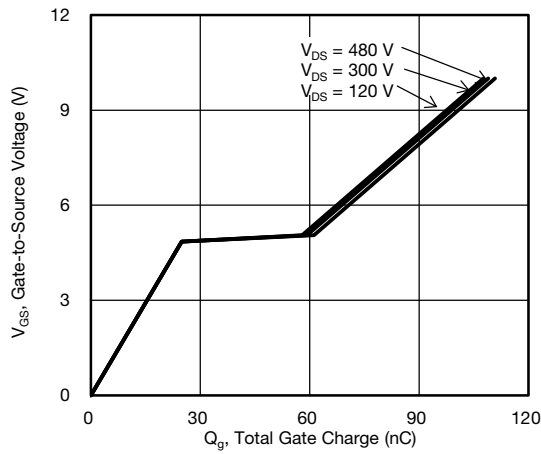


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

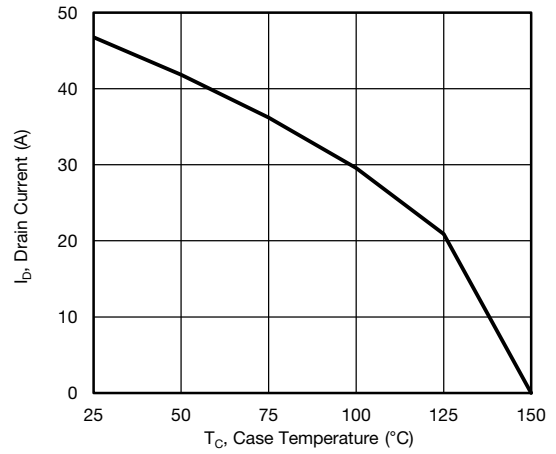


Fig. 10 - Maximum Drain Current vs. Case Temperature

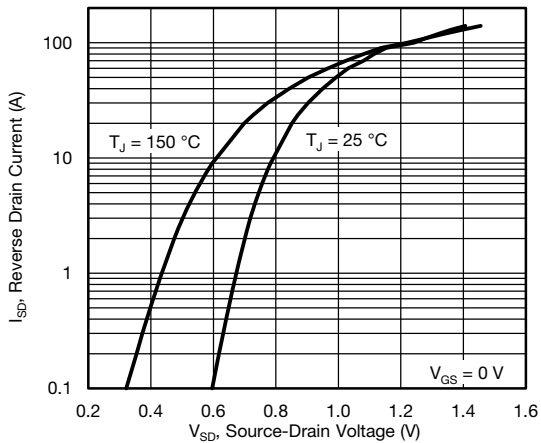


Fig. 8 - Typical Source-Drain Diode Forward Voltage

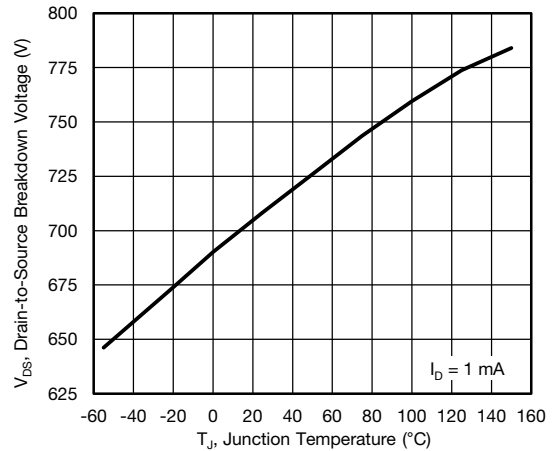


Fig. 11 - Temperature vs. Drain-to-Source Voltage

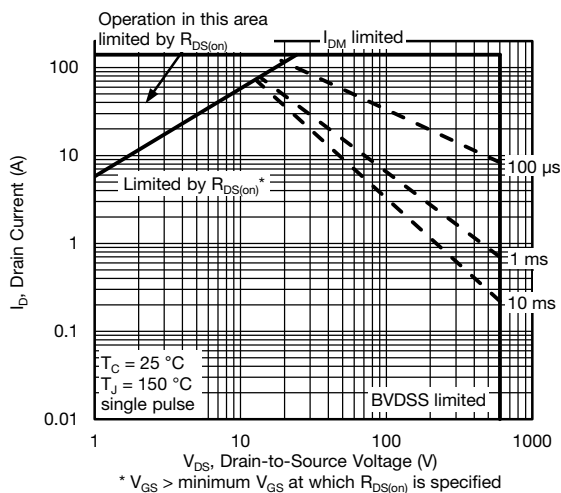


Fig. 9 - Maximum Safe Operating Area

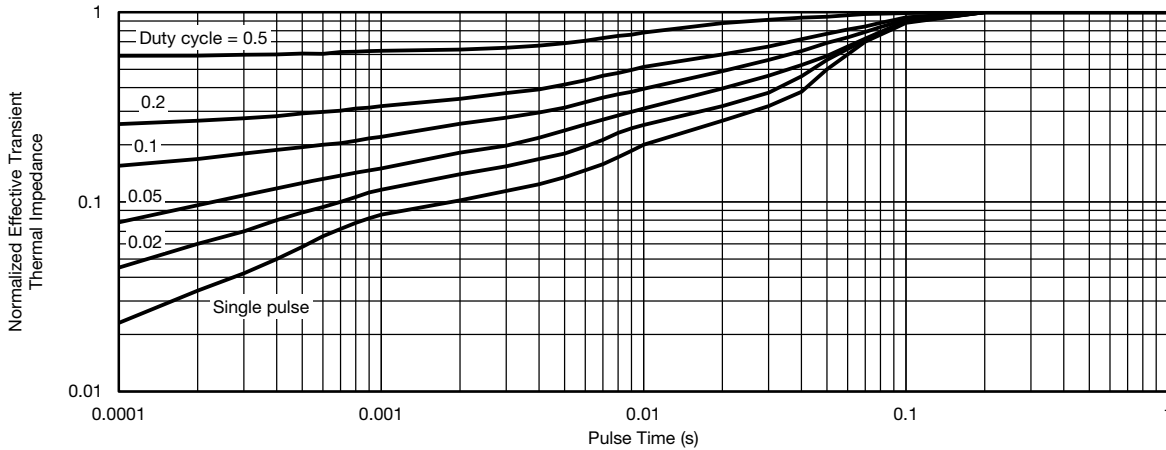


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms

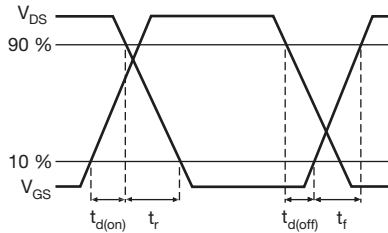


Fig. 14 - Switching Time Waveforms

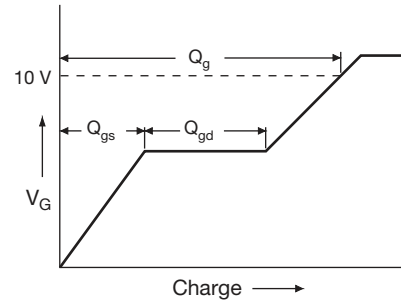


Fig. 17 - Basic Gate Charge Waveform



Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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