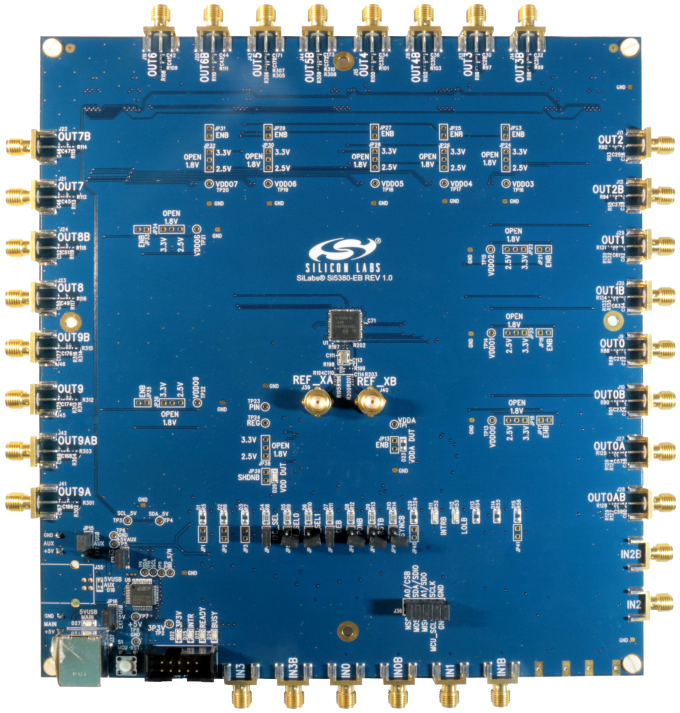
Si5380 Evaluation Board User's Guide

The Si5380-EVB is used for evaluating the Ultra Low Jitter, Any-Frequency, 12-output JESD204B Clock Generator. The Si5380 employs 4th generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5380-EVB has four independent input clocks and a total of 12 outputs. The Si5380-EVB can be easily controlled and configured using Silicon Labs' Clock Builder Pro™ (CBPro™) software tool.

EVB FEATURES

- Powered from USB port or external power supply
- Onboard 54 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5380
- CBPro™ GUI programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V
- CBPro™ GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro™ GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5380
- SMA connectors for input clocks, output clocks and optional external timing reference clock



1. Si5380 Functional Block Diagram

Below is a functional block diagram of the Si5380-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 6.1 Installing ClockBuilderPro (CBPro) Desktop Software for more information.

Note: All Si5380 schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/si538x-4x-evb

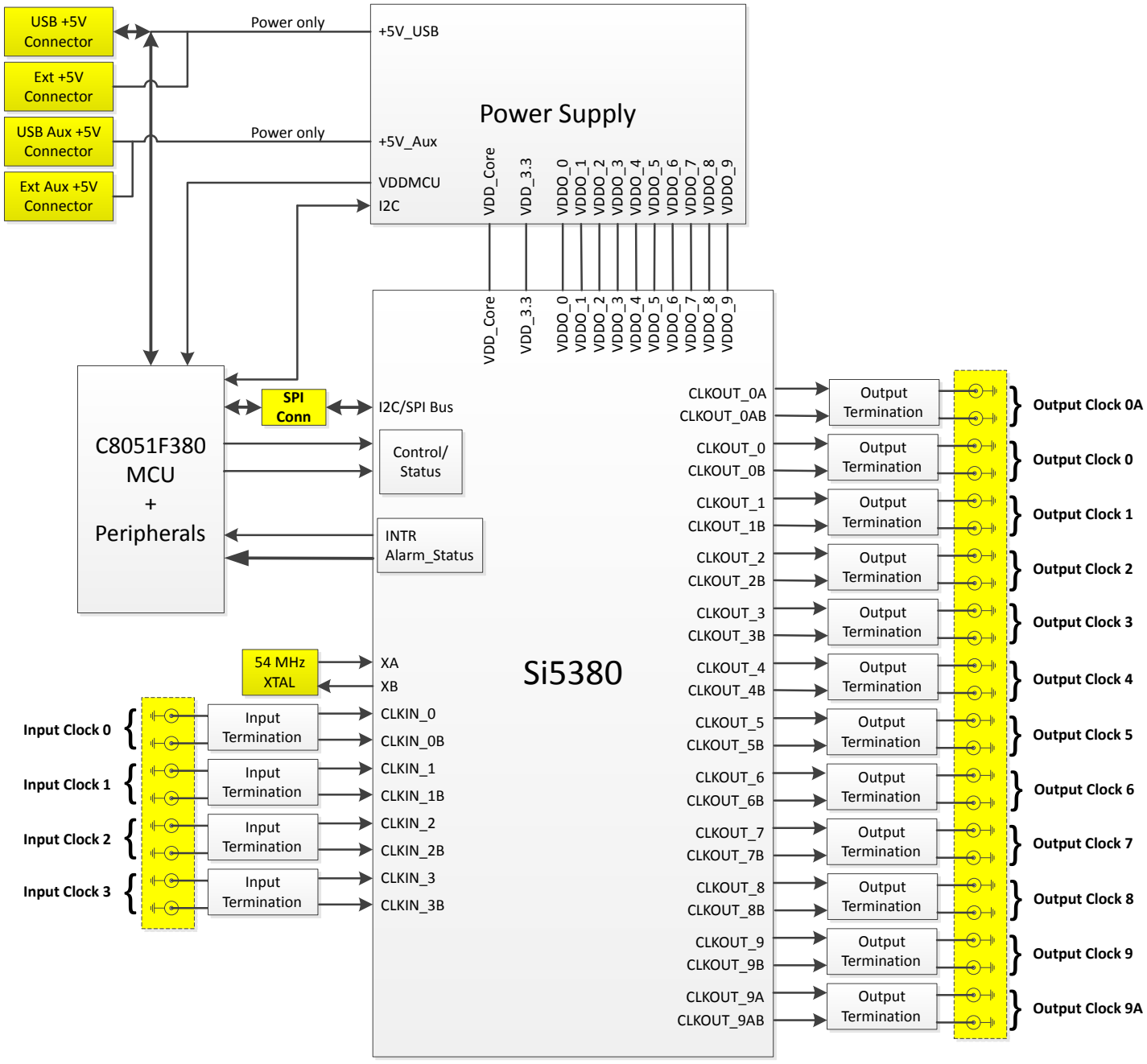


Figure 1.1. Functional Block Diagram of Si5380-EVB

2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilderPro software.

1. Install ClockBuilderPro desktop software. http://www.silabs.com/CBPro
2. Connect a USB cable from the Si5380-EVB to the PC where the software was installed.
3. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
4. You can use ClockBuilderPro to create, download, and verify a frequency plan on the Si5380-EVB.
5. For the Si5380 data sheet, go to: http://www.silabs.com/timing and search for Si5380 datasheet.

The following table lists the Si5380 EVB jumper defaults.

Table 2.1. Si5380 EVB Jumper Defaults*

Location	Type	I = Installed O= Open	Location	Type	I = Installed O= Open
JP1	2 pin	O	JP23	2 pin	O
JP2	2 pin	O	JP24	3 pin	all open
JP3	2 pin	O	JP25	2 pin	O
JP4	2 pin	I	JP26	3 pin	all open
JP5	2 pin	O	JP27	2 pin	O
JP6	2 pin	O	JP28	3 pin	all open
JP7	2 pin	I	JP29	2 pin	O
JP8	2 pin	O	JP30	3 pin	all open
JP9	2 pin	O	JP31	2 pin	O
JP10	2 pin	O	JP32	3 pin	all open
JP13	2 pin	O	JP33	2 pin	O
JP14	2 pin	I	JP34	3 pin	all open
JP15	3 pin	1 to 2	JP35	2 pin	O
JP16	3 pin	1 to 2	JP36	3 pin	all open
JP17	2 pin	O	JP39	2 pin	O
JP18	3 pin	all open	JP40	2 pin	O
JP19	2 pin	O	JP41	2 pin	O
JP20	3 pin	all open			
JP21	2 pin	O			
JP22	3 pin	all open	J36	5x2 Hdr	All 5 installed

Note: Refer to the Si5380-EVB schematics for the functionality associated with each jumper.

3. Status LEDs

Table 3.1. Si5380 EVB Status LEDs

Location	Silkscreen	Color	Status Function Indication
D11	INTRB	Blue	DUT Interrupt Active
D12	LOLB	Blue	DUT Loss of Lock Indicator
D21	READY	Green	MCU Ready
D22	3P3V	Blue	DUT +3.3 V is present
D24	BUSY	Green	MCU Busy
D25	INTR	Red	MCU Interrupt active
D26	VDD DUT	Blue	DUT VDD voltage present
D27	5VUSBMAIN	Blue	Main USB +5 V present

D27, D22, and D26 are illuminated when USB +5 V, Si5380 +3.3 V, and Si5380 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.

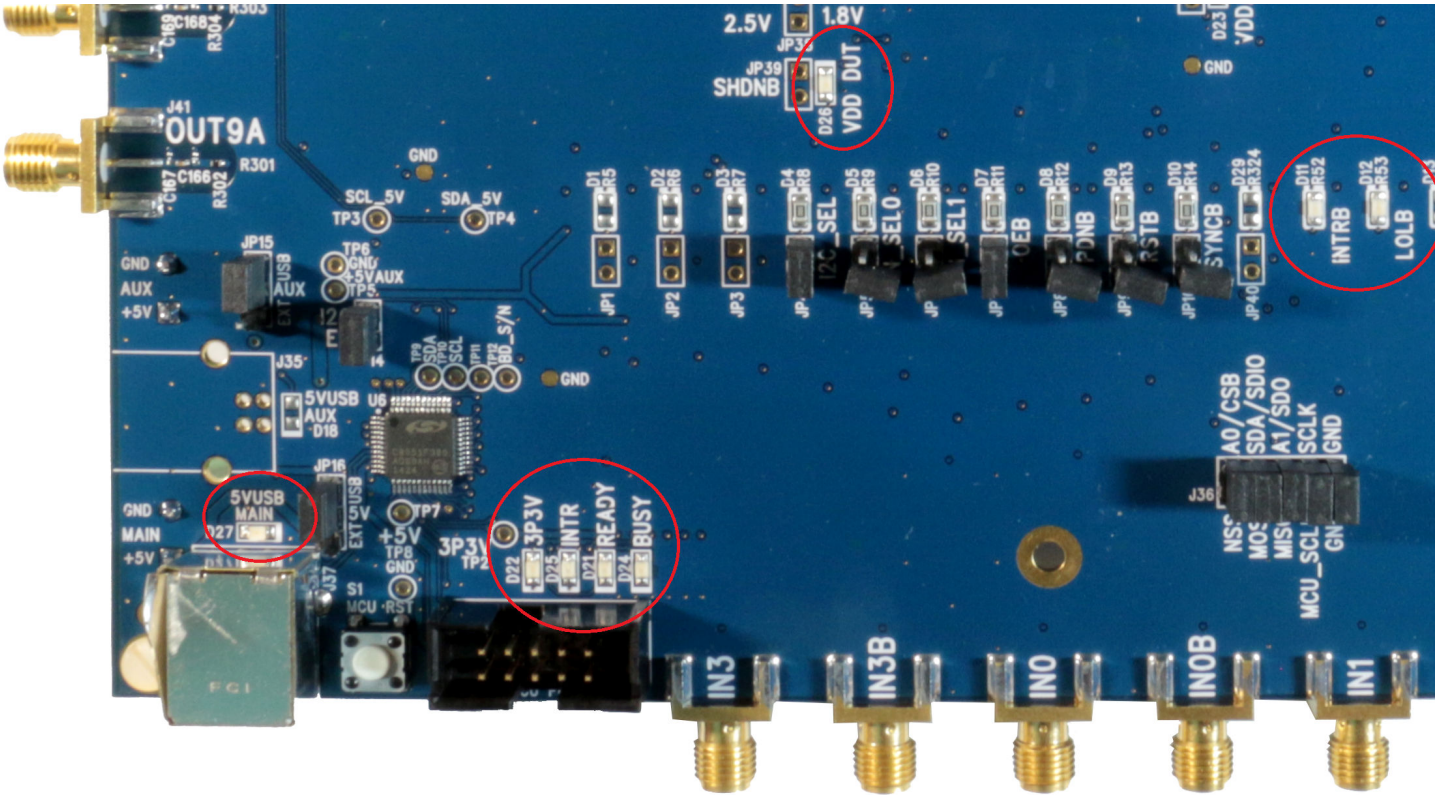


Figure 3.1. Status LEDs

4. External Reference Input (XA/XB)

An external reference (XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5380-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with a REFCLK, C111 and C113 must be populated and the XTAL removed (see figure below). The REFCLK can then be applied to J39 and J40.
Note: The remaining components marked "NI" are not installed.

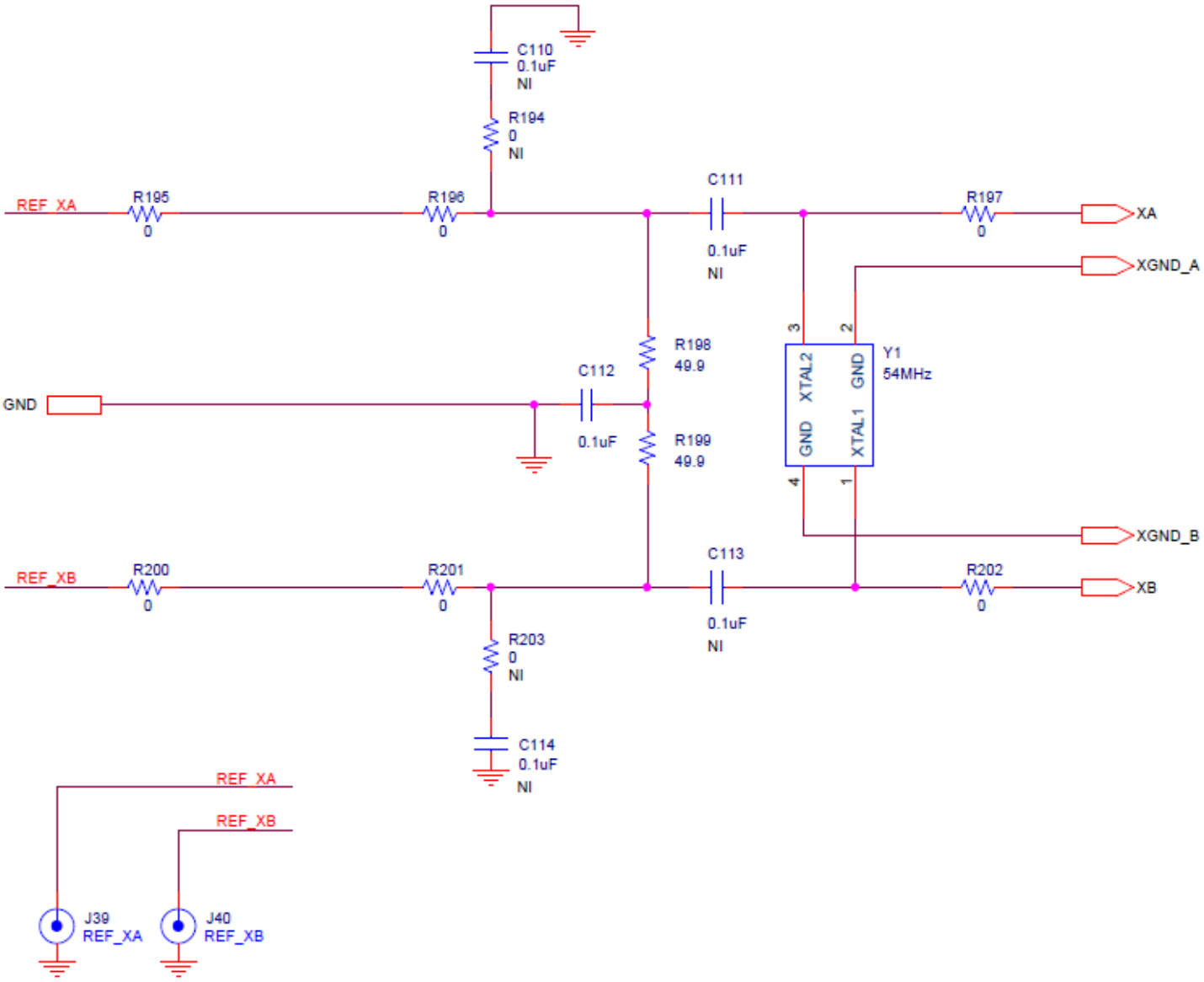


Figure 4.1. External Reference Input Circuit

5. Clock Input and Output Circuits

5.1 Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5380-EVB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB_IN)/IN3B(FB_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5380 data sheet.

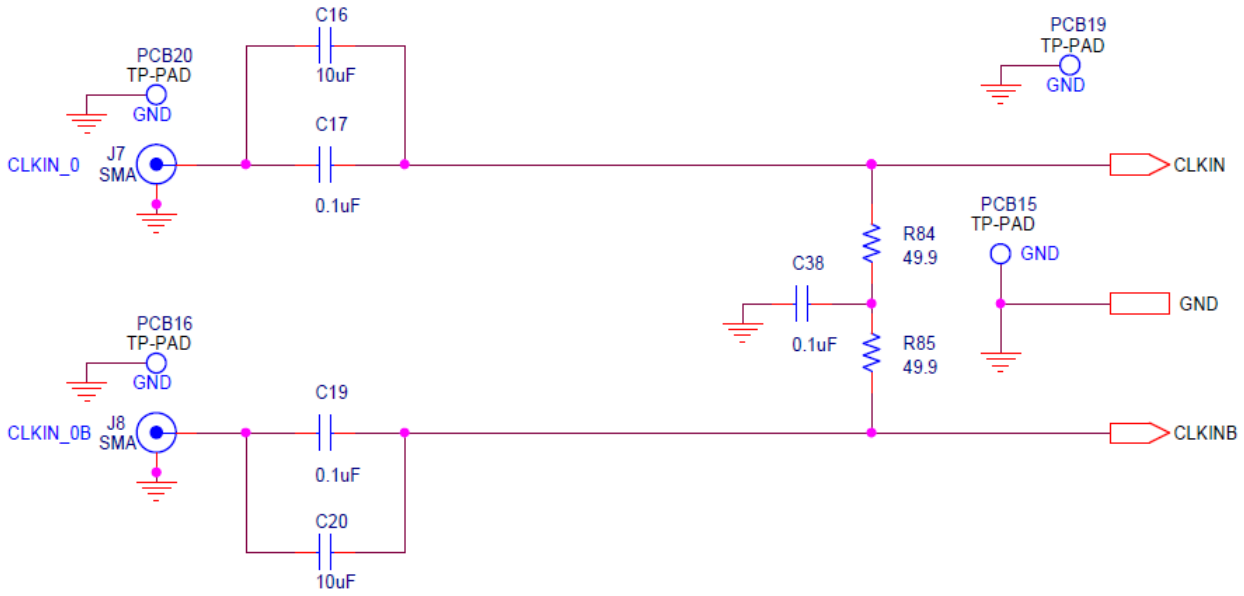


Figure 5.1. Input Clock Termination Circuit

5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5380-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5380-EVB, and provide locations on the PCB for optional dc/ac terminations by the end user.

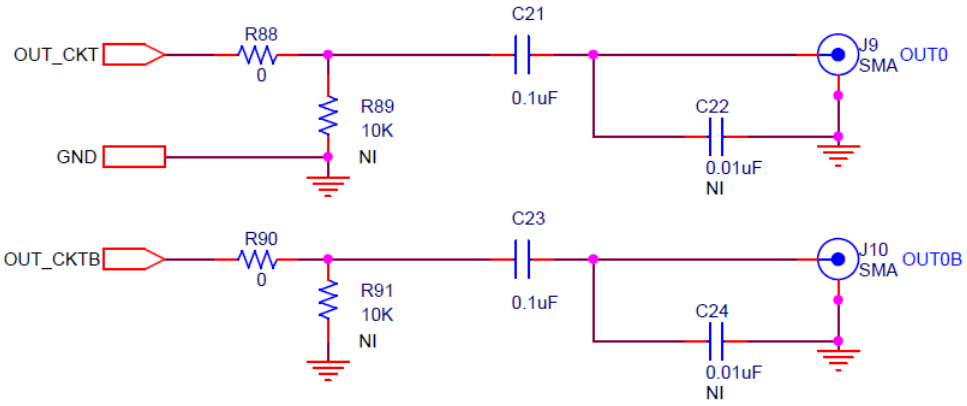


Figure 5.2. Output Clock Termination Circuit

6. Using the Si5380 EVB and Installing ClockBuilderPro (CBPro) Desktop Software

6.1 Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/si538x-4x-evb and download the ClockBuilderPro software.

Installation instructions, release notes, and a user's guide for ClockBuilderPro can be found at the download link shown above. Please follow the instructions as indicated.

6.2 Connecting the EVB to Your Host PC

Once ClockBuilderPro software in installed, connect to the EVB with a USB cable as shown below.

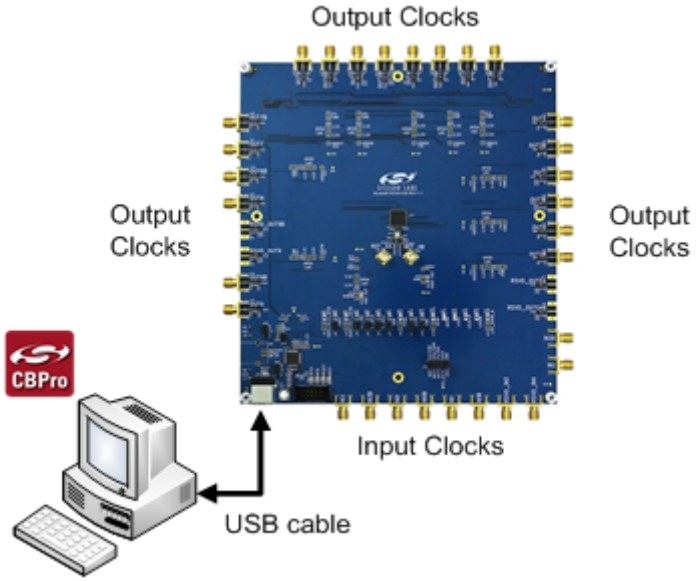


Figure 6.1. EVB Connection Diagram

6.3 Additional Power Supplies

The Si5380-EVB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select “USB”. These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or unexplained increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the “**All Voltages**” tab of the GUI and clicking on the “**Read All**” button produces a display similar to this one:

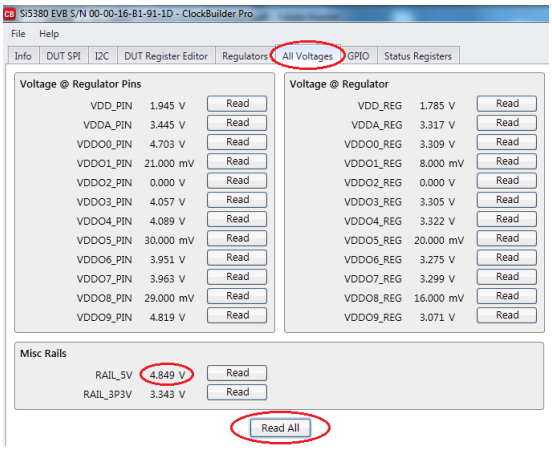


Figure 6.2. EVB GUI - Power Supply Check

Verify that the “**RAIL_5V**” measurement shows the EVB voltage > 4.7 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main SI5380 device supplies. To make this change, move jumper JP15 to connect pins 2-3 “EXT”. Connect J33 to an external 5 V, 0.5A or higher, power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

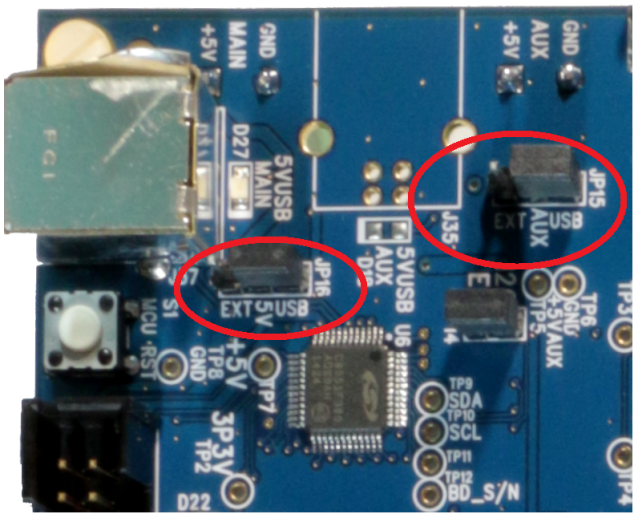


Figure 6.3. JP15-JP16 Standard Jumper Shunt Installation

Errata Note: Some early versions of the 64-pin Si534x-EVBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the *right hand side* as read and viewed in the above figure.

6.4 Overview of ClockBuilderPro Applications

The ClockBuilderPro installer will install two main applications.

Application 1:

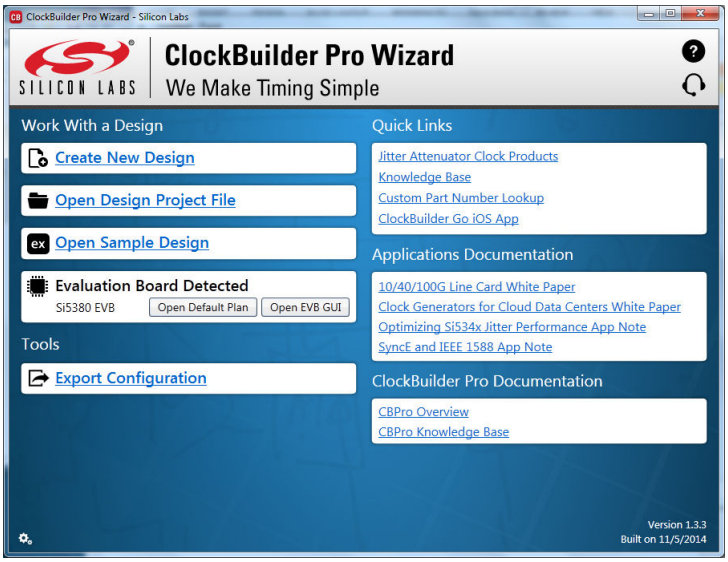


Figure 6.4. ClockBuilderPro Wizard

Use the CBPro Wizard to do the following:

- Create a new design.
- Review or edit an existing design.
- Export: Create in-system programming files.

Application 2:

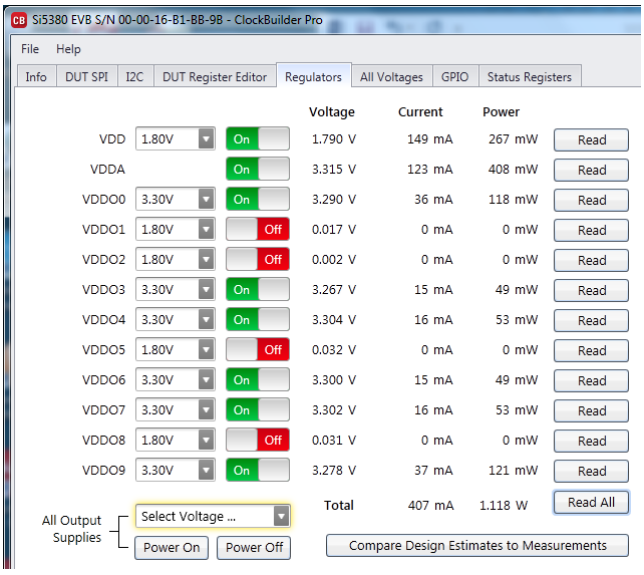


Figure 6.5. EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5380).
- Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

6.5 Common ClockBuilderPro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5380 EVB. These workflow scenarios are:

- **Workflow Scenario #1**: Testing a Silicon Labs-created Default Configuration
- **Workflow Scenario #2**: Modifying the Default Silicon Labs-created Device Configuration
- **Workflow Scenario #3**: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

6.6 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:

Figure 6.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "**Open Default Plan**" button.

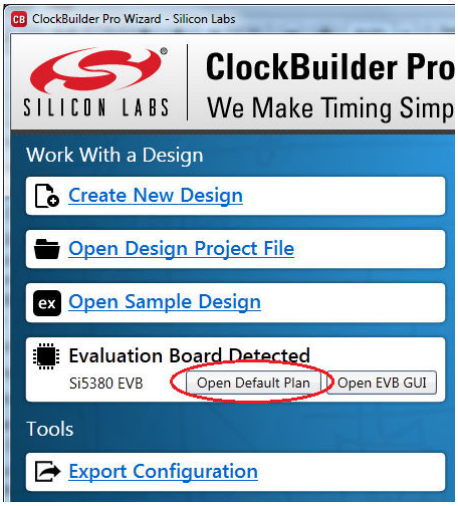


Figure 6.7. CBPro—Open Default Plan Button

Once you open the default plan, a popup will appear.

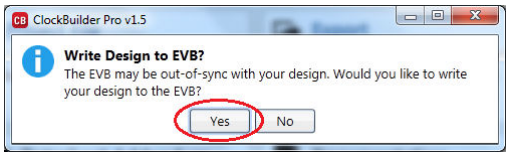


Figure 6.8. CBPro—Write Design Dialog

Select "**Yes**" to write the default plan to the Si5380 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Silicon Labs.

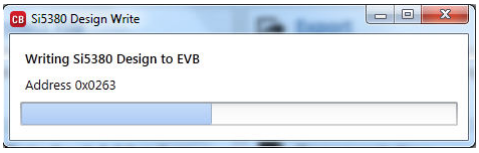


Figure 6.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "**Open EVB GUI**" as shown in the figure below.

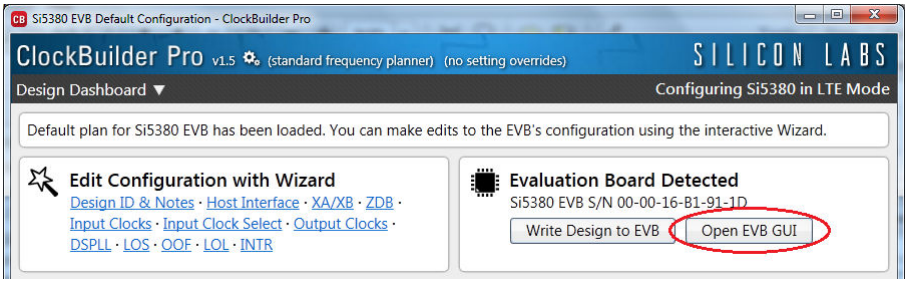


Figure 6.10. CBPro—Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "**Regulators**" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

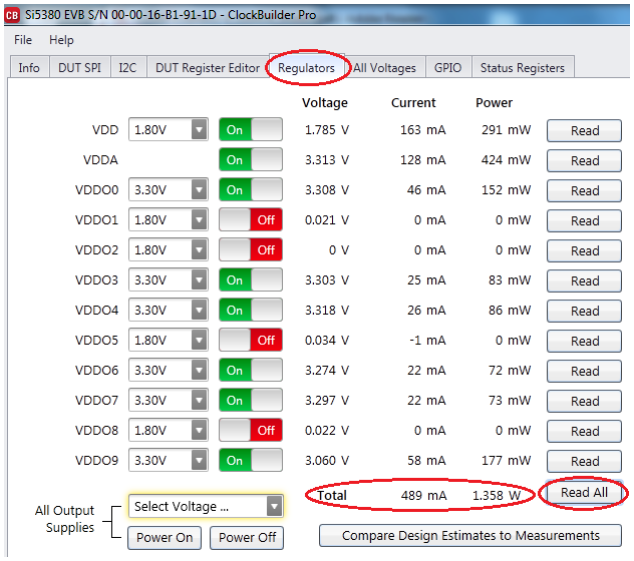


Figure 6.11. EVB GUI—Regulators

6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled “INx/INxB” and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the EVB crystal.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the “**Read All**” button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.
Note: Turning V_{DD} or V_{DDA} “Off” will power-down and reset the DUT. Once both of these supplies are turned “On” again, you must reload the desired frequency plan back into the device memory by selecting the “**Write Design to EVB**” button on the CBPro home screen:

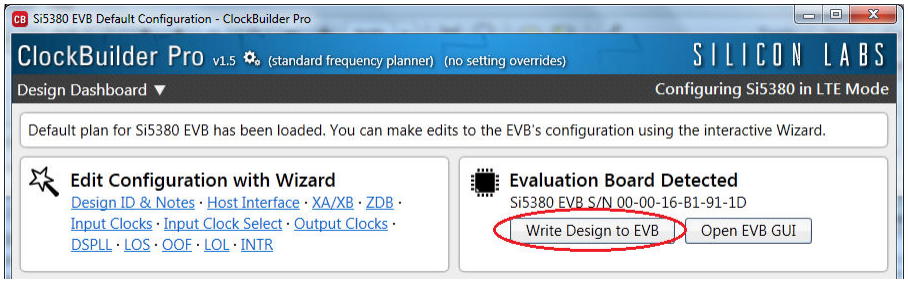


Figure 6.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the crystal, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on “**Frequency Plan Valid**” to see the design report.

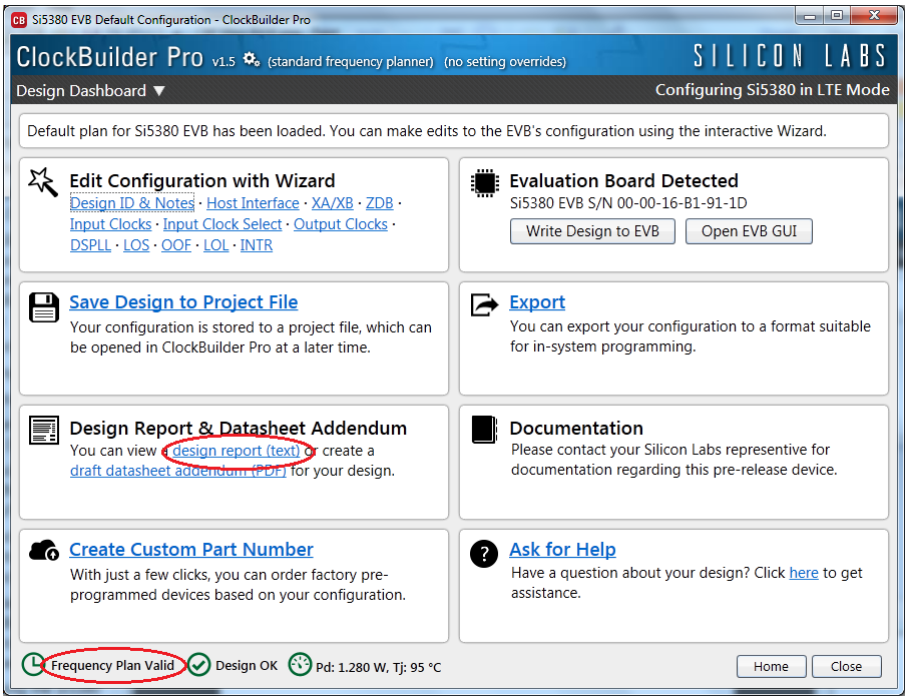


Figure 6.13. CBPro—Design Report Button and Link

Your configuration’s design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project’s Design Report.

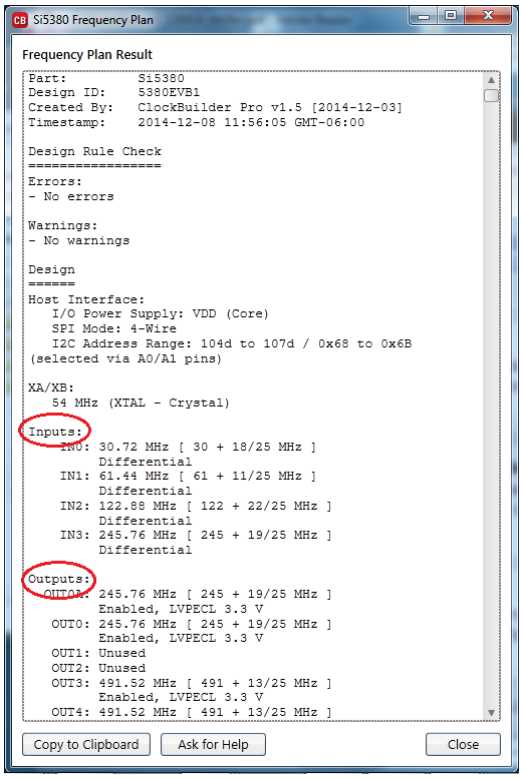


Figure 6.14. CBPro—Design Report

6.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in “locked” mode.

6.7 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a drop-down list by clicking on the "**Design Dashboard**" button above this section.

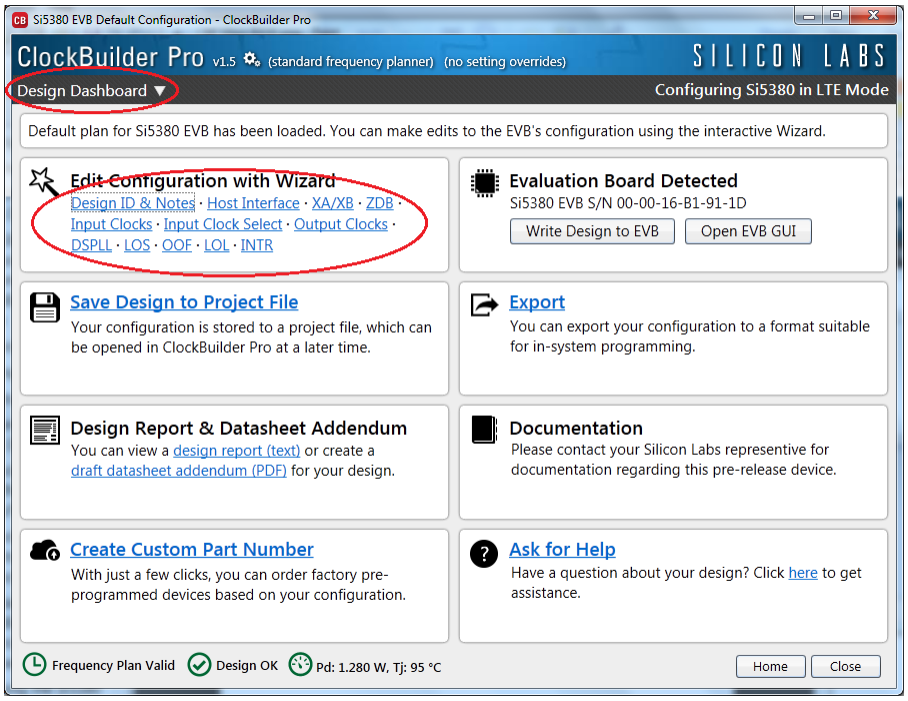


Figure 6.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

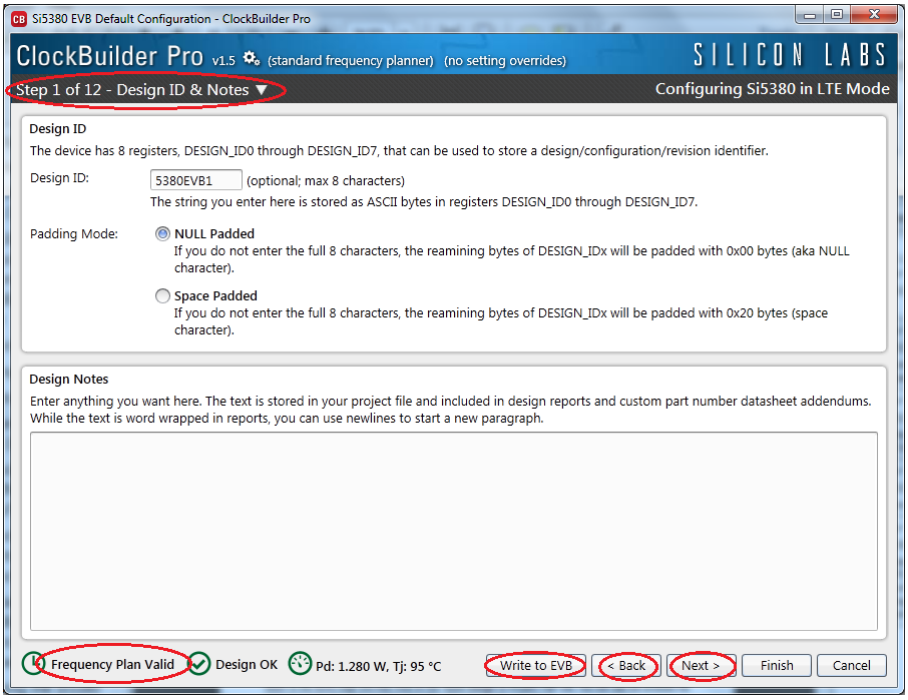


Figure 6.16. CBPro—Design ID and Notes Edit Page

As you edit the settings, you may notice the "**Frequency Plan Valid**" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "**> Next**" or "**< Back**" buttons to move from page to page. When you are done making all your desired changes, you can click on "**Write to EVB**" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.

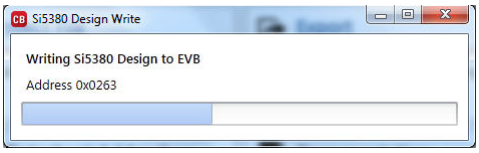


Figure 6.17. CBPro—Design Write Progress Window

When you have verified your design settings, you may save the design project. Click on the "**Finish**" button to return to the home page and then click on the "**Save Design to Project File**" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

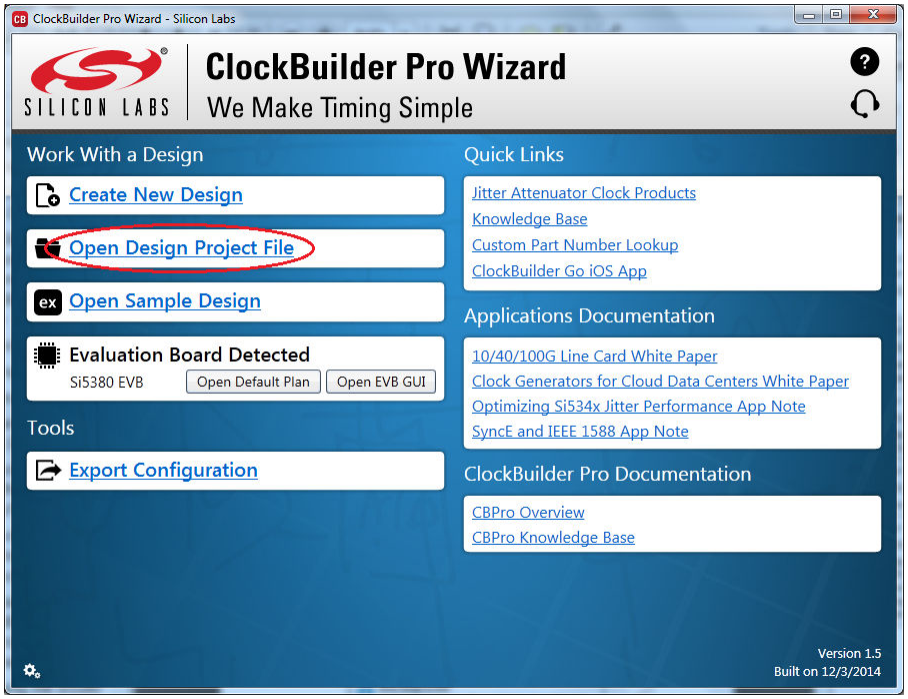


Figure 6.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (*.slabtimeproj or *.sitproj file).

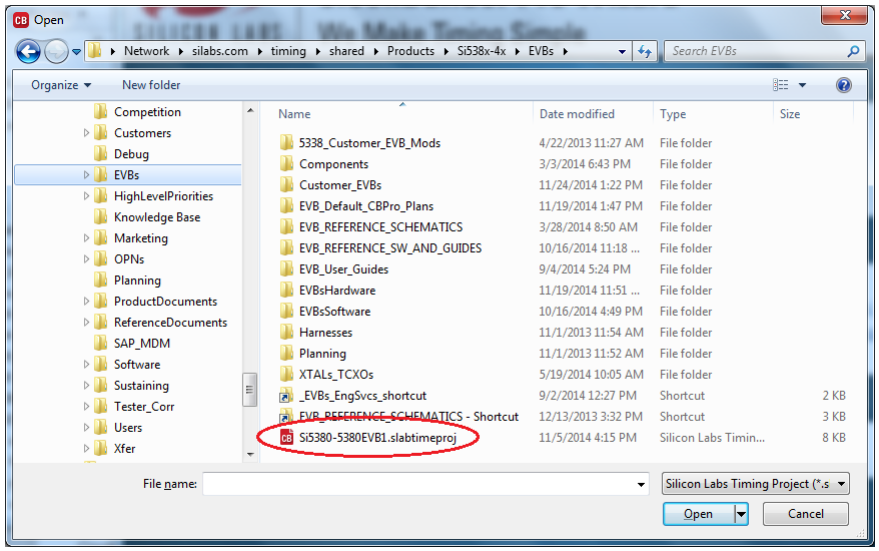


Figure 6.19. CBPro—Windows File Browser

Select "**Yes**" when the WRITE DESIGN to EVB popup appears:

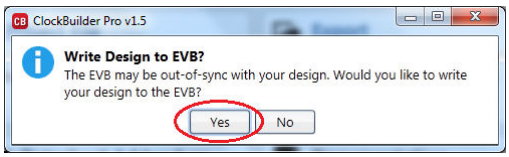


Figure 6.20. CBPro—Write Design Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "**Export**" as shown below:

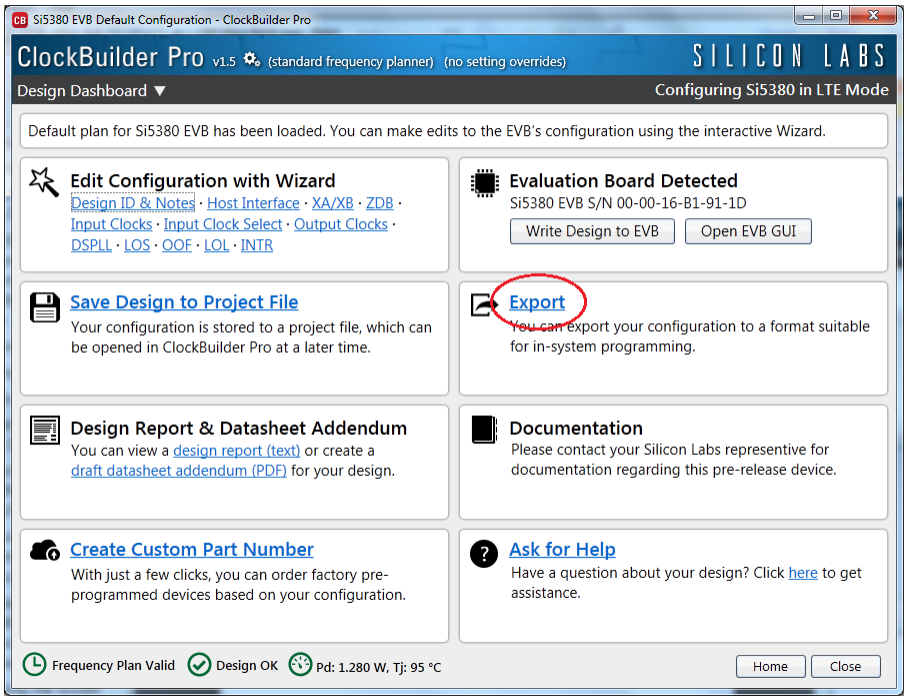


Figure 6.21. CBPro—Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

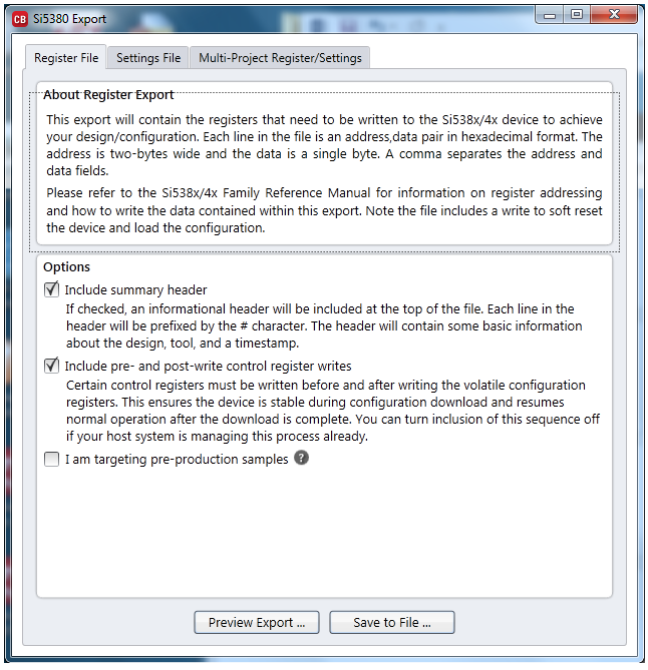


Figure 6.22. CBPro—Export Configuration Window

7. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5380 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.
Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5380 using ClockBuilder-Pro on the Si5380 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5380 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si5380 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

8. Serial Device Communications (Si5380 <-> MCU)

8.1 On-Board SPI Support

The MCU on-board the Si5380-EVB communicates with the Si5380 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5380 device is the SPI slave. The Si5380 device can also support a 2-wire I^2C serial interface, although the Si5380-EVB does NOT support the I^2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I^2C.

8.2 External I^2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5380 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5380 device. The shunt at J4 (I2C_SEL) must also be removed to select I^2C as Si5380 interface type. An external I^2C controller connected to the Si5380 side of J36 can then communicate to the Si5380 device. *(For more information on I^2C signal protocol, please refer to the Si5380 data sheet.)*

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5380 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I^2C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I^2C SDA and J36 pin 8 (DUT_SCLK) as the I^2C SCLK. Please note the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

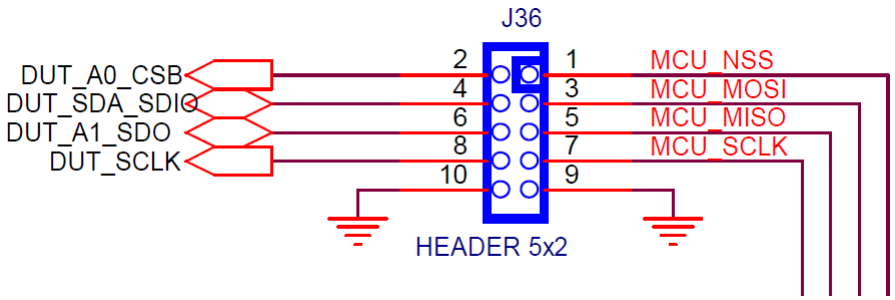


Figure 8.1. Serial Communications Header J36

9. Si5380-EVB Schematic and Bill of Materials (BOM)

The Si5380 EVB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/si538x-4x-evb
Note: Please be aware the Si5380 EVB schematic is in **OrCad Capture** *hierarchical format* and not in a typical “flat” schematic format.

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Silicon Laboratories Inc.
400 West Cesar Chavez
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