Integrated Circuit Systems, Inc.

ICS1524A

Dual Output Phase Controlled SSTL_3/PECL Clock Generator

General Description

The **ICS1524A** is a low-cost, very high-performance frequency generator and phase controlled clock synthesizer. It is perfectly suited to phase controlled clock synthesis and distribution as well as line-locked and genlocked applications.

The **ICS1524A** offers two channels of clock phase controlled outputs; CLK and DPACLK. These two output channels have both 250 MHz PECL differential and 150 MHz SSTL_3 single-ended output pins. The CLK output channel has a fixed phase relationship to the PLL's input and the DPACLK uses the Dynamic Phase Adjust circuitry to allow control of the clock phase relative to input signal.

Optionally, the CLK outputs can operate at half the clock rate and phase aligned with the DPACLK channel, enabling deMUXing of multiplexed analog-to-digital converters. The FUNC pin provides either the regenerated input from the phase-locked loop (PLL) divider chain output or a re-synchronized and sharpened input HSYNC.

The advanced PLL uses either its internal programmable feedback divider or an external divider and is programmed by a standard I²C-bus™ serial interface.

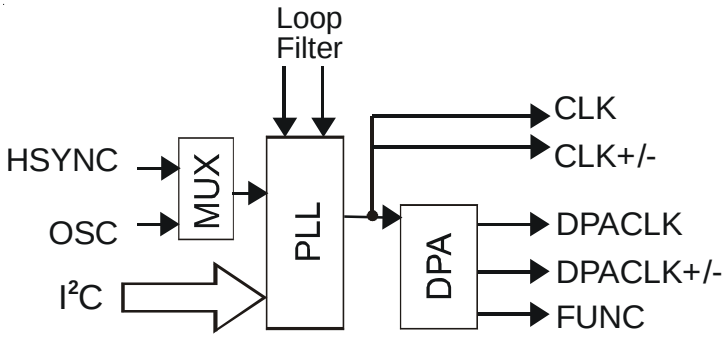
Features

- Wide input frequency range
  - 8 kHz to 100 MHz
- 250 MHz balanced PECL differential outputs
- 150 MHz single-ended SSTL_3 clock outputs
- Dynamic Phase Adjust (DPA) for DPACLK outputs
  - Software controlled phase adjustment
  - 360° Adjustment down to 1/64 clock increments
- External or internal loop filter selection
- Uses 3.3 VDC Inputs are 5 volt tolerant.
- I²C-bus serial interface runs at either low speed (100 kHz) or high speed (400 kHz).
- Hardware and Software PLL Lock detection

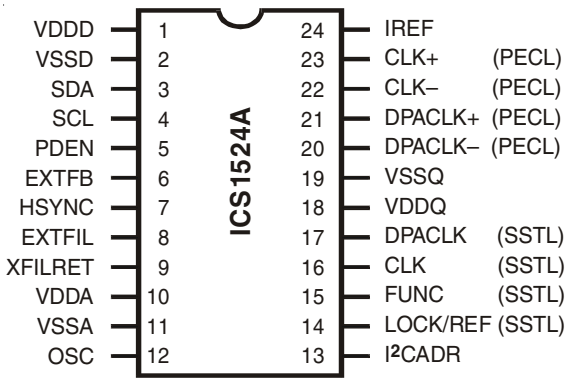
Applications

- Generic Frequency Synthesis
- LCD Monitors and Projectors
- Genlocking Multiple Video Systems

Block Diagram



Pin Configuration



24 Pin 300-mil SOIC

I²C-bus is a trademark of Philips Corporation.

Document Revision History

Rev A

ICS1523 Rev T Datasheet used as a starting template
New Block Diagram substituted for old 1523 one
- Removed reference to CLK / 2 Functionality
- Created a set of clock outputs that bypass the DPA
- External PDEN is now the IN-SEL MUX control bit

Text descriptions changed to support new 1524 block diagram

Rev B

Replaced page 15 “Layout Guidelines”
Replaced SIOC Package diagram on page 22
“Advanced Status” removed
Redrew front page graphics for clairity

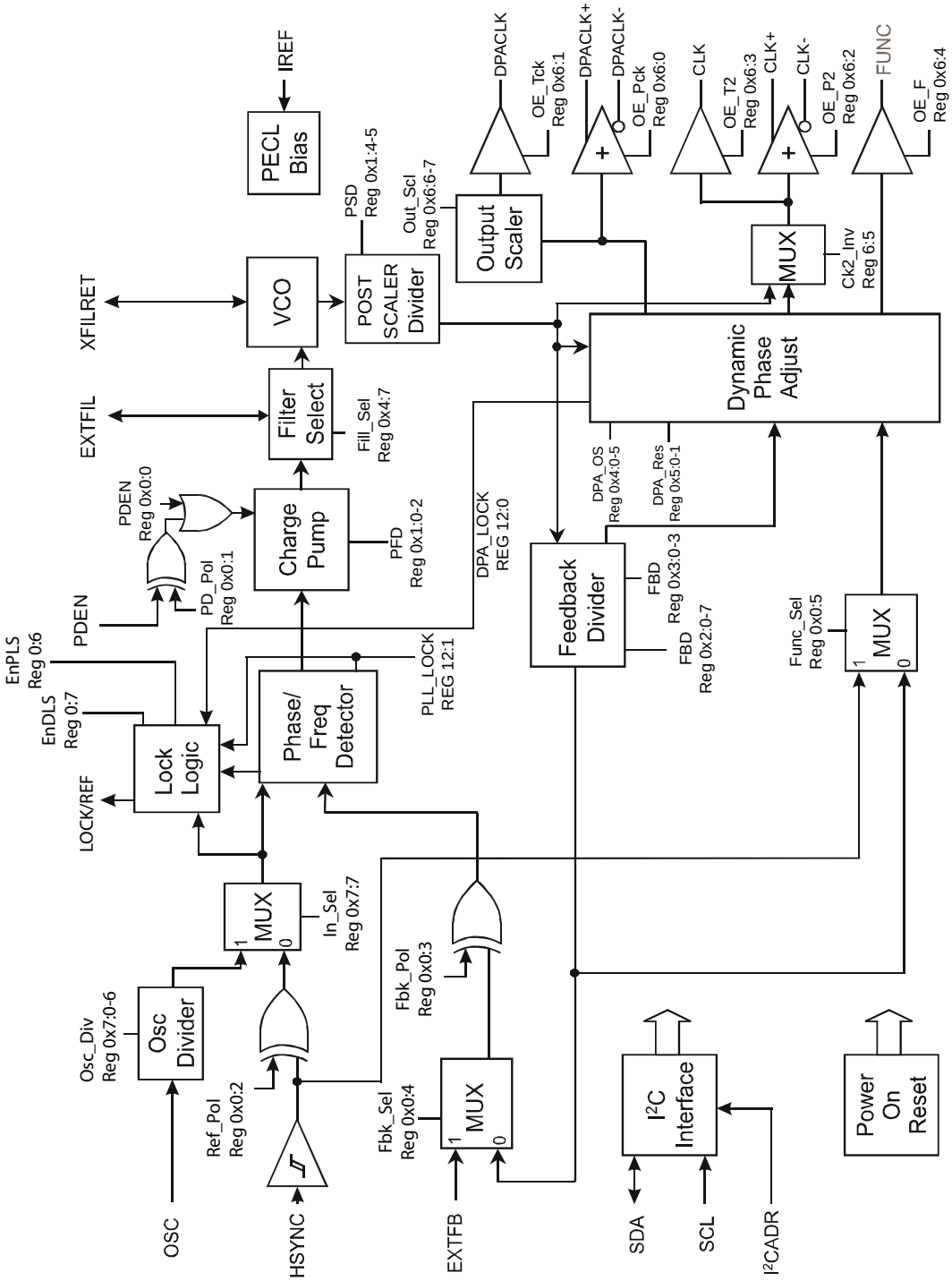
Rev C

Corrected Chip Revision and Chip Version values on page 5
Changed Title on Page 1
Minor format changes to pages 8 and 21
Corrected pin names on page 10

Rev D

Miscellaneous updates to Block Diagram on page 3
Changed reference from “Phase Detector” to “Charge Pump”. Pages 4-7, 10

Block Diagram



Pin Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION	COMMENTS
1	VDDD	PWR	Digital supply	3.3V to digital sections
2	VSSD	PWR	Digital ground	Ground for digital sections
3	SDA	IN/OUT	Serial data	I²C-bus[1]
4	SCL	IN	Serial clock	I²C-bus[1]
5	PDEN	IN	Charge Pump	Suspends charge pump[1]
6	EXTFB	IN	External feedback	External divider input to PFD[1]
7	HSYNC	IN	Horizontal sync	Clock input to PLL[1]
8	EXTFIL	IN	External filter	External PLL loop filter
9	XFILRET	IN	External filter return	External PLL loop filter return
10	VDDA	PWR	Analog supply	3.3V for analog circuitry
11	VSSA	PWR	Analog ground	Ground for analog circuitry
12	OSC	IN	Oscillator	Input from crystal oscillator package[1, 2]
13	I²CADR	IN	I²C address	Chip I²C address select Low = 4Dh read, 4Ch write High = 4Fh read, 4Eh write
14	LOCK/REF	SSTL	Lock indicator/reference	Displays PLL or DPA lock or REF input
15	FUNC	SSTL	Function output	SSTL_3 selectable HSYNC output
16	CLK	SSTL	Pixel clockt	Non-Delayed SSTL_3 Clock
17	DPACLK	SSTL	DPA Delayed Clock	DPA Delayed SSTL_3 Clock
18	VDDQ	PWR	Output driver supply	3.3V VDD for output drivers
19	VSSQ	PWR	Output driver ground	Ground for output drivers
20	DPACLK–	PECL	DPA Delayed PECL clock -	DPA Delayed Inverted PECL Clock Open drain.
21	DPACLK+	PECL	DPA Delayed PECL clock +	DPA Delayed PECL Clock Open drain.
22	CLK–	PECL	PECL clock -	Non-Delayed Inverted PECL Clock Open drain.
23	CLK+	PECL	PECL clock +	Non-Delayed PECL Clock Open drain.
24	IREF	IN	Reference current	Reference current for PECL outputs

Notes:

1. These LVTTL inputs are 5V-tolerant.
2. Connect to ground if unused.

I²C Register Map Summary

Register Index	Name	Access	Bit Name	Bit #	Reset Value	Description
0h	Input Control	R / W	PDen	0	1	Charge Pump Enable (0=Disable 1=Enable)
			PD_Pol	1	0	Charge Pump Enable Polarity
			Ref_Pol	2	0	External Reference Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Pol	3	0	External Feedback Polarity (0=Positive Edge, 1=Negative Edge)
			Fbk_Sel	4	0	External Feedback Select (0=Internal Feedback, 1=External)
			Func_Sel	5	0	Function Out Select (0=Recovered HSYNC, 1=Input HSYNC)
			EnPLS	6	1	Enable PLL Lock/Ref Status Output (0=Disable 1=Enable)
			EnDLS	7	0	Enable DPA Lock/Ref Status Output (0=Disable 1=Enable)
1h	Loop Control	R / W *	PFD0-2	0-2	0	Charge Pump Gain
			Reserved	3	0	Reserved
			PSD0-1	4-5	0	Post-Scaler Divider (0 = /2, 1 = /4, 2 = /8, 3 = /16)
			Reserved	6-7	0	Reserved
2h	FdBk Div 0	R / W *	FBD0-7	0-7	FF	PLL FeedBack Divider LSBs (bits 0-7) *
3h	FdBk Div 1	R / W *	FBD8-11	0-3	F	PLL Feedback Divider MSBs (bits 8-11) *
			Reserved	4-7	0	Reserved
4h	DPA Offset	R / W	DPA_OS0-5	0-5	0	Dynamic Phase Aligner Offset
			Reserved	6	0	Reserved
			Fil_Sel	7	1	Loop Filter Select (0=External, 1=Internal)
5h	DPA Control	R / W **	DPA_Res0-1	0-1	3	DPA Resolution (0=16 delay elements, 1=32, 2=Reserved, 3=64)
			Metal_Rev	2-7	0	Metal Mask Revision Number
6h	Output Enables	R / W	OE_Pck	0	1	Output Enable for PECL DPACLK (0=High Z, 1=Enabled)
			OE_Tck	1	1	Output Enable for STTL_3 DPACLK (0=High Z, 1=Enabled)
			OE_P2	2	1	Output Enable for PECL CLK (0=High Z, 1=Enabled)
			OE_T2	3	1	Output Enable for STTL_3 CLK (0=High Z, 1=Enabled)
			OE_F	4	1	Output Enable for STTL_3 FUNC (0=High Z, 1=Enabled)
			Ck2_Inv	5	0	Select non-delayed CLK (1) or DPA delayed CLK/2 (0) on CLKx pins
			Out_Scl	6-7	0	SSTL DPACLK (Pin 17) Scaler (0 = ÷1, 1 = ÷2, 2 = ÷4, 3 = ÷8)
7h	Osc_Div	R / W	Osc_Div 0-6	0-6	0	Osc Divider modulus
			In-Sel	7	1	RESERVED
8h	Reset	Write	DPA	0-3	x	Writing xA hex resets DPA and loads working register 5
			PLL	4-7	x	Writing 5x hex resets PLL and loads working registers 1-3
10h	Chip Ver	Read	Chip Ver	0-7	18	Chip Version 17 hex
11h	Chip Rev	Read	Chip Rev	0-7	01	Chip Revision C2 hex
12h	Rd_Reg	Read	DPA_Lock	0	N/A	DPA Lock Status (0=Unlocked, 1=Locked)
			PLL_Lock	1	N/A	PLL Lock Status (0=Unlocked, 1=Locked)
			Reserved	2-7	0	Reserved

* Identifies double-buffered registers. Working registers are loaded during software PLL reset.

** Identifies double-buffered register. Working registers are loaded during software DPA reset.

Detailed Register Description

Name: Input Control
Register: 0h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
PDen	0	1	Charge Pump Enable
PD_Pol	1	0	Charge Pump Enable Polarity
Ref_Pol	2	0	External Reference Polarity
Fbk_Pol	3	0	External Reference Feedback Polarity
Fbk_Sel	4	0	External Feedback Select
Func_Sel	5	0	Function Output Select
EnPLS	6	1	Enable PLL Lock Status Output on LOCK/REF pin
EnDLS	7	0	Enable DPA Lock Status Output on LOCK/REF pin

Bit **Name** **Description**

0 PDen

Charge Pump Enable
0 = External Enable via PDEN pin
1 = Always Enable

1 PD_Pol

Charge Pump Enable Polarity
0 = Active High
1 = Active Low

2 Ref_Pol

External Reference Polarity —
Edge of input signal on which Phase/Frequency Detector triggers.
0 = Rising Edge (default)
1 = Falling Edge

3 Fbk_Pol

External Reference Feedback Polarity — Edge of EXTFB (pin 6) signal on which Phase/Frequency Detector triggers when external feedback is used (Reg0 [4]=1).
0 = Positive Edge (default)
1 = Negative Edge

4 Fbk_Sel

External Feedback Select
0 = Internal Feedback (default)
1 = External Feedback

5 Func_Sel

Function Output Select — Selects re-clocked output to FUNC (pin 15).
0 = Recovered HSYNC (default). Regenerated HSYNC output.
1 = External HSYNC. Schmitt-trigger conditioned input from HSYNC (pin 7).

6 EnPLS

7 EnDLS

Enable LOCK/REF (pin14) Output

EnPLS	EnDLS	IN_SEL	LOCK/REF(14)
0	0	N/A	0
0	1	N/A	1 if DPA locked, 0 otherwise
1	0	N/A	1 if PLL locked, 0 otherwise
1	1	0	Post Schmitt trigger HSYNC(7) XOR Ref_Pol
1	1	1	F_{osc} ÷ Osc_Div

Name: Loop Control Register
Register: 1h
Index: Read/Write*

Bit Name	Bit #	Reset Value	Description
PFD0-2	0-2	0	Charge Pump Gain
Reserved	3	0	Reserved
PSD0-1	4-5	0	Post-Scaler Divider
Reserved	6-7	0	Reserved

Bit Name Description

0-2 PFD0-2 Charge Pump Gain

Bit 2	Bit 1	Bit 0	CP Gain (µA/2π rad)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

3 Reserved

4-5 PSD0-1 Post-Scaler Divider — Divides the output of the VCO to the DPA and Feedback Divider.

Bit 5	Bit 4	PSD Divider
0	0	2 (default)
0	1	4
1	0	8
1	1	16

6-7 Reserved

*Double-buffered register. Actual working registers are loaded during software PLL reset. See register 8h for details.

Name: Feedback Divider 0 Register / Feedback Divider 1 Register
Register: 2h, 3h
Index: Read/Write*

Bit Name	Index	Bit #	Reset Value	Description
FBD 0-7	2	0-7	FF	PLL Feedback Divider LSBs (0-7).* When Bit 0 = 0, then the total number of clocks per line is even. When Bit 0 = 1, then the total number of clocks is odd.
FBD 8-11	3	0-3	F	PLL Feedback Divider MSBs (8-11)*
Reserved	3	4-7		Reserved

The value that is programmed into these two registers, plus a value of 8, defines the total number of clock periods that the ICS 1524 generates between HSYNCs. Program these registers with the total number of horizontal clocks per line minus 8.

Feedback Divider Modulus =

Reg 3				Reg 2							
3	2	1	0	7	6	5	4	3	2	1	0

+8

$12 \leq$ Feedback Divider Modulus ≤ 4103

*Double-buffered registers. Actual working registers are loaded during software PLL reset. See Register 8h for details.

Name: DPA Offset Register
Register: 4h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
DPA_OS0-5	0-5	0	Dynamic Phase Adjust Offset
Reserved	6	0	Reserved
Fil_Sel	7	0	Loop Filter Select

Bit	Name	Description
0-5	DPA_OS0-5	Dynamic Phase Adjust Offset. Selects clock edge offset in discrete steps from zero to one clock period minus one step. Resolution (number of delay elements per clock cycle) is selected by DPA_Res0-1 (Reg 5:0-1). Note: Offsets equal to or greater than one clock period are neither recommended nor supported. Example: For DPA_Res0-1=01H, the clock can be delayed from 0 to 31 steps.
7	Fil_Sel	Selects external loop filter (0) or internal loop filter (1). The use of an external loop filter is strongly recommended for all designs. Typical loop filter values are 6.8K Ohms for the series resistor, 3300 pF RF-type capacitor for the series capacitor, and 33 pF for the shunt capacitor.

Name: DPA Control Register
Register: 5h
Index: Read/Write*

Bit Name	Bit #	Reset Value	Description
DPA_Res0-1	0-1	3	Dynamic Phase Adjust Resolution Select.
Metal_Rev	2-7	0	Metal Mask Revision Number.

Bit	Name	Description
0-1	DPA_Res0-1	Dynamic Phase Adjust (DPA) Resolution Select. It is not recommended to use the DPA above 160 MHz.

Bit 1	Bit 0	Delay Elements	CLK Range, MHz
0	0	16	48 – 160
0	1	32	24 – 80
1	0	Reserved	
1	1	64	12 – 40

2-7	Metal_Rev	Metal Mask Revision Number. After power-up, register bits 7:2 must be written with 111111. After this write, a read indicates the metal mask revision, as below.

Revision	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
A	1	1	1	1	1	1
B	0	1	1	1	1	1
C1	1	0	1	1	1	1
C2	0	0	1	1	1	1
D	1	1	0	1	1	1
E	1	1	1	0	1	1
F	1	1	1	1	0	1
G	1	1	1	1	1	0

* Double-buffered register. Actual working registers are loaded during software DPA reset. See register 8h for details.

Name: Output Enable Register
Register: 6h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
OE_Pck	0	0	Output Enable for DPACLK Outputs (PECL, Pins 21, 20)
OE_Tck	1	0	Output Enable for DPACLK Output (SSTL_3 Pin 17)
OE_P2	2	0	Output Enable for CLK Outputs (PECL, Pins 23, 22)
OE_T2	3	0	Output Enable for CLK Output (SSTL_3, Pin 16)
OE_F	4	0	Output Enable for FUNC Output (SSTL_3, Pin 15)
CK2_Inv	5	0	Select CLK Output Source (Pins 23, 22, 16)
Out_Scl	6-7	0	DPACLK Output Scaler (SSTL_3, Pin 17)

Bit	Name	Description
0	OE_Pck	Output Enable for DPACLK Outputs (PECL) 0 = High Z 1 = Enabled
1	OE_Tck	Output Enable for DPACLK Output (SSTL_3) 0 = High Z 1 = Enabled
2	OE_P2	Output Enable for CLK Outputs (PECL) 0 = High Z 1 = Enabled
3	OE_T2	Output Enable for CLK Output (SSTL_3) 0 = High Z 1 = Enabled
4	OE_F	Output Enable for FUNC Output (SSTL_3) 0 = High Z 1 = Enabled
5	Ck2_Inv	Select CLK Output Source (Pins 23, 22, 16) 0 = Half Speed DPA Delayed clock to CLK outputs 1 = Full Speed non-DPA Delayed clock to CLK outputs
6-7	Out_Scl	Clock (DPACLK, pin 17) Scaler

Bit 7	Bit 6	DPACLK Divider
0	0	1
0	1	2
1	0	4
1	1	8

Name: Oscillator Divider Register
Register: 7h
Index: Read/Write

Bit Name	Bit #	Reset Value	Description
Osc_Div 0-6	0-6	0	Osc Divider Modulus
In_Sel	7	1	Input Select

Bit	Name	Description
0-6	Osc_Div 0-6	Oscillator Divider Modulus. Divides the input from OSC (pin 12) by the set modulus. The modulus equals the programmed value, plus 2. Therefore, the modulus range is from 3 to 129.
7	In_Sel	Input Select — Selects the input to the Phase/Frequency Detector 0 = HSYNC 1 = Osc Divider

Name: RESET Register
Register: 8h
Index: Write

Bit Name	Bit #	Reset Value	Description
DPA Reset	0-3	x	Writing xAh to this register resets DPA working register 5
PLL Reset	4-7	x	Writing 5xh to this register resets PLL working registers 1-3

Bit	Name	Description
0-3	DPA	Writing xAh to this register resets DPA working register 5
4-7	PLL	Writing 5xh to this register resets PLL working registers 1-3

Value	Resets
xA	DPA
5x	PLL
5A	DPA and PLL

Name: Chip Version Register
Register: 10h
Index: Read

Bit Name	Bit #	Reset Value	Description
Chip Ver	0-7	17	Chip Version 24 (18h)

Name: Chip Revision Register
Register: 11h
Index: Read

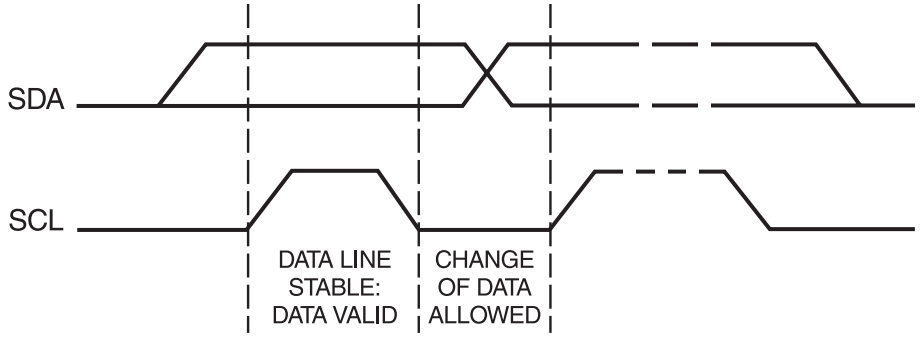
Bit Name	Bit #	Reset Value	Description
Chip Rev	0-7	01+	Initial value 01h. +Value increments with each all-layer change.

Name: Status Register
Register: 12h
Index: Read

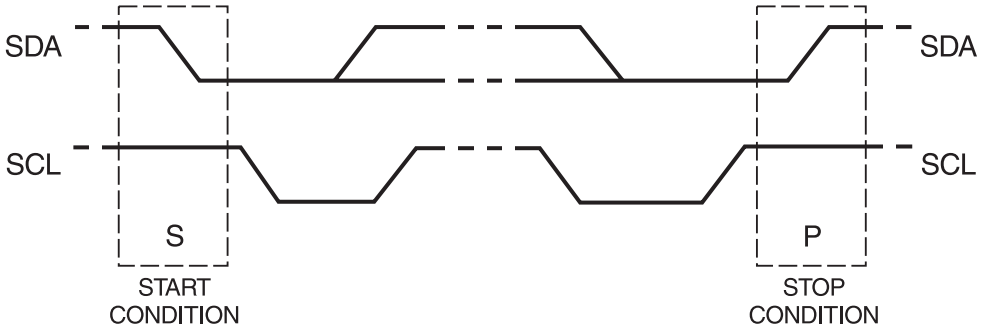
Bit Name	Bit #	Reset Value	Description
DPA_Lock	0	N/A	DPA Lock Status
PLL_Lock	1	N/A	PLL Lock Status
Reserved	2-7	0	Reserved

Bit	Name	Description
0	DPA_Lock	DPA Lock Status. (Refer to Register 0h, bits 6 and 7.) 0 = Unlocked 1 = Locked
1	PLL_Lock	PLL Lock Status. (Refer to Register 0h, bits 6 and 7.) 0 = Unlocked 1 = Locked
2-7	Reserved	

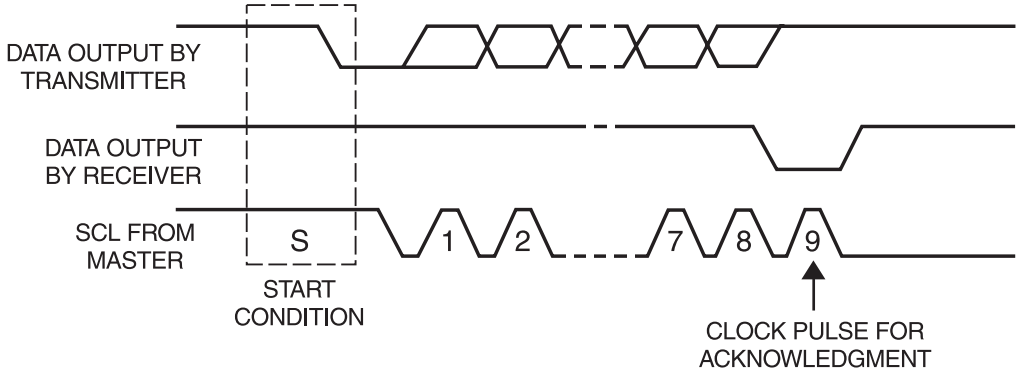
I²C Data Characteristics



Bit transfer on the I²C-bus



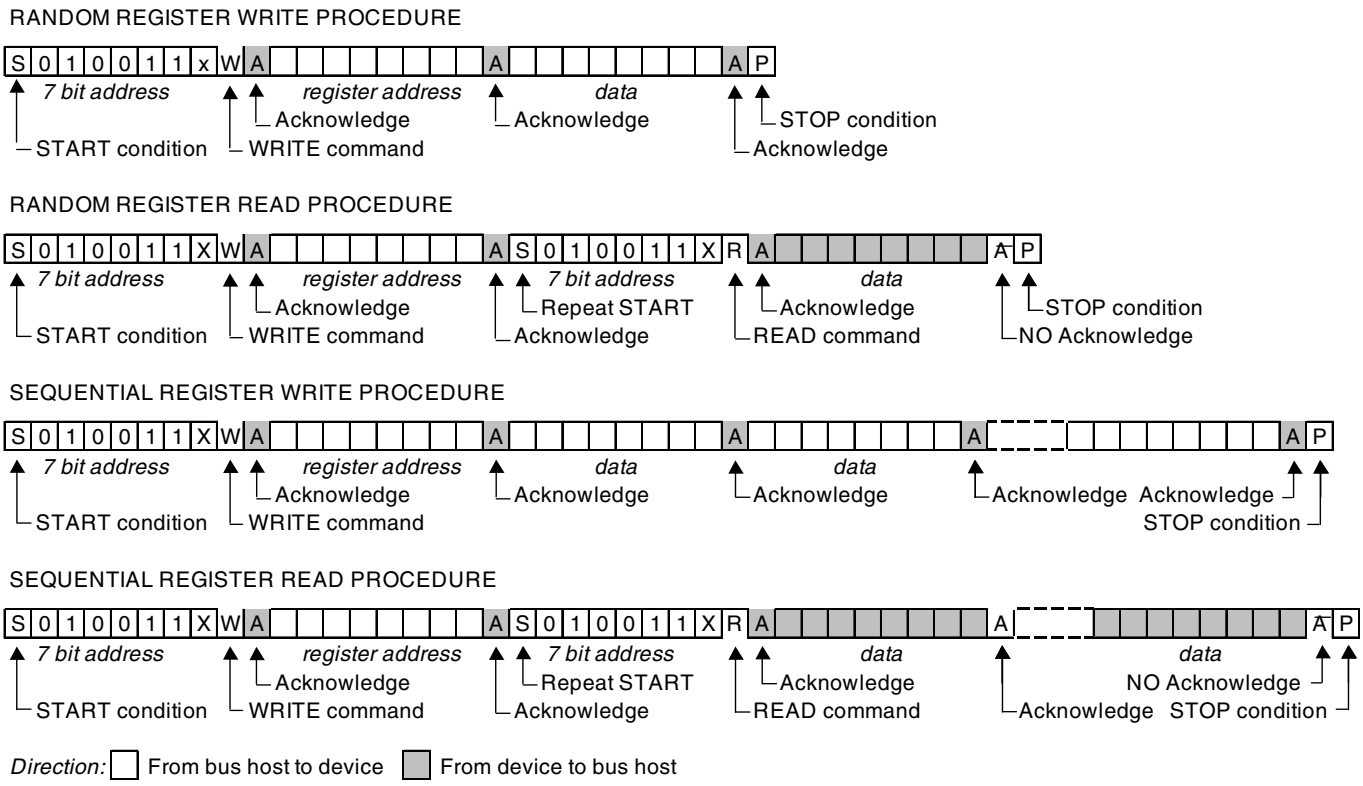
START and STOP conditions



Acknowledge on the I²C-bus

These waveforms are from "The I²C-bus and how to use it," published by Philips Semiconductor.
The document can be obtained from http://www-us2.semiconductors.philips.com/acrobat/various/i2c_bus_specification_1995.pdf

I²C Data Format

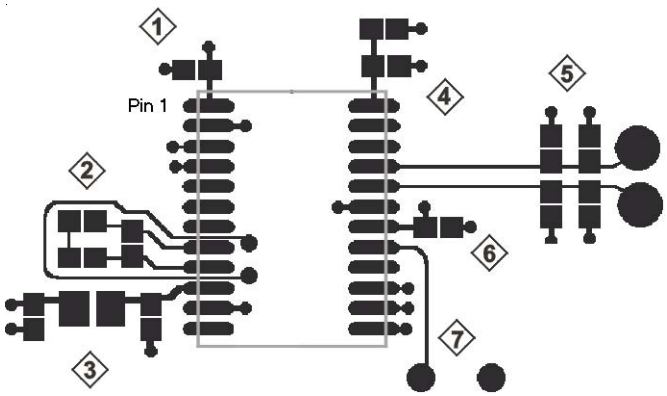


Note:

1. All values are transmitted with the most-significant bit first and the least-significant bit last.
2. The value of the X bit equals the logic state of pin 13 (I^2CADR).
3. R = READ = 1 and W = WRITE = 0

General Layout Guidelines

- Use a PC board with at least four layers: one power, one ground, and two signal.
- Use at least one 4.7 uF Tantalum (or similar) capacitor for global VDD bulk decoupling.
- All supply voltages must be supplied from a common source and must ramp together.
- Any flux or other board surface debris can degrade the performance of the external loop filter.
- Ensure that the 1524A area of the board is free of contaminants.



Specific Layout Guidelines

1. **Digital Supply (VDD) –** Bypass pin 1 (VDD) to pin 2 (VSS) a 0.1-µF capacitor, located as close as possible to the pins. A 0.01-µF capacitor may be added for additional high frequency rejection.

2. **External Loop Filter – Strongly recommended in <u>All Designs</u>.** Locate loop filter components as close to pins 8 and 9 (EXTFIL and EXTFILRET) as possible with minimum length traces. Typical loop filter values are 6.8K Ohms for the series resistor, 3300 pF RF-type capacitor for the series capacitor, and 33 pF for the shunt capacitor. (For details, see the *Frequently Asked Questions* part of the *ICS1523 Applications Guide*, FAQ2 and FAQ3.) A ground isolated, surface trace can be useful to isolate this section from the rest of the board.

3. **Analog PLL Supply (VDDA) –** Decouple main VDD from pin 10 (VDDA) with a series ferrite bead. Bypass the supply end of the bead with 4.7-µF. Bypass pin 10 to pin 11 (VSSA) with a 0.1-µF capacitor. A 0.01-µF capacitor may be added for additional high frequency rejection. Locate these components as close as possible to the pins.

4. **PECL Current Set Resistor –** Locate PECL current-set resistor as close as possible to pin 24 (IREF). Bypass pin 24 to ground with a 0.1-µF capacitor.

5. **PECL Outputs –** Implement these outputs as microstrip transmission lines. The trace widths shown are for 75 Ohm characteristic impedance. Locate any optional series “snubbing” resistors as close as possible to the source pins. If the termination resistors are included on-board, locate them as close as possible to the load and connect directly to the power and ground planes.

   [These termination resistors are omitted if the load device implements them internally. For details, see the ICS application note on microstrip and striplines (1572AN1) and within the *ICS1523 Applications Guide*, the application note on *Designing a Custom Interface for the ICS1523* (1523AN4.)]

6. **Output Driver Supply –** Bypass pin 18 (VDDQ) to pin 19 (VSSQ) with a 0.1-µF capacitor, located as close as possible to the pins. A 0.01-µF capacitor may be added for additional high frequency rejection.

7. **SSTL_3 Outputs –** SSTL_3 outputs can be used like conventional CMOS rail-to-rail logic or as a terminated transmission line system at higher-output frequencies. With terminated outputs, the considerations of item 5, “PECL Outputs” apply. See JEDEC documents JESD8-A and JESD8-8.

PECL Outputs

For information on using the ICS1524A's PECL output pins, please refer to Application Note 4: Designing a Custom PECL Interface for the ICS1523

SSTL_3 Outputs

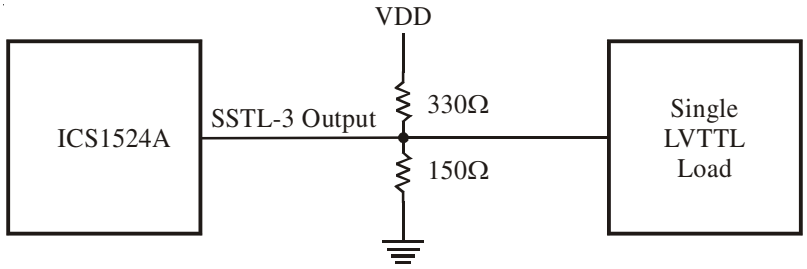
Unterminated Outputs

In the ICS1524A, unterminated SSTL_3 output pins display exponential transitions similar to those of rectangular pulses presented to RC loads. The 10-90% rise time is typically 1.6 ns, and the corresponding fall time is typically 700 ps. In turn, this asymmetry contributes to duty cycle asymmetry at higher output frequencies. In the absence of significant load capacitance (which can further increase rise and fall time), this asymmetry is the dominant factor determining high-frequency performance of these single-ended outputs. Typically, no termination is required either for the LOCK/REF, FUNC, and CLK/2 outputs or for CLK outputs up to approximately 135 MHz.

Terminated Outputs

SSTL_3 outputs are intended to terminate in low impedances to reduce the effect of external circuit capacitance. Use of transmission line techniques enables use of longer traces between source and driver without increasing ringing due to reflections. Where external capacitance is minimal and substantial voltage swing is required to meet LVTTL V_{IH} and V_{OL} requirements, the intrinsic rise and fall times of ICS1524A SSTL outputs are only slightly improved by termination in a low impedance.

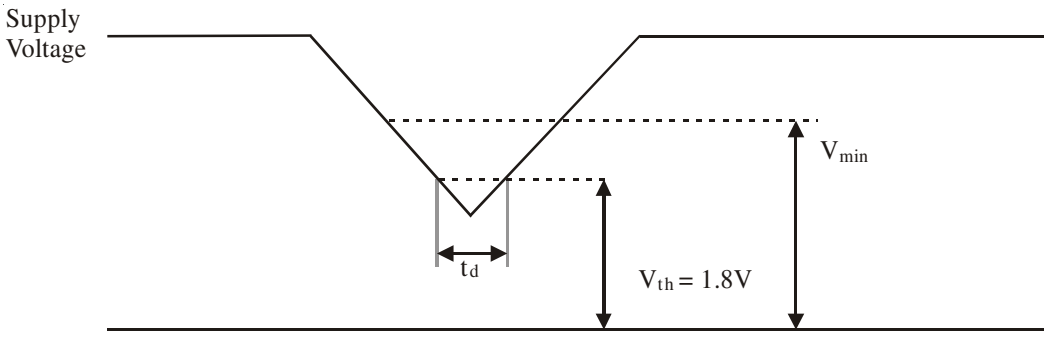
The ICS1524A SSTL output source impedance is typically less than 60 Ohms. Termination impedance of 100 Ohms reduces output swing by less than 30% which is more than enough to drive a single load of LVTTL inputs.



For more information on using the ICS1524A's SSTL output pins, please refer to Application Note 3: Using SSTL_3 Outputs with CMOS or LVTTL Inputs

Power Supply Considerations

The ICS1524A incorporates special internal power-on reset circuitry that requires no external reset signal connection. The supply voltage (VDD) must remain within the recommended operating conditions during normal operation. To reset the ICS1524A, the supply voltage at the part must be reduced below the threshold voltage (V_{th}) of the power-on reset circuit. The supply voltage must remain below that threshold voltage such that board power conditioning capacitors are drained and the proper reset state is latched. The amount of time (t_d) to hold the voltage in a reset state varies with the design. However, a typical value of 10 ms should be sufficient.



Absolute Maximum Ratings

VDD, VDDA, VDDQ (measured to VSS)	4.3V
Digital Inputs	VSS – 0.3V to 5.5V
Analog Outputs	VSSA – 0.3V to VDDA +0.3V
Digital Outputs	VSSQ – 0.3V to VDDQ +0.3V
Storage Temperature	– 65°C to +150°C
Junction Temperature	175°C
Soldering Temperature	260°C
ESD Susceptibility*	> 2 KV

(*Electrostatic-sensitive devices. Do not open or handle except in a static-free workstation.)

Recommended Operating Conditions

VDD, VDDQ, VDDA (measured to VSS) . 3.0 to 3.6 V
Operating Temperature (Ambient) . . . . . 0 to +70°C

DC Supply Current

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Current, Digital	IDDD	VDDD = 3.6V	—	25	mA
Supply Current, Output Drivers	IDDQ	VDDQ = 3.6V, no output drivers enabled.	—	6	mA
Supply Current, Analog	IDDA	VDDA = 3.6V	—	5	mA

Digital Inputs (SDA, SCL, PDEN, EXTFB, HSYNC, OSC, I^2CADR)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	VIH		2	5.5	V
Input Low Voltage	VIL		VSS-0.3	0.8	V
Input Hysteresis			0.2	0.6	V
Input High Current	IIH	V_{IH} = VDD	—	±10	µA
Input Low Current	IIL	V_{IL} = 0	—	±200	µA
Input Capacitance	Cin		—	10	pF

SDA (In Output Mode: SDA is Bidirectional)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Low Voltage	VOL	IOUT = 3 mA. VOH = 6.0V maximum as determined by the external pull-up resistor.		0.4	V

PECL Outputs (DPACLK+, DPACLK–, CLK+, CLK -)

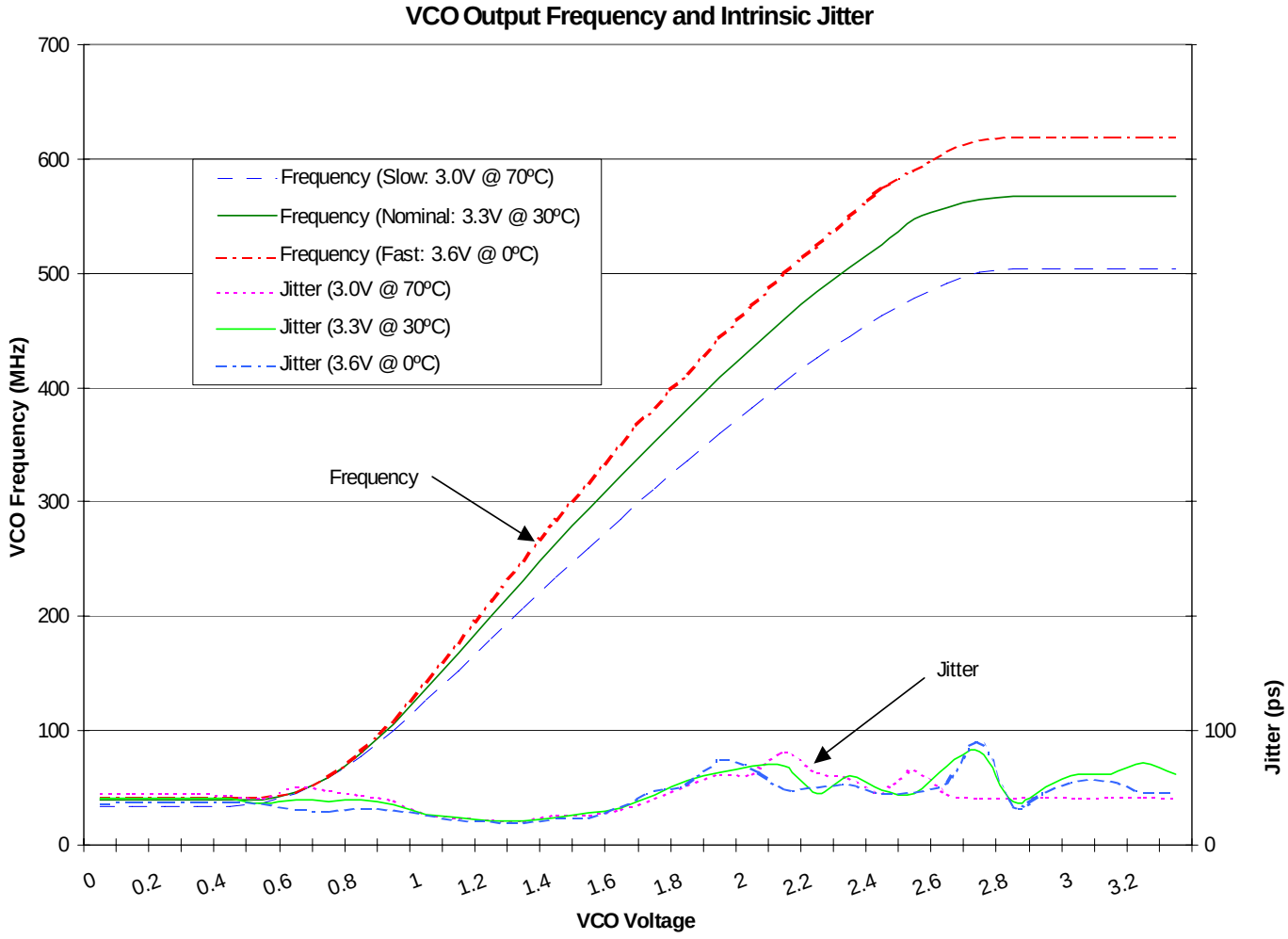
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage	VOH	IOUT = 0	—	VDD	V
Maximum Output Frequency	Fp MAX	VDDD = 3.3V	—	250	MHz
Output Low Voltage (Note: VOL must not fall below the level given so that the correct value for IOUT can be maintained.)	VOL	IOUT = programmed value	1.0	—	V

SSTL-3 Outputs (DPACLK, CLK, FUNC, LOCK/REF)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Resistance	R_O	1 <V_O<2V	—	80	Ω
Maximum Output Frequency	Fs MAX	VDDD = 3.3V	—	150	MHz

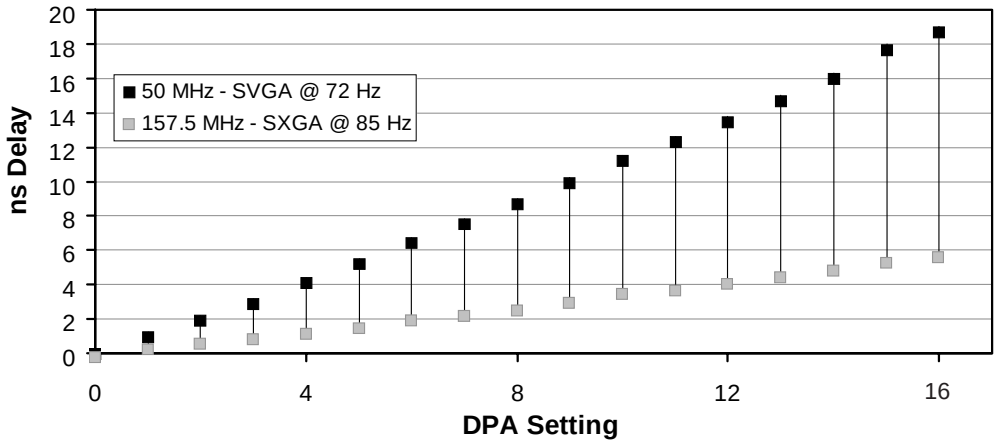
AC Input Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
HSYNC Input Frequency	f_{HSYNC}		.008	10	MHz
OSC Input Frequency	f_{OSC}		.02	100	MHz

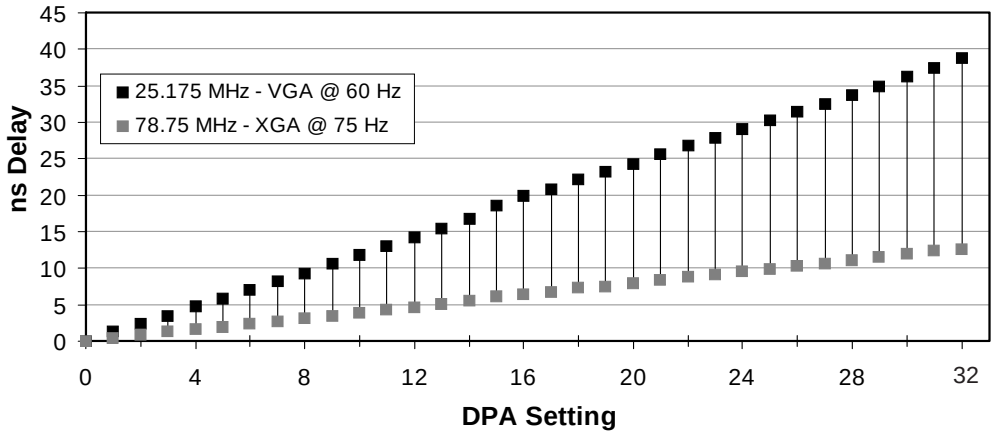


Note: Measured with an Externally Forced Filter Voltage

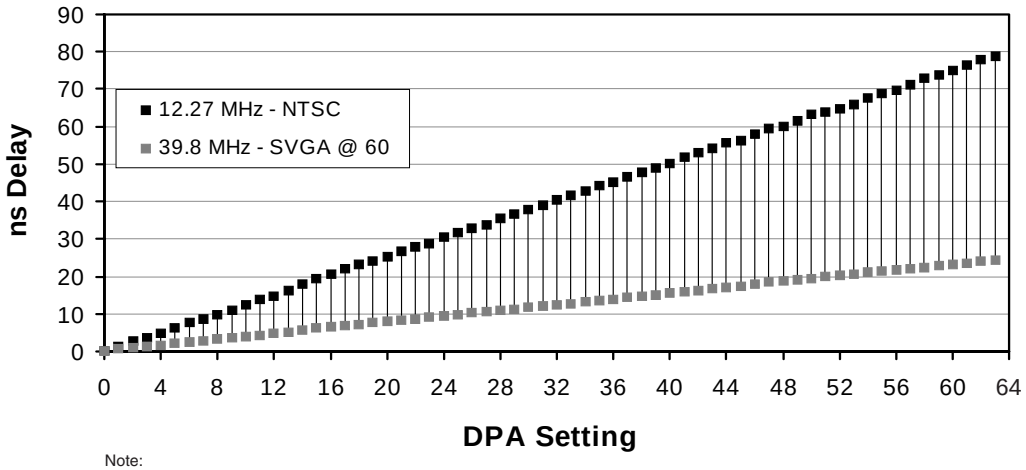
DPA Delay-16 Element Resolution



DPA Delay - 32 Element Resolution

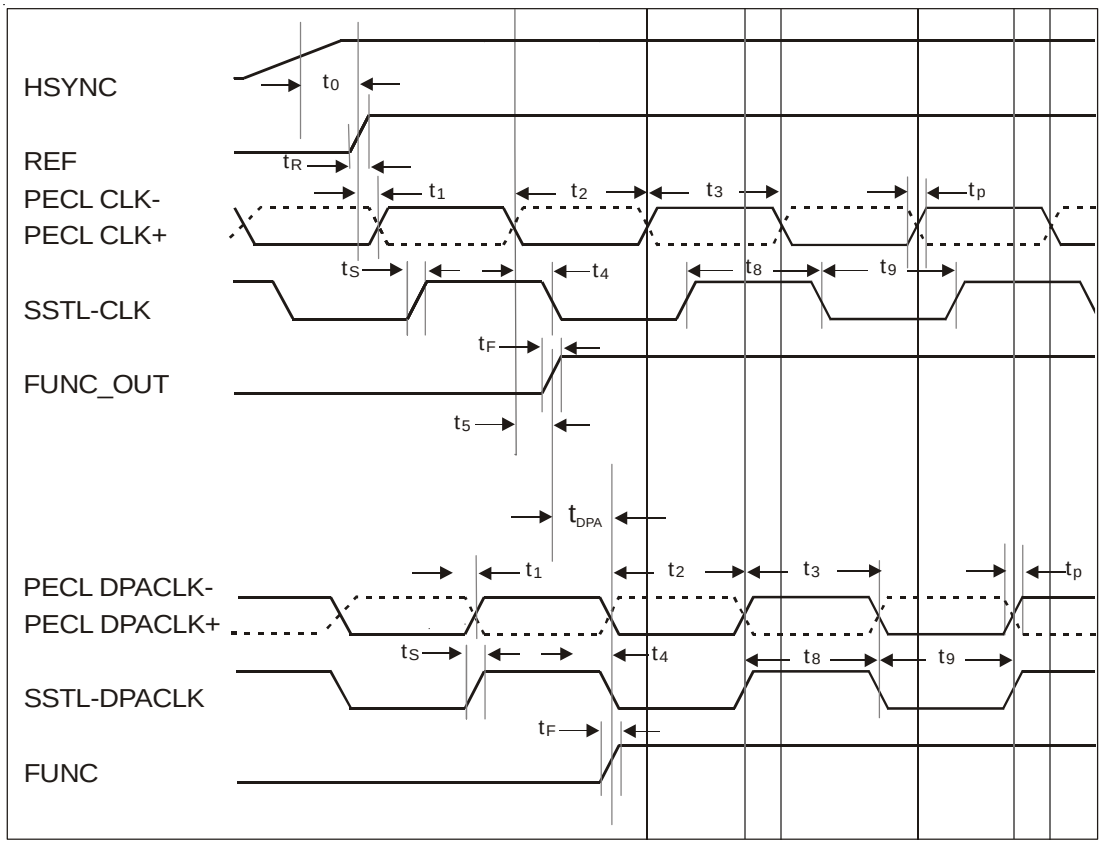


DPA Delay - 64 Element Resolution



Note:
Maximum number of data points used for this graph.

Output Timing Diagram



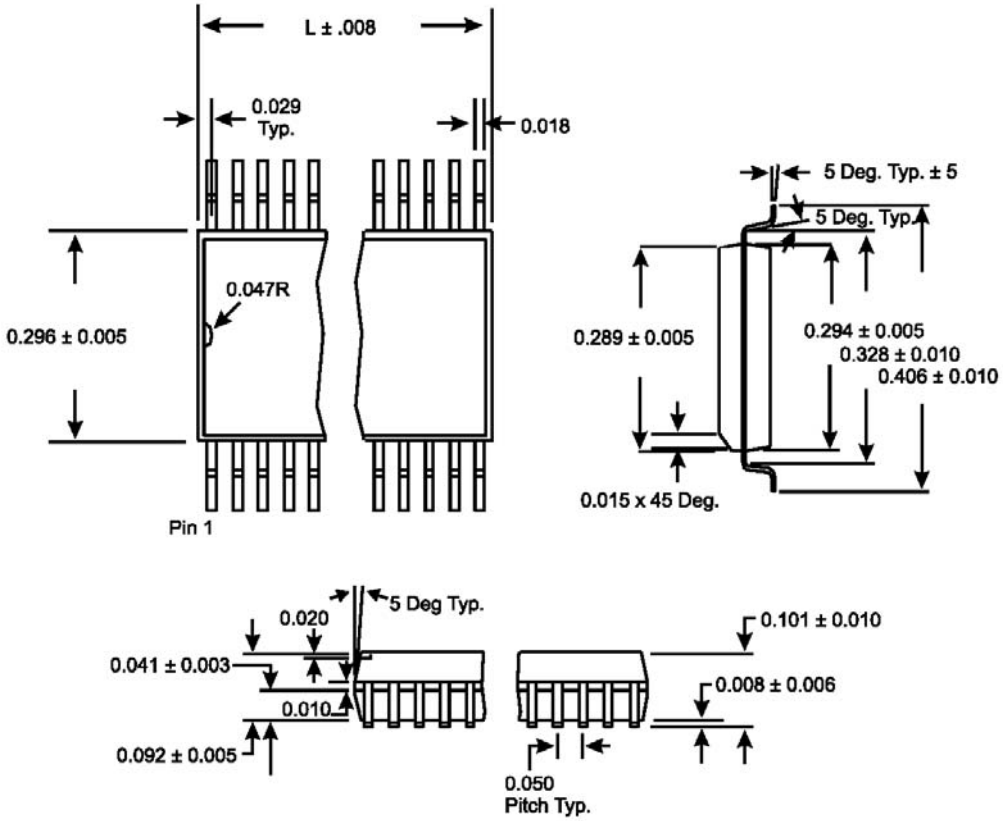
Typical Transition Times*

Symbol	Timing Description	Rise	Fall	Units
t_R	REF	2.8	1.8	ns
t_P	PECL CLK	1.0	1.2	ns
t_S	SSTL-CLK	1.6	0.7	ns
t_F	FUNC_OUT	1.2	1.0	ns

Output Timing*

Symbol	Timing Description	Min	Typ	Max	Units
t_0	HSYNC to REF delay	11.3	11.5	12	ns
t_1	REF to PECL clock delay	-1.0	0.8	2.2	ns
t_2, t_3	PECL clock duty cycle	45	50	55	%
t_4	PECL clock to SSTL_3 clock delay	0.2	0.75	1.2	ns
t_5	PECL clock to FUNC_OUT delay	1.5	1.9	2.3	ns
t_6	PECL clock to PECL/2 clock	1.0	1.3	1.5	ns
t_7	PECL clock to SSTL_3–CLK/2 delay	1.1	1.4	1.8	ns
t_8, t_9	SSTL clock duty cycle	45	50	55	%

*Note: Measured at 3.6V 0°C, 135-MHz output frequency, PECL clock lines to 75 Οηµ termination, SSTL_3 clock lines unterminated, 20-pF load. Transition times vary based on termination.



LEAD COUNT	24L
DIMENSION L	0.604

24-Pin SOIC (wide body)

Ordering Information			
Part/Order Number	**Marking**	**Package**	**Shipping**
ICS1524AMLF	1524AMLF	SIOC-24	Tubes
ICS1524AMLFT	1524AMLF	SIOC-24	Tape and Reel

NOTES

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