NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL9211B

DATASHEET

Charging System Safety Circuit

ISL9211A

The ISL9211A is an integrated circuit (IC) optimized to provide a redundant safety protection to a Li-ion battery charging system. The IC monitors the input voltage, the battery voltage, and the charge current. When any of the three parameters exceeds its limit, the IC turns off an internal N-channel MOSFET to remove the power from the charging system to the battery. In addition to the above protected parameters, the IC also monitors its own internal temperature and turns off the N-channel MOSFET when the temperature exceeds +150°C. Together with the battery charger IC and the protection module in a battery pack, the charging system using the ISL9211A has triple-level protection and is two-fault tolerant.

The IC is designed to turn on the internal NFET slowly to avoid inrush current at power up but will turn off the NFET quickly when the input is overvoltage in order to remove the power before any damage occurs. The ISL9211A has a logic flag output to indicate a fault condition. The enable input allows the system to cut off the input power if needed.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Features

- 24V Max Input Voltage
- Supports Up To 2.0A Input Current
- Fully Integrated Protection Circuit for Three Protected Variables
- High Accuracy Protection Thresholds
- User Programmable Overcurrent Protection Threshold
- Responds To Input Overvoltage in Less Than 1µs
- High Immunity of False Triggering Under Transients
- Fault Indication for Various Fault Occurrence
- Easy to Use
- Pb-Free (RoHS Compliant)

Applications

- Cell Phones
- Digital Still Cameras
- PDAs and Smart Phones
- Portable Instruments
- Desktop Chargers

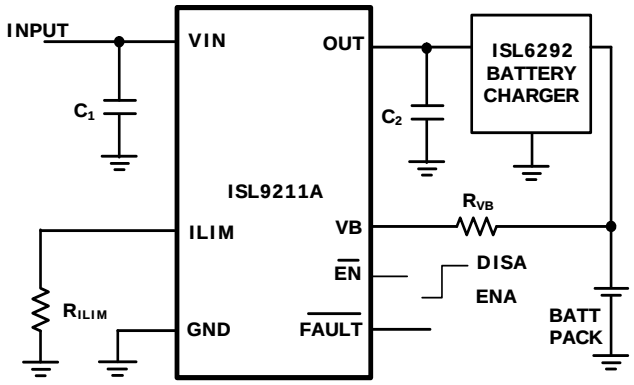
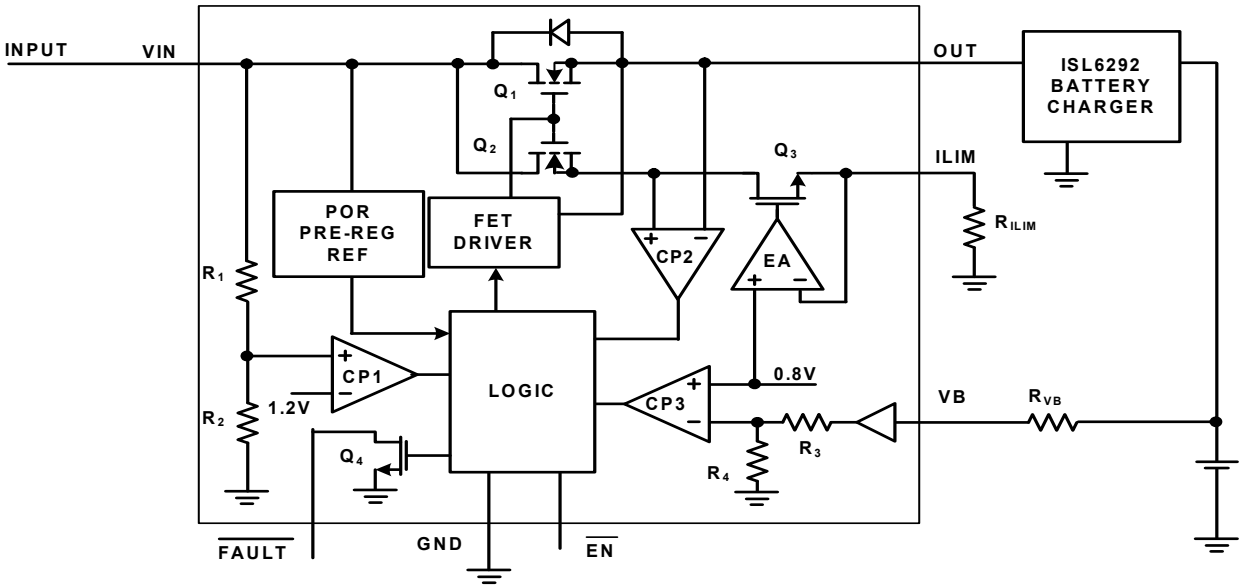


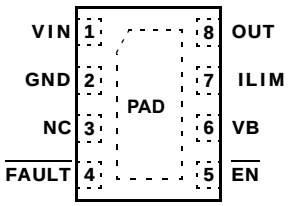
FIGURE 1. TYPICAL APPLICATION CIRCUIT

Block Diagram



Pin Configuration

ISL9211A
(8 LD µTDFN)
TOP VIEW



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VIN	1	The input power source. The VIN can withstand 24V input.
GND	2	System ground reference.
NC	3	No connection and must be left floating.
$\overline{\text{FAULT}}$	4	$\overline{\text{FAULT}}$ is an open-drain logic output that turns LOW when any protection event occurs.
$\overline{\text{EN}}$	5	IC enable pin. Pull this pin to LO to enable the device and pull it to HI to disable.
VB	6	Battery voltage monitoring input. This pin is connected to the battery pack positive terminal via an isolation resistor.
ILIM	7	Overcurrent protection threshold setting pin. Connect a resistor between this pin and GND to set the OCP threshold.
OUT	8	Output pin.
-	PAD	Exposed pad. Connect to system ground

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL9211AIRU48XZ-T	4XE	-40 to +85	8 Ld µTDFN	L8.2x2B
ISL9211AIRU58XZ-T	5XX	-40 to +85	8 Ld µTDFN	L8.2x2B
ISL9211AIRU68XZ-T	6XX	-40 to +85	8 Ld µTDFN	L8.2x2B
ISL9211AIRU48EVZ	Evaluation Board			
ISL9211AIRU58EVZ	Evaluation Board			
ISL9211AIRU68EVZ	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9211A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage (V_{IN}) . . . . . -0.3V to 26V
Output and VB Pin (OUT, VB) (Note 4) . . . . . -0.3V to 8V
Other Pins (ILIM, $\overline{FAULT}$, $\overline{EN}$) . . . . . -0.3V to 5.5V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 3kV
Machine Model (Tested per JESD22-A115-A) 200V
Latch Up (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld 2x2 µTDFN (Notes 5, 6)	98	37

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Supply Voltage, V_{IN} . . . . . 4.3V to 24V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. The maximum voltage rating for the VB pin under continuous operating conditions is 5.5V. All other pins are allowed to operate continuously at the absolute maximum ratings.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER-ON RESET						
V_{IN} Threshold	V_{POR}	Rising	-	-	2.47	V
		Falling	2.20	-	-	V
V_{IN} Bias Current	I_{VIN}	R_{ILIM} = 24.9k, $\overline{EN}$ = L	-	-	1000	µA
		$\overline{EN}$ = H	-	80	-	µA
PROTECTIONS						
Input Overvoltage Protection	V_{OVP}	ISL9211ARU48	4.6	4.8	5.0	V
		ISL9211ARU58	5.6	5.8	6.0	V
		ISL9211ARU68	6.6	6.8	7.0	V
Input OVP Hysteresis			-	100	-	mV
Input OVP Falling Threshold		ISL9211ARU48	4.55	-	-	V
		ISL9211ARU58	5.55	-	-	V
		ISL9211ARU68	6.55	-	-	V
Input OVP Response Time (Note 7)			-	-	1	µs
Overcurrent Protection	I_{OCP}	V_{VB} = 3V, R_{ILIM} = 24.9kΩ	0.93	1.0	1.07	A
Maximum Output Current	I_{MAX}	R_{ILIM} = 9.53kΩ	-	2.0	-	A
Overcurrent Protection Blanking Time	BT_{OCP}		-	180	-	µs
Battery Overvoltage Protection Threshold	V_{BOVP}		4.25	4.34	4.40	V
Battery OVP Threshold Hysteresis			-	30	-	mV
Battery OVP Blanking Time	BT_{BOVP}		-	180	-	µs
VB Pin Leakage Current		V_{VB} = 4.34V	-	-	20	nA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Over-Temperature Protection Rising Threshold			-	150	-	°C
Over-Temperature Protection Falling Threshold			-	110	-	°C
LOGIC						
$\overline{EN}$ Input Logic HIGH			1.5	-	-	V
$\overline{EN}$ Input Logic LOW			-	-	0.4	V
$\overline{EN}$ Internal Pull-down Resistor			-	200	-	kΩ
$\overline{FAULT}$ Output Logic Low		Sink 5mA current	-	0.4	0.8	V
$\overline{FAULT}$ Output Logic High Leakage Current		Pin Voltage = 4.2V	-	-	1.5	µA
POWER MOSFET						
On-Resistance (Note 7)	$r_{DS(ON)}$	Measured at 200mA	-	170	280	mΩ

NOTES:

7. Limits should be considered typical and are not production tested.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application

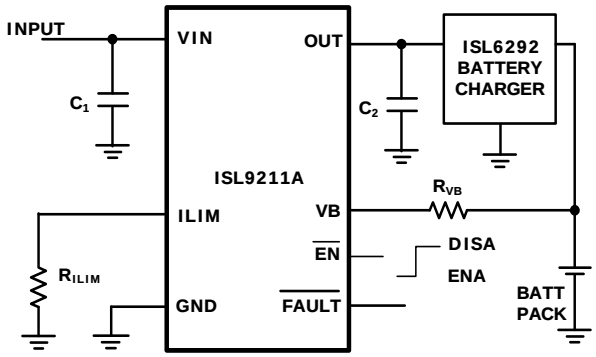
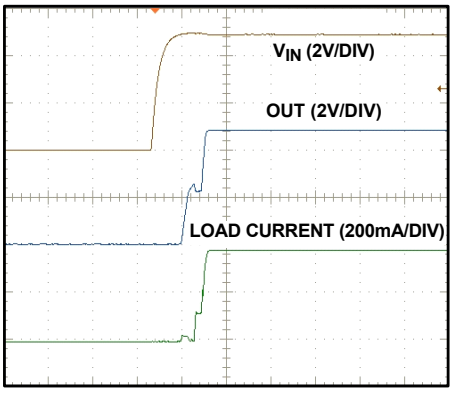


TABLE 1. TYPICAL COMPONENT VALUES

PART	DESCRIPTION
R_{ILIM}	24.9kΩ
R_{VB}	200kΩ to 1MΩ
C_1, C_2	1µF/25V X5R ceramic capacitor

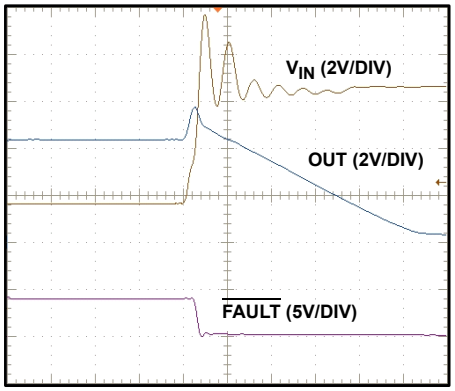
Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ILIM} = 24.9kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted.



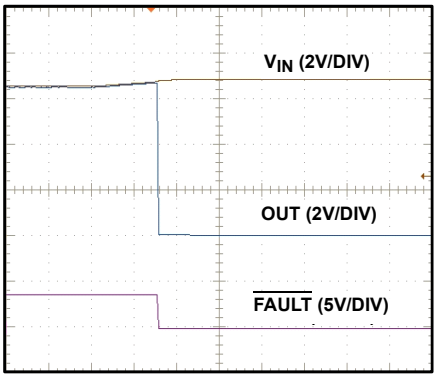
TIME - 4ms/DIV

FIGURE 2. CAPTURED WAVEFORMS FOR POWER-UP. THE OUTPUT IS LOADED WITH A 10Ω RESISTOR



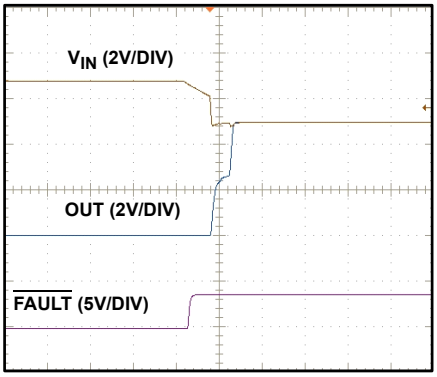
TIME - 20µs/DIV

FIGURE 3. CAPTURED WAVEFORMS WHEN THE INPUT VOLTAGE STEPS FROM 5.5V TO 9.5V



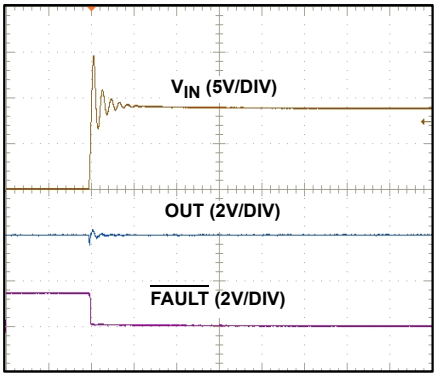
TIME - 2s/DIV

FIGURE 4. CAPTURED WAVEFORMS WHEN THE INPUT GRADUALLY RISES TO THE INPUT OVERVOLTAGE THRESHOLD



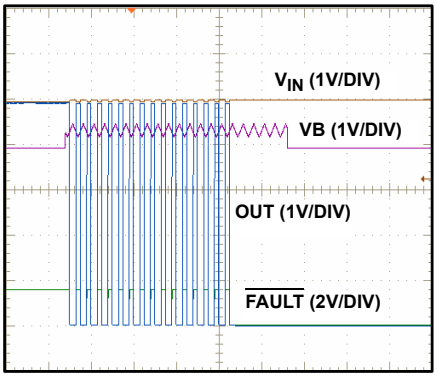
TIME - 4ms/DIV

FIGURE 5. TRANSIENT WHEN THE INPUT VOLTAGE STEPS FROM 6.5V TO 5.5V



TIME - 40µs/DIV

FIGURE 6. TRANSIENT WAVEFORMS WHEN INPUT STEPS FROM 0V TO 9V



TIME - 20s/DIV

FIGURE 7. BATTERY OVERVOLTAGE PROTECTION. THE IC IS LATCHED OFF AFTER 16 COUNTS OF PROTECTION. VB VOLTAGE VARIES BETWEEN 4.3V TO 4.5V

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ILIM} = 24.9kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted. *(Continued)*

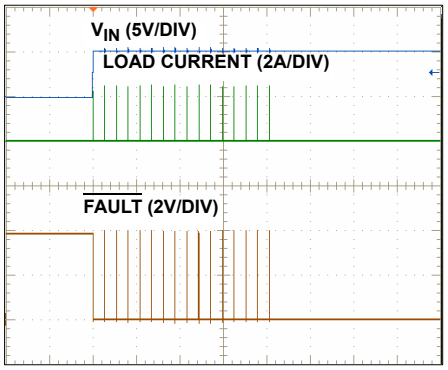


FIGURE 8. POWER-UP WAVEFORMS WHEN OUTPUT IS SHORT-CIRCUITED

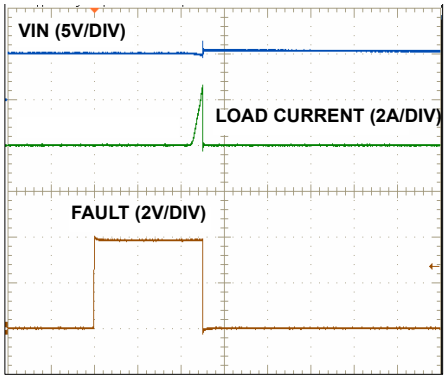


FIGURE 9. ZOOMED-IN VIEW OF FIGURE 8

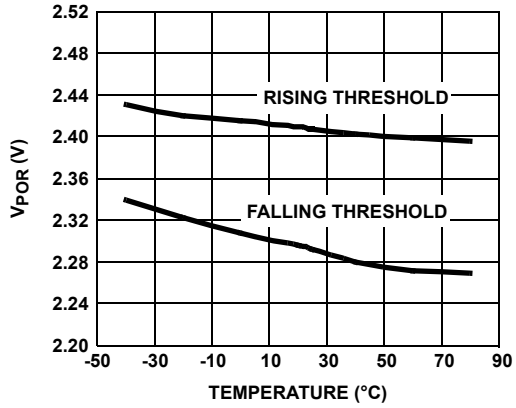


FIGURE 10. V_{POR} vs TEMPERATURE

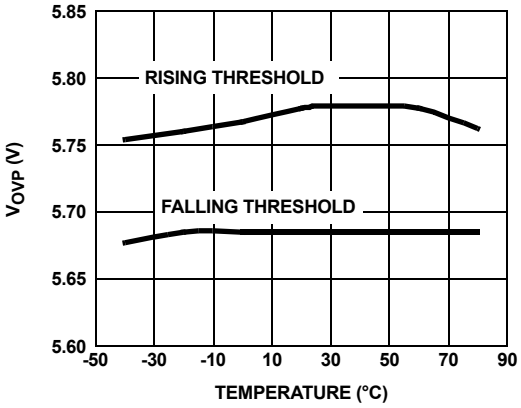


FIGURE 11. INPUT OVERVOLTAGE PROTECTION vs TEMPERATURE

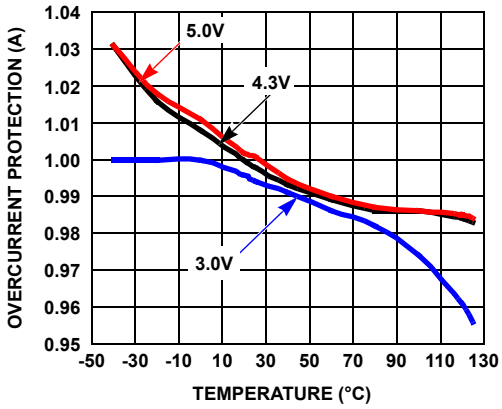


FIGURE 12. OVERCURRENT PROTECTION vs TEMPERATURE AT VARIOUS INPUT VOLTAGES

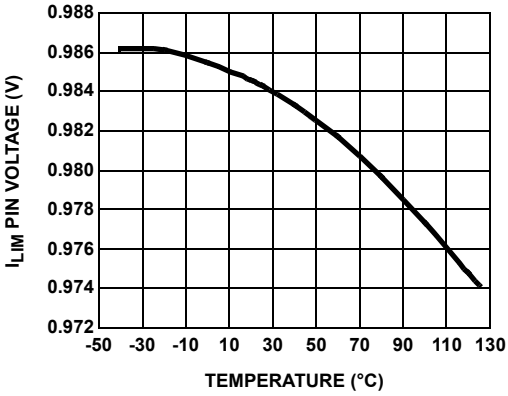


FIGURE 13. I_{LIM} PIN VOLTAGE vs TEMPERATURE

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{ILIM} = 24.9kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted. *(Continued)*

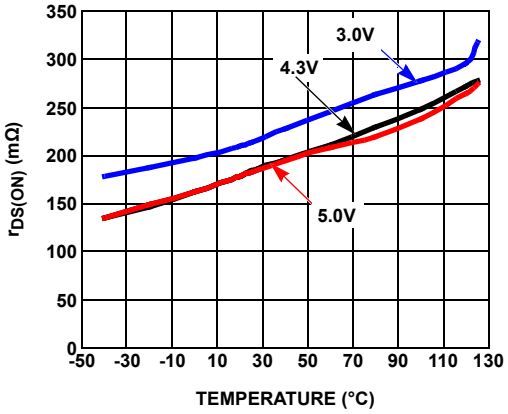


FIGURE 14. ON-RESISTANCE vs TEMPERATURE AT DIFFERENT INPUT VOLTAGES

Theory of Operation

The ISL9211A is an integrated circuit (IC) optimized to provide a redundant safety protection to a Li-ion battery from charging system failures. The IC monitors the input voltage, the battery voltage, and the charge current. When any of the above three parameters exceeds its limit, the IC turns off an internal N-channel MOSFET to remove the power from the charging system. In addition to the above protected parameters, the IC also monitors its own internal temperature and turns off the N-channel MOSFET when the temperature exceeds +150°C. Together with the battery charger IC and the protection module in a battery pack, the charging system has triple-level protection from overcharging the Li-ion battery and is two-fault tolerant. The ISL9211A protects up to 26V input voltage.

Power-Up

The ISL9211A has a power-on reset (POR) threshold of 2.47V (max). Before the input voltage reaches the POR threshold, the internal power NFET is off. Approximately 10ms after the input voltage exceeds the POR threshold, the IC resets itself and begins the soft-start. The 10ms delay allows any transients at the input during a hot insertion of the power supply to settle down before the IC starts to operate. The soft-start slowly turns on the power NFET to reduce the inrush current as well as the input voltage drop during the transition. The power-up sequence is illustrated in Figure 2.

Input Overvoltage Protection (OVP)

The input voltage is monitored by the comparator CP1 in the "Block Diagram" on page 2. CP1 has an accurate reference of 1.2V from the bandgap reference. The OVP threshold is set by the resistive divider consisting of R_1 and R_2. When the input voltage exceeds the threshold, the CP1 outputs a logic signal to turn off the power NFET within 1µs (see Figure 3) to prevent the high input voltage from damaging the electronics in the handheld system. The hysteresis for the input OVP threshold is given in the "Electrical Specifications" table on page 4. When the input overvoltage condition is removed, the ISL9211A re-enables the output by running through the soft-start, as shown in Figure 5.

Because of the 10ms second delay before the soft-start, the output is never enabled if the input rises above the OVP threshold quickly, as shown in Figure 6.

Battery Overvoltage Protection

The battery voltage OVP is realized with the VB pin. The comparator CP3, as shown in the "Block Diagram" on page 2, monitors the VB pin and issues an overvoltage signal when the battery voltage exceeds the 4.34V battery OVP threshold. The threshold has 30mV built-in hysteresis. The comparator CP3 has a built-in 180µs blanking time to prevent any transient voltage from triggering the OVP. If the OVP situation still exists after the blanking time, the power NFET is turned off. The control logic contains a 4-bit binary counter that if the battery overvoltage event occurs 16 times, the power NFET is turned off permanently, as shown in Figure 7. Recycling the input power will reset the counter and restart the ISL9211A.

The resistor between the VB pin and the battery, R_{VB}, as shown in the "TYPICAL APPLICATION CIRCUIT" on page 1, is an important component. This resistor provides a current limit in case the VB pin is shorted to the input voltage under a failure mode. The VB pin leakage current under normal operation is negligible to allow a resistance of 200kΩ to 1MΩ be used.

Overcurrent Protection (OCP)

The current in the power NFET is limited to prevent charging the battery with an excessive current. The current is sensed using the voltage drop across the power FET after it is turned on. The reference of the OCP is generated using a sensing FET Q_2 (Mirror to Q_1), as shown in the "Block Diagram" on page 2. The current in the sensing FET is forced to match the value programmed by I_{LIM} pin. The OCP threshold can be set with the resistor R_{LIM}, as shown in Table 2.

TABLE 2. R_{LIM} VALUE vs OCP THRESHOLD

R_{LIM} (kΩ)	OCP (mA)	R_{LIM} (kΩ)	OCP (mA)
82.5	300	21	1200
61.9	400	19.1	1300
49.9	500	16.5	1400
41.2	600	15.4	1500
35.7	700	14	1600
31.6	800	12.4	1700
28	900	11.3	1800
24.9	1000	10.5	1900
22.6	1100	9.53	2000

The size of the power FET Q_1 is 31,250 times the size of the sensing FET. Therefore, when the current in the power FET is 31,250 times the current in the sensing FET, the drain voltage of the power FET falls below that of the sensing FET. The comparator CP2 then outputs a signal to turn off the power FET, where the 0.8V is the regulated reference voltage at the ILIM pin. The OCP comparator CP2 has a built-in 180µs delay to prevent false triggering by transient signals. The OCP function also has a 4-bit binary counter that accumulates during an OCP event. When the total count reaches 16, the power NFET is turned off permanently until the input power is recycled or the enable pin is toggled. Figures 8 and 9 illustrate the waveforms during the power-up when the output is shorted to ground.

Internal Over-Temperature Protection

The ISL9211A monitors its own internal temperature to prevent thermal failures. When the internal temperature reaches +150°C, the IC turns off the N-channel power MOSFET. The IC does not resume operation until the internal temperature drops below +110°C.

Fault Indication Output

The $\overline{FAULT}$ pin is an open-drain output that indicates a LOW signal when any of the three fault events happens. This provides a signal to the microprocessor to take further action to enhance the safety of the charging system.

Applications Information

The ISL9211A is designed to meet the "Lithium-Safe" criteria when operating together with a qualified Li-ion battery charger. The "Lithium-Safe" criteria requires the charger output to fall within the green region shown in Figure 15 under normal operating conditions and NOT to fall in the red region when there is a single fault in the charging system. Taking into account the safety circuit in a Li-ion battery pack, the charging system is allowed to have two faults without creating hazardous conditions for the battery cell. The output of the Li-ion charger, such as the ISL6292C, has a typical I-V curve shown with the blue lines under normal operation, which is within the green region. The function of the ISL9211A is to add a redundant protection layer such that, under any single fault condition, the charging system output does not exceed the I-V limits shown with the red lines. As a result, the charging system adopting the ISL9211A and the ISL6292C chip set can easily pass the "Lithium-Safe" criteria test procedures.

The ISL9211A is a simple device that requires only three external components, in addition to the ISL6292 charger circuit, to meet the "Lithium-Safe" criteria, as shown in the "TYPICAL APPLICATION CIRCUIT" on page 1. The selection of the current limit resistor R_{ILIM} is given in "Overcurrent Protection (OCP)" on page 8.

R_{VB} Selection

The R_{VB} prevents a large current from the VB pin to the battery terminal, in case the ISL9211A fails. The recommended value should be between 200kΩ to 1MΩ. With 200kΩ resistance, the worst case current flowing from the VB pin to the charger output is shown in Equation 1, assuming the VB pin voltage is 24V under a failure mode and the battery voltage is 4.2V.

$$(24V - 4.2V)/(200k\Omega) = 99\mu A \quad \text{(EQ. 1)}$$

Such a small current can be easily absorbed by the bias current of other components in the handheld system. Increasing the R_{VB} value reduces the worst case current, but at the same time increases the error for the 4.34V battery OVP threshold.

The error of the battery OVP threshold is the original accuracy at the VB pin given in the "Electrical Specifications" table on page 4 plus the voltage built across the R_{VB} by the VB pin leakage current. The VB pin leakage current is less than 20nA, as given in the "Electrical Specifications" table on page 4. With the 200kΩ resistor, the worst-case additional error is 4mV and with a 1MΩ resistor, the worst-case additional error is 20mV.

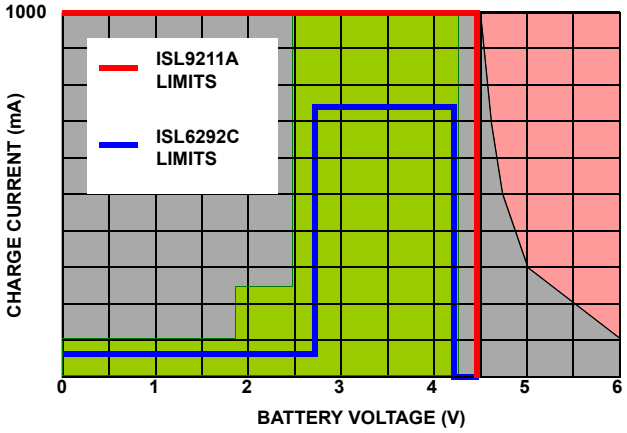


FIGURE 15. LITHIUM-SAFE OPERATING REGIONS

Capacitor Selection

The input capacitor (C_1 in the "TYPICAL APPLICATION CIRCUIT" on page 1) is for decoupling. Higher value reduces the voltage drop or the over-shoot during transients.

Two scenarios can cause the input voltage over-shoot. The first one is when the AC adapter is inserted live (hot insertion) and the second one is when the current in the power NFET of the ISL9211A has a step-down change. Figure 16 shows an equivalent circuit for the ISL9211A input. The cable between the AC/DC converter output and the handheld system input has a parasitic inductor. The parasitic resistor is the lumped sum of

various components, such as the cable, the adapter output capacitor ESR, the connector contact resistance, and so on.

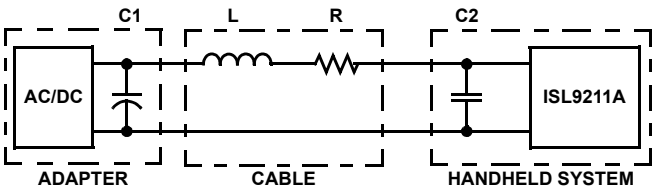


FIGURE 16. EQUIVALENT CIRCUIT FOR THE ISL9211A INPUT

During the load current step-down transient, the energy stored in the parasitic inductor is used to charge the input decoupling capacitor C_2. The ISL9211A is designed to turn off the power NFET slowly during the OCP and the battery OVP event. Because of such design, the input over-shoot during those events is not significant. During an input OVP, however, the NFET is turned in less than 1µs and can lead to significant over-shoot. Higher capacitance reduces the over-shoot.

The over-shoot caused by a hot insertion is not very dependent on the decoupling capacitance value. Especially when ceramic type capacitors are used for decoupling. In theory, the over-shoot can rise up to twice of the DC output voltage of the AC adapter. The actual peak voltage is dependent on the damping factor that is mainly determined by the parasitic resistance (R in Figure 16).

In practice, the input decoupling capacitor is recommended to use a 25V, X5R dielectric ceramic capacitor with a value between 0.1µF to 1µF.

The output of the ISL9211A and the input of the charging circuit typically share one decoupling capacitor. The selection of that capacitor is mainly determined by the requirement of the charging circuit. When using the ISL6292 family chargers, a 1µF, 6.3V, X5R capacitor is recommended.

Layout Recommendation

The ISL9211A uses a thermal-enhanced TDFN package with an exposed thermal pad at the bottom of the package. The layout should include as much copper as possible beneath the exposed pad on the component layer to improve thermal performance. The exposed pad under the package should be connected to the ground plane electrically as well as thermally. The vias should be about 0.3mm to 0.33mm in diameter, use as many vias as possible to fit in the exposed pad area.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
January 29, 2014	FN6702.3	Page 3, updated note 2 for the ordering information to reflect the correct finish used.
November 22, 2013	FN6702.2	Page 3, added evaluation boards to “Ordering Information”. Page 3, pinout and pin descriptions, changed $\overline{\text{ILIM}}$ to ILIM Page 4, “Absolute Maximum Ratings” table, changed $\overline{\text{ILIM}}$ to ILIM Page 9, paragraph after Table 2, changed $\overline{\text{ILIM}}$ to ILIM
May 5, 2010	FN6702.1	In Table 2 on page 9, changed layout from: 2 columns to 4 columns. In “Electrical Specifications” table on page 4, changed the test conditions for “Maximum Output Current” from “Rlim = 12.4k” to “Rlim = 9.53k”.
March 30, 2010		Converted to new Intersil template. Edits include: Moved “Block Diagram” to page 2, “Pin Configuration” to page 3, “Ordering Information” to page 3 and “TYPICAL APPLICATION CIRCUIT” on page 1. Added MSL Note 3 and TB347 Note 1 to “Ordering Information” on page 3. Converted “Pin Descriptions” to tabular format and moved after “Pin Configuration” on page 3. Added Exposed Pad to “Pin Descriptions” on page 3. Added PAD label to “Pin Configuration” on page 3. Added “ESD Rating” on page 4. Added “Latch up” to page 4. Moved “Parameters with MIN and Max..” in common conditions of “Electrical Specifications” table to Note 8 in MIN MAX columns. Removed the following from “Overcurrent Protection (OCP)” on page 9: “The OCP threshold can be calculated using Equation 1: ILIM = 0.8V/RILIM x 31250 - 25000/RILIM (EQ. 1)” Added Table 2 to page 9 and following sentence to“Overcurrent Protection (OCP)” on page 9: “The OCP threshold can be set with the resistor RLIM as shown in Table 2." Added “Revision History” on page 11 .
April 2, 2009	FN6702.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

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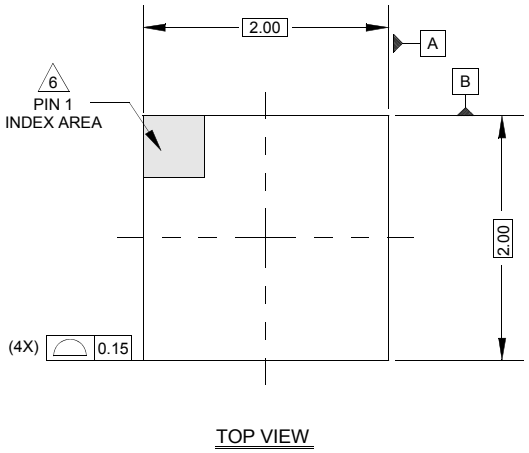
Package Outline Drawing

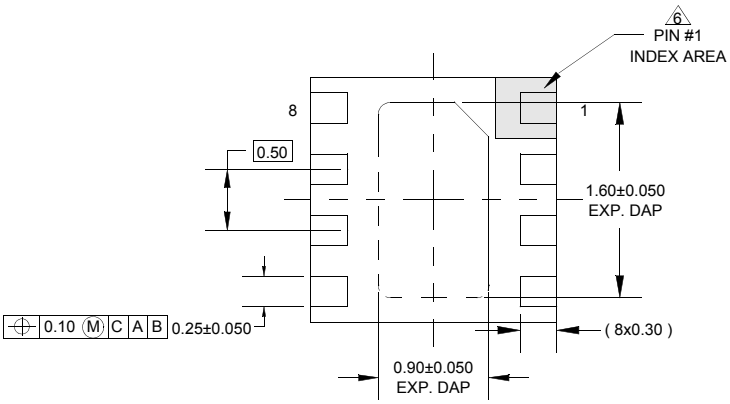
L8.2x2B

8 LEAD MICRO THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (µTDFN) WITH E-PAD

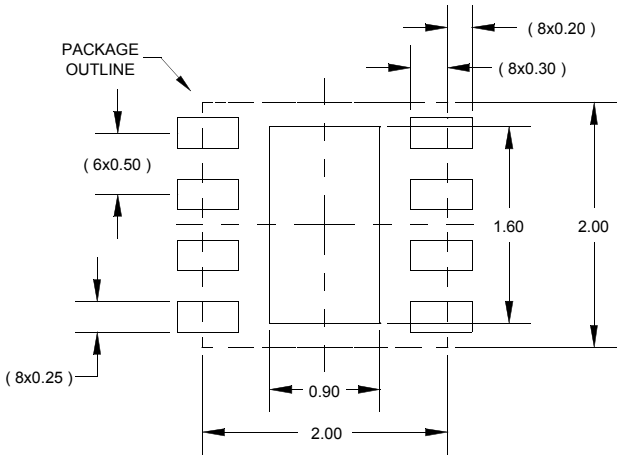
Rev 0, 04/08



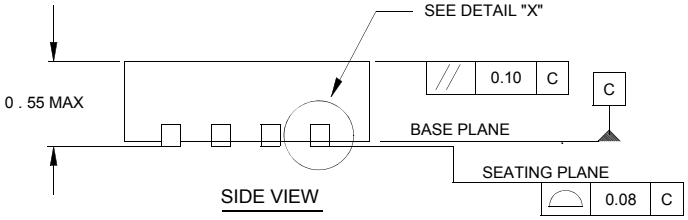
TOP VIEW



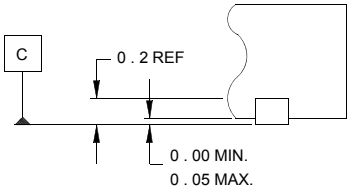
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.