



SY56040AR

Low Voltage 1.2V/1.8V/2.5V CML 4x4
Crosspoint Switch 6.4Gbps, 5GHz

General Description

The SY56040AR is a fully differential, low voltage 1.2V/1.8V/2.5V CML 4x4 Crosspoint switch. The SY56040AR can process clock signals as fast as 5GHz or data patterns up to 6.4Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals as small as 100mV (200mV_{pp}) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V_T pin. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY56040AR operates from a 2.5V ±5% core supply and a 1.2V/1.8V/2.5V ±5% output supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY56040AR is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.



Precision Edge[®]

Features

- 1.2V/1.8V/2.5V CML 4x4 Crosspoint Switch
- Guaranteed AC performance over temperature and voltage:
 - DC to 6.4Gbps throughput
 - <400ps typical propagation delay (IN-to-Q)
 - <25ps typical output skew
 - <80ps rise/fall times
- Ultra-low jitter design
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{PP} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
- High-speed CML outputs
- 2.5V ±5% , 1.2V/1.8V/2.5V ±5% power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 44-pin (7mm x 7mm) MLF[®] package

Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

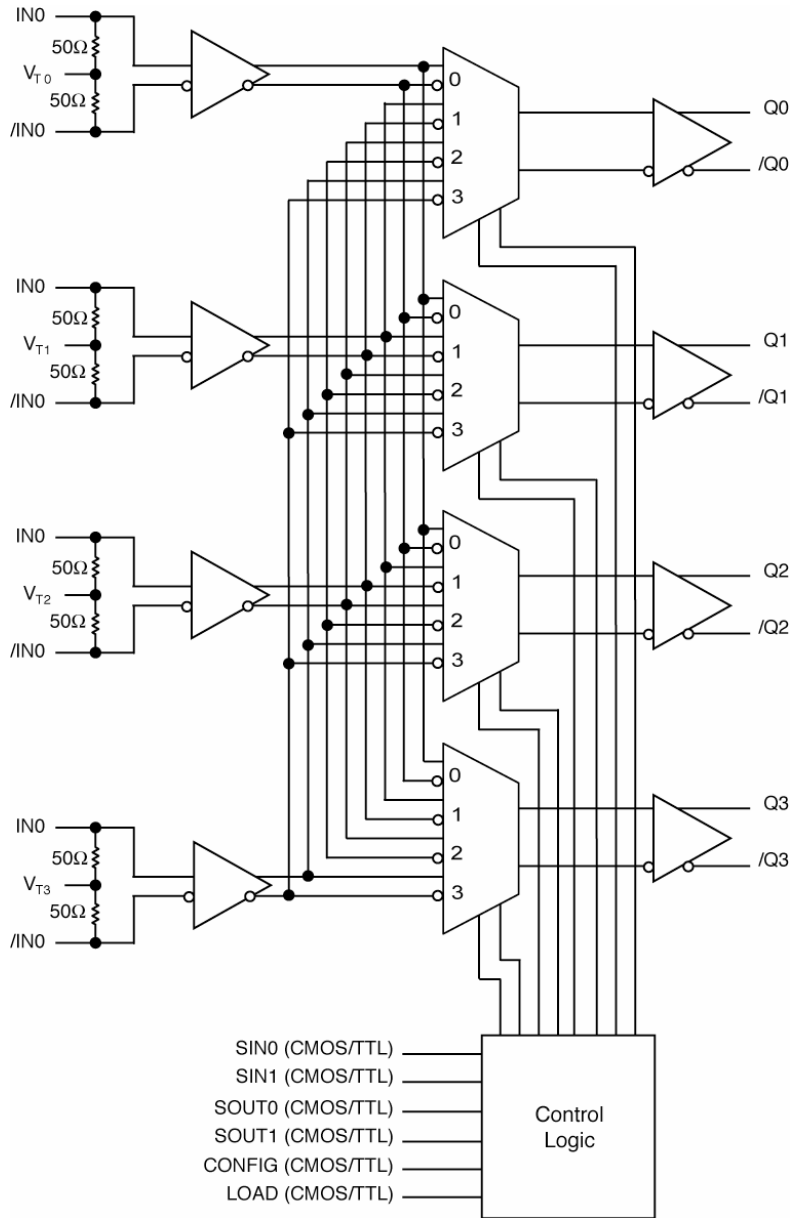
Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

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Functional Block Diagram



Truth Table

| Input Select Address Table | | |
|----------------------------|------|-------|
| SIN1 | SIN0 | INPUT |
| 0 | 0 | IN0 |
| 0 | 1 | IN1 |
| 1 | 0 | IN2 |
| 1 | 1 | IN3 |

| Output Select Address Table | | |
|-----------------------------|-------|--------|
| SOUT1 | SOUT0 | OUTPUT |
| 0 | 0 | Q0 |
| 0 | 1 | Q1 |
| 1 | 0 | Q2 |
| 1 | 1 | Q3 |

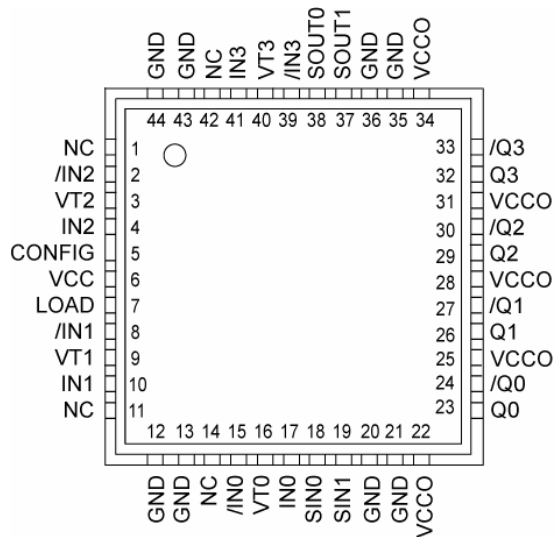
Ordering Information ⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|------------------------------|--------------|-----------------|---|-------------|
| SY56040ARMY | MLF-44 | Industrial | SY56040ARMY with Pb-Free bar-line indicator | Matte-Sn |
| SY56040ARMYTR ⁽²⁾ | MLF-44 | Industrial | SY56040ARMY with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only
2. Tape and Reel.

Pin Configuration



44-Pin MLF[®] (MLF-44)

Pin Description

| Pin Number | Pin Name | Pin Function |
|----------------------------------|---|---|
| 17,15 10,8 4,2 41,39 | IN0, /IN0 IN1, /IN1 IN2, /IN IN3, /IN3 | Differential Inputs: These input pairs are the differential signal inputs to the device. They accept differential signals as small as 100mV (200mV _{PP}). Each input pin internally terminates with 50Ω to the VT pin. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Interface Applications" section for more details. |
| 16 9 3 40 | VT0 VT1 VT2 VT3 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC-coupling. For AC-coupling, bypass VT with a 0.1μF low ESR capacitor to VCC. See "Interface Applications" subsection and Figure 2a. |
| 18 19 | SIN0 SIN1 | These single-ended TTL/CMOS-compatible inputs address the data inputs during switch configuration. Note that this input is internally connected to a 25k ohm pull-up resistor and will default to a logic HIGH state if left open. |
| 38 37 | SOUT0 SOUT1 | These single-ended TTL/CMOS-compatible inputs address the data outputs during switch configuration. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. |
| 5 7 | CONFIG LOAD | <p>These single-ended TTL/CMOS-compatible inputs control the transfer of the addresses defined by SIN0/1 and SOUT0/1. See "Switch Configuration," "Address Table" and "Timing Diagram" sections for more details. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open.</p> <ol style="list-style-type: none"> 1. Load: Loads configurations into first set of latches. After programming SIN and SOUT with input and output address respectively, pulse the LOAD signal with a Low to High to Low signal to <u>latch</u> SIN and SOUT. Four LOAD pulses are needed, each LOAD pulse for each output. See simplified control circuit and switch configuration description on page 9 for further clarification. 2. CONFIG: Loads new configuration into the second set of latches and updates switch configuration. After Loading, pulse CONFIG with a Low to High to Low signal to load/transfer the latched signal to the output. See simplified control circuit and switch configuration description on Page 9 for further clarification. <p>If the LOAD and CONFIG control signals are floating, one of the output pairs is set by the programmed SIN and SOUT addresses, as shown in address tables. For the remaining outputs, setup is random at power up or from previous programmed states.</p> |
| 23,24 26,27 29,30 32,33 | Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 | CML Differential Output Pairs: Differential buffered copy of the selected input signal. The output swing is typically 390mV. See "Interface Application" subsection for termination information. |
| 6 | VCC | Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V _{CC} pin as possible. Supplies input and core circuitry. |
| 22,25,28,31,34 | VCCO | Output Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V _{CCO} pins as possible. Supplies the output buffer. |
| 12,13,20,21,35, 36,43,44 | GND, Exposed pad | Ground: Exposed pad must be connected to a ground plane that is at the same potential as the ground pin. |
| 1,11,14,42 | NC | Not Connected. |

Absolute Maximum Ratings⁽¹⁾

| | | |
|--|-------|--------------------------|
| Supply Voltage (V_{CC}) | | -0.5V to +3.0V |
| Supply Voltage (V_{CCO}) | | -0.5V to +2.7V |
| $V_{CC} - V_{CCO}$ | | <1.8V |
| $V_{CCO} - V_{CC}$ | | <0.5V |
| Input Voltage (V_{IN}) | | -0.5V to $V_{CC} + 0.5V$ |
| CML Output Voltage (V_{OUT}) | | 0.6V to $V_{CCO} + 0.5V$ |
| Current (I_T) | | |
| Source or sink current on VT pin | | $\pm 100mA$ |
| Input Current | | |
| Source or sink current on (IN, /IN) | | $\pm 50mA$ |
| Maximum Operating Junction Temperature | | 125°C |
| Lead Temperature (soldering, 20sec.) | | 260°C |
| Storage Temperature (T_s) | | -65°C to +150°C |

Operating Ratings⁽²⁾

| | | |
|---|-------|------------------|
| Supply Voltage (V_{CC}) | | 2.375V to 2.625V |
| (V_{CCO}) | | 1.14V to 2.625V |
| Ambient Temperature (T_A) | | -40°C to +85°C |
| Package Thermal Resistance ⁽³⁾ | | |
| MLF [®] | | |
| Still-air (θ_{JA}) | | 40°C/W |
| Junction-to-board (ψ_{JB}) | | 20°C/W |

DC Electrical Characteristics⁽⁴⁾

$T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|--|-------|-----|----------------|----------|
| V_{CC} | Power Supply Voltage Range | V_{CC} | 2.375 | 2.5 | 2.625 | V |
| | | V_{CCO} | 1.14 | 1.2 | 1.26 | V |
| | | V_{CCO} | 1.7 | 1.8 | 1.9 | V |
| | | V_{CCO} | 2.375 | 2.5 | 2.625 | V |
| I_{CC} | Power Supply Current | Max. V_{CC} | | 155 | 200 | mA |
| I_{CCO} | Power Supply Current | No Load. Max. V_{CCO} | | 64 | 84 | mA |
| R_{IN} | Input Resistance (IN-to- V_T , /IN-to- V_T) | | 45 | 50 | 55 | Ω |
| R_{DIFF_IN} | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input HIGH Voltage (IN, /IN) | IN, /IN | 1.2 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, /IN) | V_{IL} with $V_{IHMIN} = 1.2V$ | 0.2 | | $V_{IH} - 0.1$ | V |
| V_{IH} | Input HIGH Voltage (IN, /IN) | IN, /IN | 1.14 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage (IN, /IN) | V_{IL} with $V_{IHMIN} = 1.14V (1.2V-5\%)$ | 0.66 | | $V_{IH} - 0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, /IN) | see Figure 3a | 0.1 | | 1.0 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing (IN - /IN) | see Figure 3b | 0.2 | | 2.0 | V |
| V_{T_IN} | Voltage from Input to V_T | | | | 1.28 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

CML Outputs DC Electrical Characteristics⁽⁵⁾

$V_{CCO} = 1.14V$ to $1.26V$, $R_L = 50\Omega$ to V_{CCO} ,

$V_{CCO} = 1.7V$ to $1.9V$; $2.375V$ to $2.625V$, $R_L = 50\Omega$ to V_{CCO} or 100Ω across the outputs.

$V_{CC} = 2.375V$ to $2.625V$. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|-----------------------------------|-------------------------------|-----------------|-----------------|-----------|----------|
| V_{OH} | Output HIGH Voltage | $R_L = 50\Omega$ to V_{CCO} | $V_{CCO}-0.020$ | $V_{CCO}-0.010$ | V_{CCO} | V |
| V_{OUT} | Output Voltage Swing | See Figure 3a | 300 | 390 | 475 | mV |
| V_{DIFF_OUT} | Differential Output Voltage Swing | See Figure 3b | 600 | 780 | 950 | mV |
| R_{OUT} | Output Source Impedance | | 45 | 50 | 55 | Ω |

LVTTL/CMOS DC Electrical Characteristics⁽⁵⁾

$V_{CC} = 2.5V \pm 5\%$. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|----------|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | V_{CC} | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | Input HIGH Current | | -125 | | 30 | μA |
| I_{IL} | Input LOW Current | | -300 | | | μA |

Note:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics ⁽⁶⁾

$V_{CC0} = 1.14V$ to $1.26V$, $R_L = 50\Omega$ to V_{CC0} .

$V_{CC0} = 1.7V$ to $1.9V$, $2.375V$ to $2.625V$, $R_L = 50\Omega$ to V_{CC0} or 100Ω across the outputs.

$V_{CC} = 2.375V$ to $2.625V$. $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units | |
|--------------|---|------------------------------|--------------------------|------|-----|---------------|---------------|
| f_{MAX} | Maximum Data Rate/ Frequency | NRZ Data | 6.4 | | | Gbps | |
| | | $V_{OUT} > 200mV$ Clock | 5 | | | GHz | |
| t_{PD} | Propagation Delay | IN-to-Q | 200 | 290 | 400 | ps | |
| | | CONFIG-to-Q | | 450 | | ps | |
| | | LOAD/CONFIG-Q | | 850 | | ps | |
| t_{PW} | Pulse Width of LOAD/CONFIG signal | | 1500 | | | ps | |
| t_s | Set-up Time | SIN-to-LOAD | Note 7, Fig. 1b, Fig. 1c | 600 | | | ps |
| | | SIN-to-LOAD/CONFIG | | 600 | | | |
| | | SOUT-to-LOAD | | 800 | | | |
| | | SOUT-to-LOAD/CONFIG | | 800 | | | |
| | | LOAD-to-CONFIG | | 1400 | | | |
| | | CONFIG-to-LOAD | | 300 | | | |
| t_H | Hold time | LOAD-to-SIN | Note 8, Fig. 1b, Fig. 1c | 800 | | | ps |
| | | LOAD/CONFIG-to-SIN | | 500 | | | |
| | | LOAD-to-SOUT | | 600 | | | |
| | | LOAD/CONFIG-to-SOUT | | 500 | | | |
| t_{Skew} | Input-to-Input skew | Note 9 | | 25 | 50 | ps | |
| | Output-to-Output skew | Note 10 | | 12 | 25 | ps | |
| | Part-to-Part Skew | Note 11 | | | 75 | ps | |
| t_{Jitter} | Data | Random Jitter | Note 12 | | 1 | μS_{RMS} | |
| | | Deterministic Jitter | Note 13 | | 10 | μS_{PP} | |
| | Clock | Cycle-to-Cycle Jitter | Note 14 | | | 1 | μS_{RMS} |
| | | Total Jitter | Note 15 | | | 10 | μS_{PP} |
| | Crosstalk Induced Jitter (Adjacent Channel) | Note 16 | | | 0.7 | μS_{PP} | |
| t_R, t_F | Output Rise/Fall Times (20% to 80%) | At full output swing. | 20 | 50 | 80 | ps | |
| | Duty Cycle | Differential I/O $\leq 4GHz$ | | 47 | 53 | % | |
| | | Differential I/O $\leq 5GHz$ | | 45 | 55 | % | |

Notes:

- High frequency AC electrical values are guaranteed by design and characterization.
- Set-up time is the time a signal has to be present before the rising edge of the clock /control signal comes by. For example, t_s (SIN-LOAD/CONFIG), requires the time SIN has to transition before the L-H edge of the LOAD/CONFIG signal asserts.
- Hold time is the time a signal has to be present after the falling edge of the clock edge/control signal comes by. For example, t_H (LOAD/CONFIG-SIN) defines the time SIN signal has to transition after the H-L edge of the LOAD/CONFIG signal asserts.
- Input-to-Input skew is the difference in time between 4 inputs, measured at the same output, for the same temperature, voltage, and transition.
- Output-to-Output skew is the difference in time between 4 outputs, receiving data from the same input, for the same temperature, voltage and transition.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
- Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
- Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
- Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk induced jitter is defined as the added jitter that results from signals applied to the adjacent channel. It is measured at the output. While applying a similar, differential clock frequency to both inputs that is asynchronous with respect to each other.

Switch Configuration

As shown in the Simplified Control Circuit below, Figure 1a, each output channel consists of two sets of latches. The first set of latches stores the SIN information for each SOUT selected. The second set of latches transfers this stored information to the output MUX circuitry. These latches are transparent when EN is high and latched when EN is low.

Two pins, LOAD and CONFIG, control the programming. LOAD is ANDed with the SOUT pins to route the SIN data to the appropriate first set of latches. CONFIG subsequently transfers the information in the first set of latches to the second set of latches, which is connected to the output MUX circuitry.

There are two ways to program this device. The first is a Dual Control Mode, as shown in Figure 1b. First, all the input-output (SIN-SOUT) information is loaded. Second, this information is transferred to the output control circuitry. Each LOAD pulse loads the input information (SIN) to be assigned to the output (SOUT). In maximum, four LOAD pulses are applied, one LOAD pulse for each output. Note that LOAD pulses are necessary only for undefined and/or modified input-output combinations. After all the input-output information is loaded, the CONFIG is pulsed to transfer and latch this information to the output control circuitry.

The second programming method is the Single Control Mode, shown in Figure 1c, in which LOAD and CONFIG are tied together. Each individual output receives the appropriate input information in a one-shot control pulse. When one output is being programmed, the other outputs remain unaffected until its turn occurs.

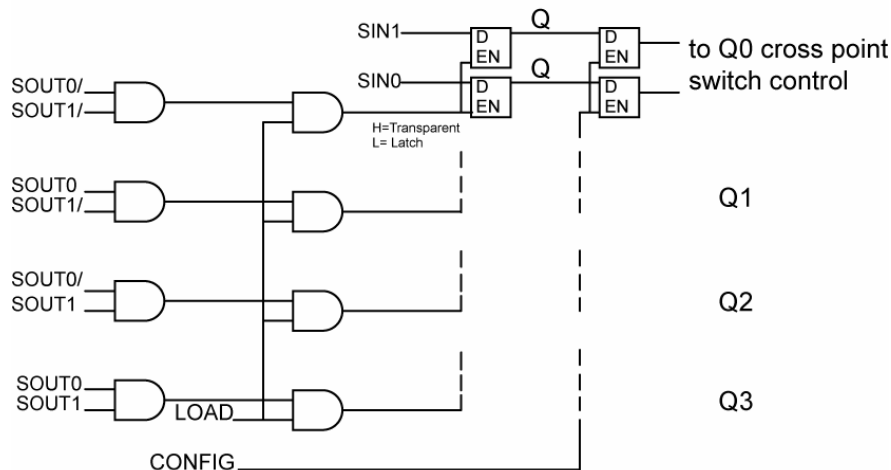


Figure 1a. Simplified Control Circuit

Interface Applications

For Input Interface Applications, see Figures 4a through 4f. For CML Output Termination, see Figures 5a through Figure 5d.

CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ω to 1.2V, DC-coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC-couple with internally terminated receiver, such as 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation. Any unused output pair needs to be terminated when VCCO is 1.2V, do not leave floating.

CML Output Termination with VCCO 1.8V, 2.5V

For VCCO of 1.8V and 2.5V, refer to Figure 5a and Figure 5b, terminate with either 50Ω to VCCO or 100Ω differentially across the outputs. See Figure 5c for AC-coupling.

Input AC-Coupling

The SY56040AR input can accept AC-coupling from any driver. Bypass VT with a 0.1μF low ESR capacitor to VCC as shown in Figures 4c and 4d. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

Timing Diagrams

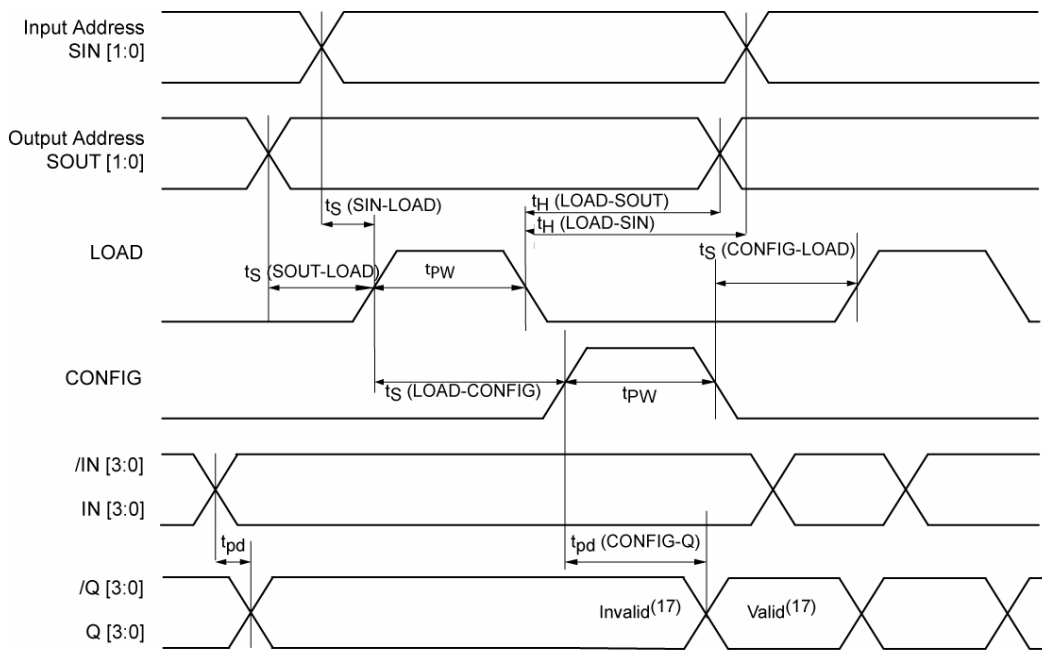


Figure 1b. Dual-Control Mode Timing Diagram

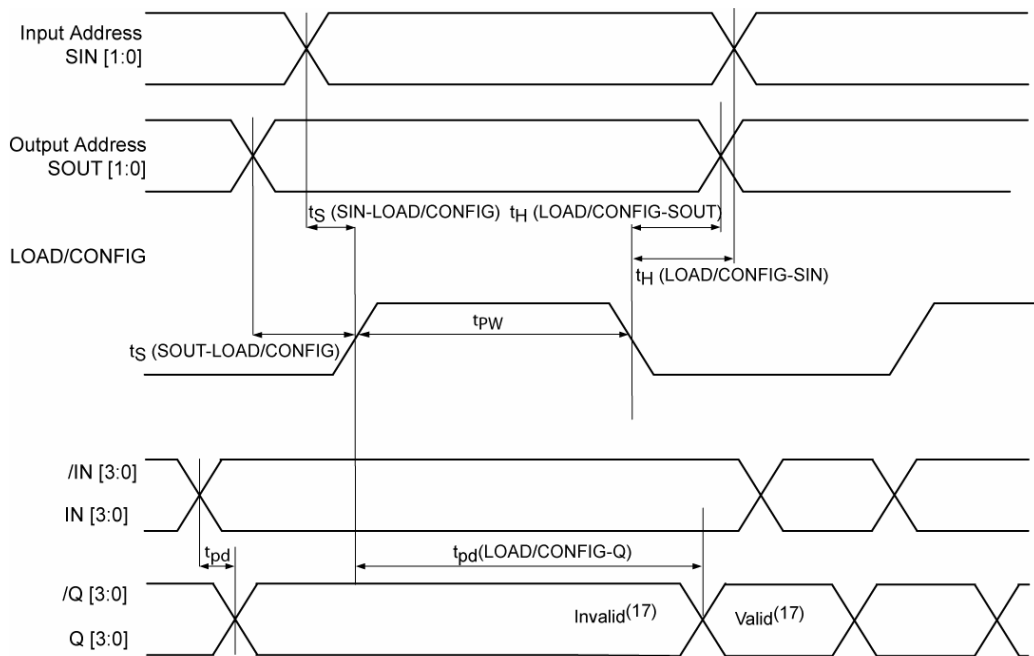
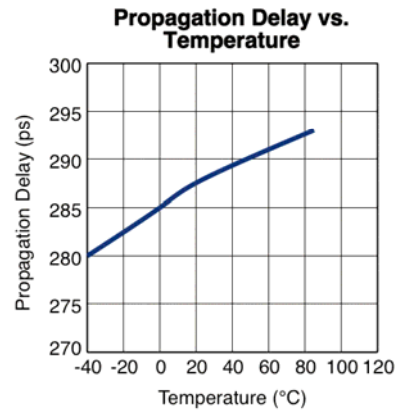
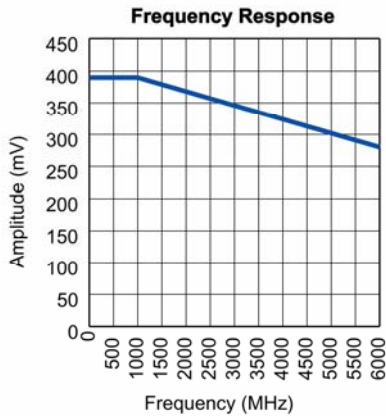


Figure 1c. Single-Control Mode Timing Diagram

Note 17. Invalid and valid refer to configurations being changed. All outputs with unchanged configurations remain valid.

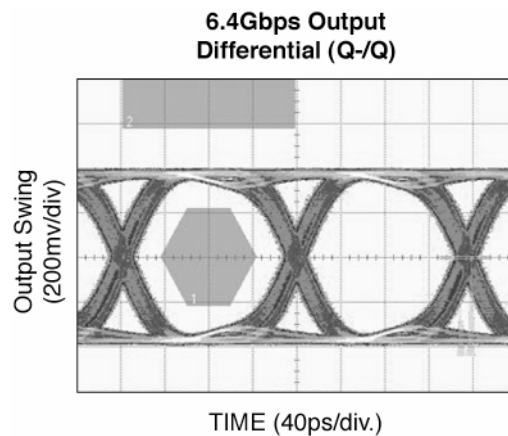
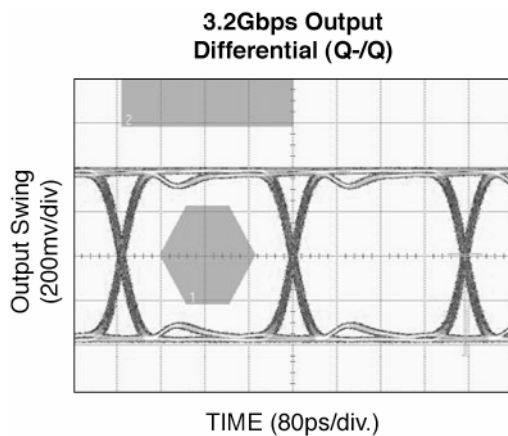
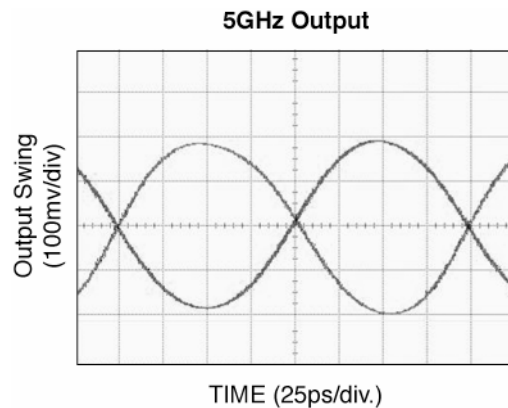
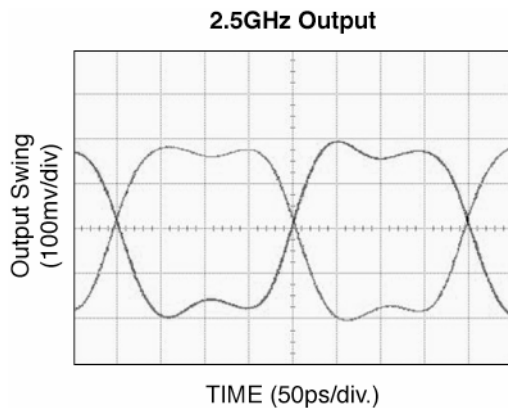
Typical Characteristics

$V_{CC} = 2.5V$, $V_{CCO} = 1.2V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 50\Omega$ to $1.2V$, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 2.5V$, $V_{CCO} = 2.5V$, $GND = 0V$, $V_{IN} = 100mV$, $R_L = 50\Omega$ to $2.5V$, Data Pattern: $2^{23}-1$, $T_A = 25^\circ C$, unless otherwise stated.



Input and Output Stage

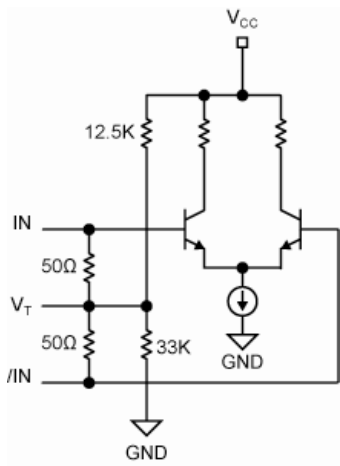


Figure 2a. Simplified Differential Input Buffer

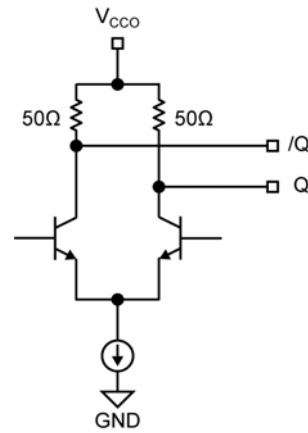


Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings



Figure 3a. Single-Ended Swing

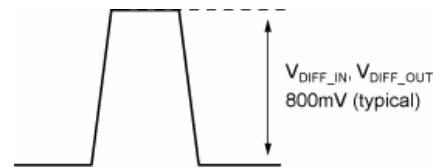


Figure 3b. Differential Swing

Input Interface Applications

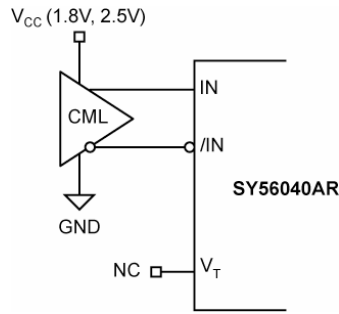


Figure 4a. CML Interface (DC-Coupled, 1.8V, 2.5V)

Option: May connect V_T to V_{CC}

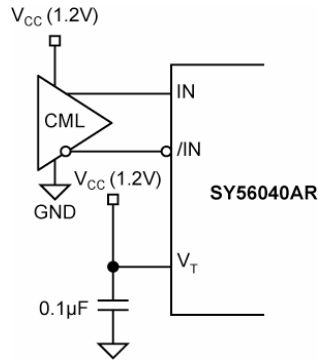


Figure 4b. CML Interface (DC-Coupled, 1.2V)

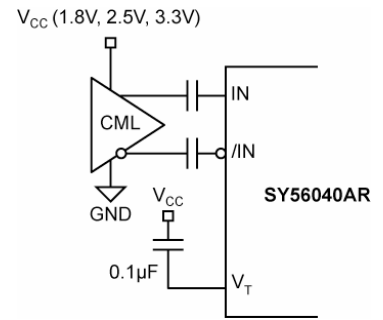


Figure 4c. CML Interface (AC-Coupled)

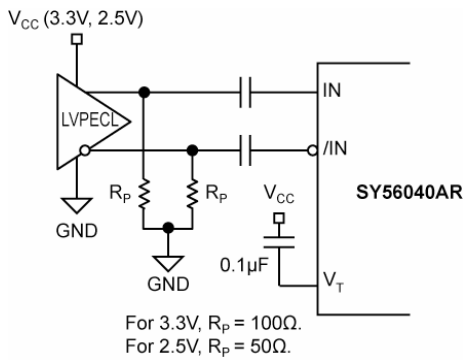


Figure 4d. LVPECL Interface (AC-Coupled)

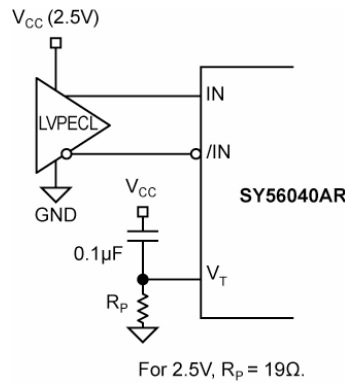


Figure 4e. LVPECL Interface (DC-Coupled)

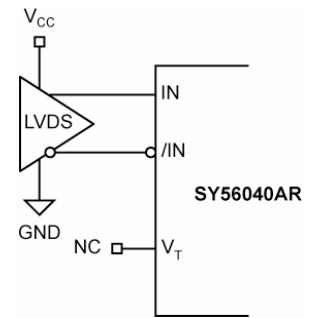
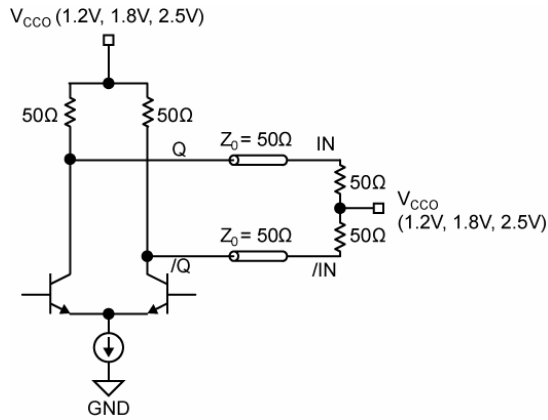
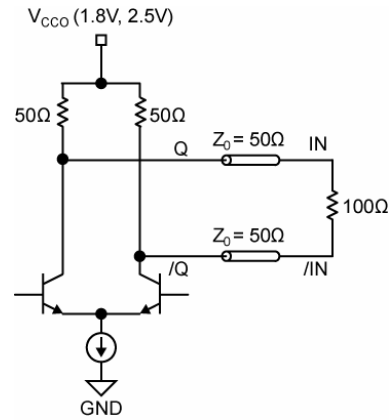


Figure 4f. LVDS Interface

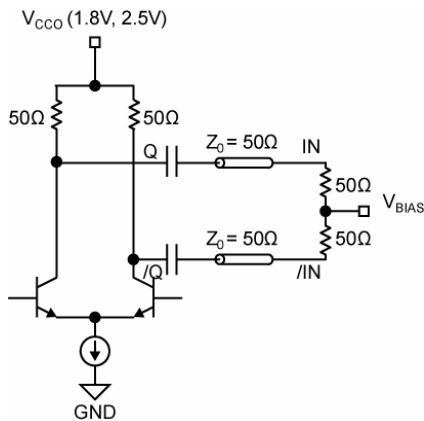
CML Output Termination



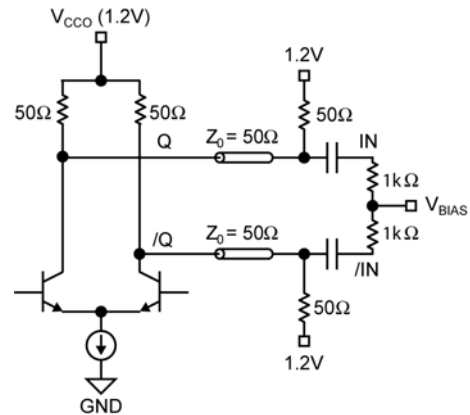
**Figure 5a. 1.2V, 1.8V or 2.5V
CML DC-Coupled Termination**



**Figure 5b. 1.8V or 2.5V
CML DC-Coupled Termination**



**Figure 5c. CML AC-Coupled Termination
(Vcco 1.8V or 2.5V)**

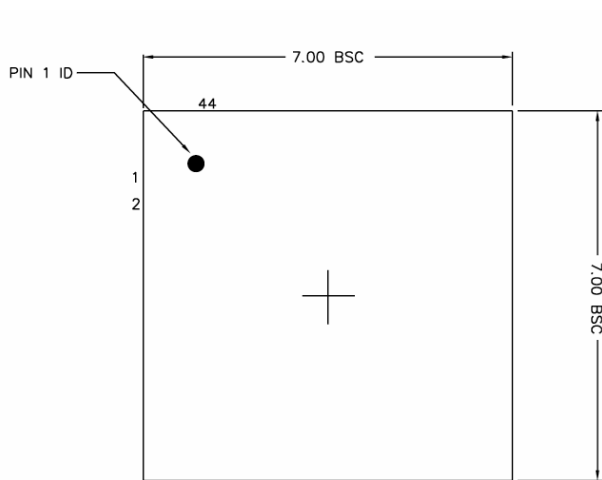


**Figure 5d. CML AC-Coupled Termination
(Vcco 1.2V only)**

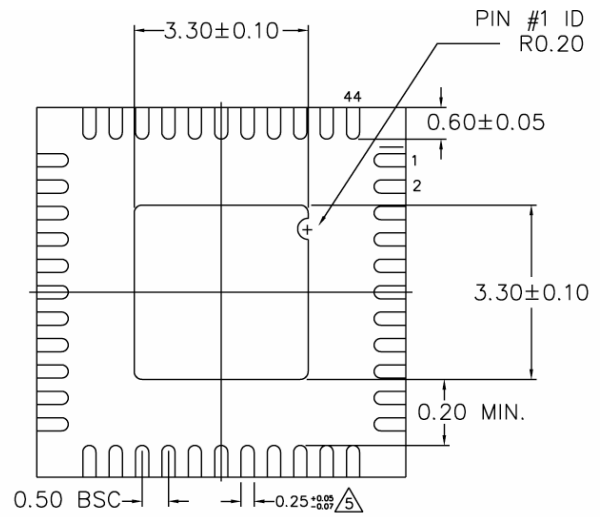
Related Product and Support Documents

| Part Number | Function | Datasheet Link |
|---------------|--|---|
| HBW Solutions | New Products and Termination Application Notes | http://www.micrel.com/page.do?page=/product-info/as/HBWolutions.shtml |
| SY58040U | 4x4 CML switch with internal I/O term. | http://www.micrel.com/_PDF/HBW/sy58040u.pdf#page=3 |
| SY89540U | 4x4 LVDS switch with internal I/O term. | http://www.micrel.com/_PDF/HBW/sy89540u.pdf#page=3 |

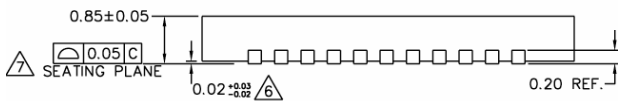
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- ⚠ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- ⚠ APPLIED ONLY FOR TERMINALS.
- ⚠ APPLIED FOR EXPOSED PAD AND TERMINALS.

44-Pin MicroLeadFrame® (MLF-44)

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