

MEC170x Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON IDENTIFICATION

Part Number	Silicon Identifier	Functional Revision C	Functional Revision E
MEC1701	Device ID ⁽¹⁾	2Dh	2Dh
	Revision ID for Silicon Revision ⁽²⁾	02h	04h
	PIS ⁽³⁾ Version/Revision	C1	C2
MEC1703	Device ID ⁽¹⁾	2Eh	2Eh
	Revision ID for Silicon Revision ⁽²⁾	02h	04h
	PIS ⁽³⁾ Version/Revision	F1	F2
MEC1704	Device ID ⁽¹⁾	33h	33h
	Revision ID for Silicon Revision ⁽²⁾	02h	04h
	PIS ⁽³⁾ Version/Revision	C1	C2
MEC1705	Device ID ⁽¹⁾	32h	32h
	Revision ID for Silicon Revision ⁽²⁾	02h	04h
	PIS ⁽³⁾ Version/Revision	C1	C2

Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.
Note 2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h.
Note 3: Product Identification System (PIS) is defined in the Product Data Sheet.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				C	E
SMB Controller	SMB Master	1.	SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only	X	X
Boot ROM	Crisis Recovery	2.	May enter crisis recovery mode in error	X	X
JTAG Pins	Pins	3.	GPIO145 & GPIO146 input disabled in SWD mode	X	X
16 Bit Basic Timer	UPD	4.	Boot ROM for UPD feature does not disable Basic Timer 16 instance 1		X
EEPROM Controller	TEST	5.	For MEC1703 and MEC1705, Test Register at address 0x4000_2C1C needs to be programmed to 0x00060101	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

MEC170x

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				C	E
ESPI	ESPI	6.	MAFS flash transfers should be to/from 4-byte aligned SRAM buffer starting addresses	X	X
ROM API's	ROM API's	7.	Some API's were removed		X
ROM API's	ROM API's	8.	Some QMSPI APIs do not function correctly	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

1. Module: SMBus 2.0 Host Controller

DESCRIPTION

SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only. This issue only occurs in a multi-master environment.

Under firmware control, it is possible to generate a new command on the bus before the Bus Idle time expires, thereby violating the SMBus Idle time.

END USER IMPLICATIONS

The SMBus Master Controller may generate a START condition too soon. The two consequences of this scenario are that another master will issue a transaction that will get corrupted, which is handled by the lost arbitration mechanism, or the MEC170x master will unfairly claim the bus too often.

Work Around

There are two solutions:

- Use the Network Layer instead of Byte mode. This anomaly does not apply to the SMBus Network Layer operation.
- If firmware polls the nBB bit to indicate not busy before asserting the PIN bit and writing the data register, the SMBus Controller will not violate the Bus Idle time.

2. Module: Crisis Recovery Mode

DESCRIPTION

The Boot ROM turns on the internal pull-up on GPIO045 (PVT_STRAP) pin before sampling the GPIO045 input value. It is supposed to sample the pin after waiting a minimum of 1 ms to determine if it should abort the standard SPI Flash load process and boot from the Crisis Recovery SPI Flash over the Private SPI Flash interface. However, the boot code turns on the pull-up and samples the pin immediately without delay. Depending on the external capacitance, this pin may not have enough time to rise to a high-level and may be misinterpreted as low and enter crisis recovery mode in error.

END USER IMPLICATIONS

The device may enter crisis recovery mode in error.

Work Around

Implement external pull-up for normal operation.

3. Module: GPIO145 and GPIO146 Inputs Disabled When JTAG Enabled

DESCRIPTION

GPIO145 and GPIO146 inputs are disabled when JTAG enabled and the JTAG debugger is connected in both 4-wire JTAG mode and 2-wire SWD mode.

END USER IMPLICATIONS

- Cannot use SMB09 when JTAG is enabled and JTAG debugger is connected if device is configured for 2-wire SWD test mode.
- Cannot use GPIO145 and GPIO146 inputs when JTAG is enabled and JTAG debugger is connected if device is configured for 2-wire SWD test mode.

Work Around

None.

4. Module: Boot ROM for UPD feature does not disable 16-bit Basic Timer instance 1

DESCRIPTION

For UPD feature, the Boot ROM turns on 16 bit Basic Timer instance 1 and does not turn it off before jumping into application code. The timer is active only when UPD is enable via eFUSE or strap. This may be required to be turned off during power characterization and normal operation.

END USER IMPLICATIONS

- More power consumed, by the chip, if this timer remains enabled.

Work Around

During application initialization, this timer needs to be disabled.

5. Module: EEPROM Controller

DESCRIPTION

The test register at address 0x4000_2C1C needs to be written to 0x00060101 by the application code during initialization before accessing EEPROM for MEC1703 and MEC1705.

END USER IMPLICATIONS

- EEPROM access may be impacted.

Work Around

During application initialization, the user needs to write the value of 0x00060101 to EEPROM Controller TEST register at address 0x4000_2C1C, before accessing EEPROM.

6. Module: ESPI

DESCRIPTION

All MAFS flash transfers must be to/from 4-byte aligned SRAM buffer starting addresses. The low-order 2 bits of the BUFFER ADDRESS register are reserved and must be written as zeros.

END USER IMPLICATIONS

- Customers are required to start all MAFS flash transfers to/from 4-byte aligned SRAM buffer starting addresses.

Work Around

Start MAFS flash transfers to/from 4-byte aligned SRAM buffer starting addresses.

MEC170x

7. Module: ROM API's

DESCRIPTION

Some APIs have been removed from the Functional Revision E devices.

The “version” API return value can be used to determine the version number of the ROM that corresponds to the functional revision of the device as shown in [Table 3](#) below.

TABLE 3: ROM VERSION NUMBER

Functional Revision	Version API Return Value	Boot ROM Revision	ROM API Manual
C	0x00280032	A1	MEC2016_Rom_A1_API_Manual.docx
E	0x00400232	B0	MEC2016_Rom_B0_API_Manual.pdf

The APIs in [Table 4](#) have been removed from the Functional Revision E devices. Note that all APIs from the Functional Revision C devices, except for those in the [Table 4](#), are present in the Functional Revision E devices.

The replacement for the removed API is shown in the [Table 4](#), if applicable. Please refer to the appropriate ROM API Manual for the device. Note that the replacement API may not be a direct replacement; please refer to the manual for the correct usage of each API.

TABLE 4: REPLACEMENT API'S

No	API in Functional Revision C	Replacement API in Functional Revision E
1	sha_init	api_sha_direct_init
2	sha_update	api_sha_direct_update
3	sha_final	api_sha_direct_finalize
4	sha12_init	api_sha256_init
5	sha12_update	api_sha256_update
6	sha12_finalize	api_sha256_finalize
7	sha35_init	api_sha512_init
8	sha35_update	api_sha512_update
9	sha35_finalize	api_sha512_finalize
10	pke_write_scm32	api_pke_copy_to_scm2
11	rsa_load_key	api_pke_rsa_load_key
12	rsa_load crt_params	api_pke_rsa_load crt_key
13	rsa_encrypt	api_pke_rsa_crypt
14	rsa_decrypt	api_pke_rsa_crypt

END USER IMPLICATIONS

- The APIs listed in the [Table 4](#) above are not present in the Functional Revision E devices. The replacement for the removed API is shown in the [Table 4](#), if applicable. Refer to the appropriate ROM API Manual for the device.

Work Around

Use the version API as described above in [Table 3](#) to determine the version of the device, if required. Use the Replacement APIs in the [Table 4](#) above for functional revision E parts.

8. Module: ROM API's

DESCRIPTION

The following QMSPI APIs do not functional correctly:

- qmspi_cfg_spi_cmd
- qmspi_read_fifo
- qmspi_start_dma

Refer to the QMSPI source code for example QMSPI accesses.

END USER IMPLICATIONS

- Some QMSPI APIs do not functional correctly. Refer to the QMSPI source code for example QMSPI accesses.

Work Around

Refer to the QMSPI source code for example QMSPI accesses.

MEC170x

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet.

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 5: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
ESPI	1.	Maximum ESPI clock frequency
ESPI	2.	eSPI MAFS-Configuration Flash Erase needs a non-zero Transfer Length
WDT	3.	WDT_STATUS bit is Reserved
EFUSE	4.	The ATE Mode bit is located in EFUSE Byte 35
PIS	5.	Version/Revision B added
Device ID	6.	The Device ID for MEC1705Q-C2-SZ is 32h and Revision ID is 84h
WDT	7.	WDT_Count is reset on RESET_SYS
WDT	8.	WDT Event Count Register is not programmed by Boot ROM, but needs to be programmed by application firmware.
PCR	9.	VBAT_RESET_STATUS in Power Clock and Reset block indicates status of RESET_VBAT
PCR	10.	JTAG_RESET_STATUS in Power Clock and Reset block is replaced with JTAG_RST# and indicates current value of JTAG_RST# pin
PCR	11.	Wake Only interrupt example and explanation
Pin Configuration	12.	In Table2-3 and Figure21-2, nSYS_RST should be read as RESET_SYS
PCR	13.	VTR_RESET_STATUS bit Power Clock and Reset block indicates is renamed to RESET_SYS_STATUS
Electrical Specification	14.	In Table 50-11: VTR SUPPLY CURRENT, I_VTR, EC_CLK is gated Off for Light Sleep condition.
RC_ID	15.	TABLE 34-2, TABLE 34-3, TABLE 34-4 are Sample RC values for 24MHz system clock and CLOCK_SET field in the RC_ID Control Register is set to '1'

1. Module: ESPI

This section captures update to ESPI_CLK clock frequencies supported.

ESPI CLOCK FREQUENCIES

The Boot ROM configures the ESPI hardware to default the maximum ESPI_CLK frequency as 50 MHz. This can be changed by customer application code downloaded from SPI Flash to support the maximum 66 MHz clock frequency. However, the ESPI GPIO Pin Control 2 register must be updated to select 12mA with a fast slew rate.

2. Module: ESPI

This section demonstrates eSPI MAFS-Configuration Flash Erase needs a non-zero Transfer Length.

ESPI MAFS-CONFIGURATION FLASH ERASE OPERATION

In Master Attached Flash configuration, before performing an Erase operation, it is necessary to write a non-zero value into the Flash Access Channel Transfer Length Register, which is in the eSPI I/O Component register set at offset 290h. For Erase, the exact value is not important except that it must be non-zero, and a value of '1' is suggested for the sake of code efficiency.

If this is not done, then if zero appears in that register, any Erase command will terminate immediately with the BAD_REQUEST error status bit set, and the requested Erase will not be performed.

3. Module: WDT

This section clarifies which WDT status bit must be used for detecting watchdog timer events.

WDT TIMER EVENTS

The WDT_STATUS bit documented in the WDT Control register is a Reserved bit and cannot be used to detect watchdog timer events.

Bit[5] WDT located in the Power-Fail and Reset Status register in the VBAT Register Bank must be used as the WDT Status bit.

4. Module: EFUSE

This section clarifies where the ATE Mode bit is located in the EFUSE block.

ATE MODE BIT IS LOCATED AT BYTE 35 BIT 7 OF EFUSE MODULE

The ATE Mode bit is located in EFUSE Byte 35 Bit[7]: ATE Mode =0

1=Normal

0=ATE Mode

If ATE Mode bit has not been programmed (i.e., blank parts) then the Boot ROM will perform the following steps:

1. Lock Secure ROM Key
2. Enable 4-wire JTAG
3. Halt Processor

If ATE Mode bit is set, Boot ROM will initialize the device and then begin the SPI Port Selection process defined in the Boot ROM document.

5. Module: Product Information System (PIS)

This section adds another entry for the Version/Revision.

B# B = UNPROVISIONED OTP - CUSTOMER NEEDS TO PROVISION, # = VERSION REVISION NUMBER

Version/Revision: B# B = Unprovisioned OTP, # = Version Revision Number

6. Module: Device ID

This section clarifies the Device ID and Revision ID for MEC1705Q-C2-SZ.

REVISION ID AND DEVICE ID OF MEC1705Q-C2-SZ

For MEC1705Q-C2-SZ, the Device ID is 32h and Revision ID is 84h.

7. Module: WDT

This section clarifies which Reset clears the WDT Count.

WDT COUNT RESET

The WDT_COUNT documented in the WDT Count Register is reset by RESET_SYS and not RESET_SYS_nWDT.

MEC170x

8. Module: WDT

This section clarifies programming of WDT EVENT COUNT Register.

WDT EVENT COUNT REGISTER IS NOT PROGRAMMED BY BOOT ROM

The WDT Event Count Register in EC Subsystem block with offset address 28h has following definition. This field is cleared to 0 on a reset triggered by the main power on reset, but not on a reset triggered by the Watchdog Timer. This field may be used by application firmware to monitor WDT activity. The application firmware must manually increment this register to indicate the number of times a WDT event fired since the chip was last reset by a RESET_SYS_nWDT event.

The recommended procedure is as follows:

1. Check WDT bit located in Power-Fail and Reset Status Register. If WDT = 1, first clear WDT status bit in Power-Fail and Reset Status Register and then increment WDT Event Count register.
2. Enable WDT using the WDT Activation Mechanism defined in Watchdog Timer (WDT) datasheet chapter

9. Module: PCR

The VBAT_RESET_STATUS (bit 5) in PCR Power Reset Status Register indicates RESET_VBAT status and not RESET_VTR.

10. Module: PCR

JTAG_RESET_STATUS bit in PCR Power Reset Status Register is renamed to JTAG_RST# and indicates the current value of JTAG_RST# pin.

JTAG RESET STATUS IS REPLACED WITH JTAG_RST# AND INDICATES STATUS OF JTAG_RST# PIN

The JTAG_RESET_STATUS (bit 7) in PCR Power Reset Status Register is replaced with the JTAG_RST# and indicates the status of JTAG_RST# pin. This is a Read Only bit.

0 = JTAG_RST# pin is low

1 = JTAG_RST# pin is high

Note: This bit always reflects the state of the JTAG_RST# pin even when Boundary Scan Enabled.

11. Module: PCR

This section clarifies Wake-Only Events in Section 4.7.4.1 and gives an example and explanation.

WAKE-ONLY INTERRUPT IN GIRQ22 JUST GENERATES CLOCK FOR THE RESPECTIVE BLOCK AND DO NOT WAKE THE PROCESSOR

The Wake-Only Events and interrupts are responsible for waking up the respective blocks from where the Event or interrupt becomes active, but will not enable the clock to the processor.

For example, when RSMRST is high and there is a desire to wake from an ESPI cycle, GIRQ22[9] is the correct wake source to use. When Chip is asleep and there is a ESPI cycle, the falling edge of the CS will cause the chips clock to turn on the ESPI block, but not the processor itself. Upon conclusion of the ESPI cycle, if no ESPI interrupt was generated (i.e. most cycles), then the clock to the ESPI block will go off, and the chip will go back to sleep. If the ESPI cycle creates an interrupt to the processor (i.e. downstream wire or downstream OOB packet for example), then an processor interrupt will be generated if enabled and the clock will remain on and the processor can service the interrupt and the processor can put the chip back to sleep when it has completed its work.

Note: The ESPI Reset itself is NOT a wake event. If wake from ESPI reset is required, then the GPIO interrupt for the ESPI reset pin can be used as a wake event.

12. Module: Pin Configuration

nSYS_RST in TABLE 2-3 heading and FIGURE 21-2 should be read as RESET_SYS.

13. Module: PCR

The VTR_RESET_STATUS (bit 6) in PCR Power Reset Status Register is replaced with RESET_SYS_STATUS and indicates the status of RESET_SYS. This R/WC bit is set any time the RESET_SYS signal is asserted.

14. Module: Electrical Specification

POWER CONSUMPTION IN LIGHT SLEEP

Table 50-11, VTR SUPPLY CURRENT, I_VTR incorrectly indicates the EC_CLK frequency is 12MHz in Light Sleep. The EC_CLK is gated Off (0 MHz) in Light sleep condition.

15. Module: RC_ID

Section 34.11 Time Constants in MEC170x Data sheet incorrectly states following statement “In the following tables, the [CLOCK_SET](#) field in the [RC_ID Control Register](#) is set to ‘0’, so the time base for measuring the rise time is 48MHz, the speed of the system clock”. The correct speed of the system clock is 24MHz for the count value listed in Table 34-2, Table 34-3 and Table 34-4.

SYSTEM CLOCK USED TO MEASURE COUNT IS 24MHZ

The correct statement for Section 34.11 is listed below.

“This section lists a set of R and C values which can be connected to the RC_ID pin. Note that rise time generally follow RC time Tau. Firmware should use the Max and Min Counts in the tables to create quantized states.

In the following tables, the CLOCK_SET field in the RC_ID Control Register is set to ‘1’, so the time base for measuring the rise time is 24MHz, the speed of the system clock. All capacitor values are $\pm 10\%$ and all resistor values are $\pm 5\%$.

Minimum and maximum count values are suggested ranges, calculated to provide reasonable margins around the nominal rise times. Rise times have been confirmed by laboratory measurements.”

MEC170x

APPENDIX A: DOCUMENT REVISION HISTORY

Revision	Description
DS80000704E (03-19-18)	Added Data Sheet Clarification # 15. - TABLE 34-2, TABLE 34-3, TABLE 34-4 are Sample RC values for 24MHz system clock and CLOCK_SET field in the RC_ID Control Register is set to '1'.
	Added Data Sheet Clarification # 6. - The Device ID for MEC1705Q-C2-SZ is 32h and Revision ID is 84h. Added Data Sheet Clarification # 7. - WDT_Count is reset on RESET_SYS. Added Data Sheet Clarification # 8. - WDT Event Count Register is not programmed by Boot ROM, but needs to be programmed by application firmware. Added Data Sheet Clarification # 9. - VBAT_RESET_STATUS in Power Clock and Reset block indicates status of RESET_VBAT. Added Data Sheet Clarification # 10. - JTAG_RESET_STATUS in Power Clock and Reset block indicates should be JTAG_RST#. Added Data Sheet Clarification # 11. - Wake Only interrupt example and explanation. Added Data Sheet Clarification # 12. - In Table 2-3 and Figure 21-2, nSYS_RST should be read as RESET_SYS. Added Data Sheet Clarification # 13. - VTR_RESET_STATUS bit Power Clock and Reset block indicates is renamed to RESET_SYS_STATUS. Added Data Sheet Clarification # 14. - In Table 50-11: VTR SUPPLY CURRENT, I_VTR, EC_CLK is gated off in Light Sleep condition. Added Silicon Summary Issue # 7. - Some API's were removed. Added Silicon Summary Issue # 8. - Some QMSPI APIs do not function correctly.
DS80000704D (01-11-18)	Added Data Sheet Clarification # 4. - The ATE Mode bit is located in EFUSE Byte 35. Added Data Sheet Clarification # 5. - Version/Revision B added to Product Information System.
DS80000704C (10-05-17)	Added Silicon Summary Issue # 5.and 6.
	Added column for Function Rev E to Table 2, "Silicon Issue Summary," on page 1 Added Silicon Summary Issue # 4.
DS80000704B (01-30-17)	Added column for Function Rev C to Table 2, "Silicon Issue Summary," on page 1 . Added Data Sheet Clarification # 2. - eSPI MAFS-Configuration Flash Erase needs a non-zero Transfer Length. Added Data Sheet Clarification # 3. - WDT_STATUS bit is Reserved.
DS80000704A (07-15-16)	Initial release.

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MEC170x

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